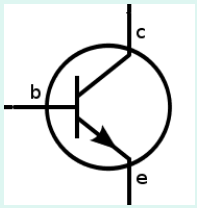
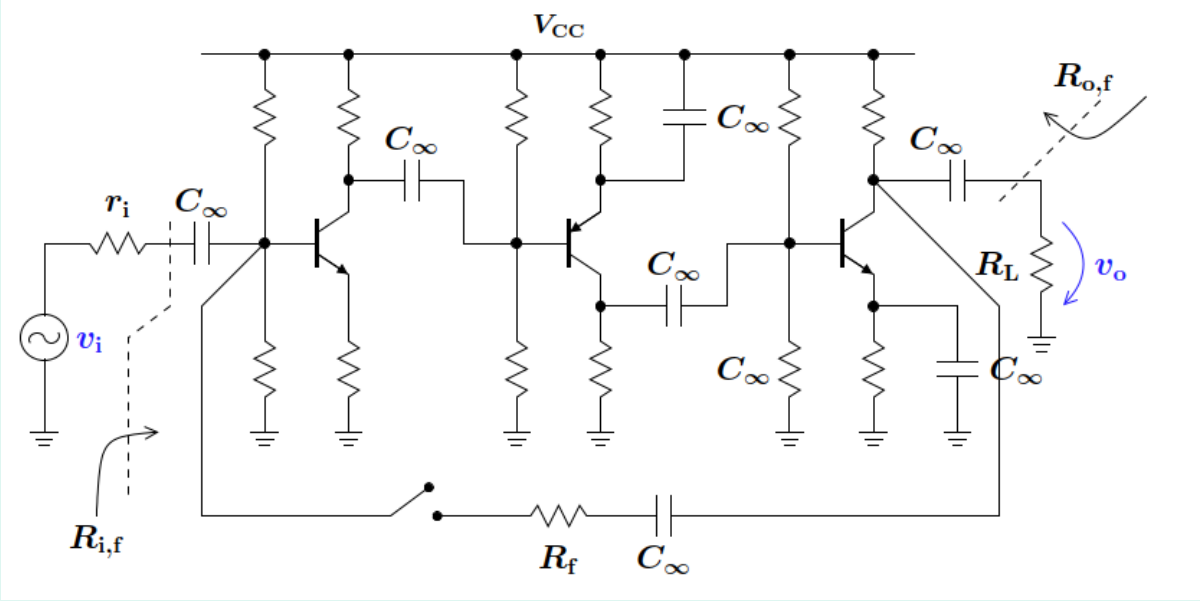
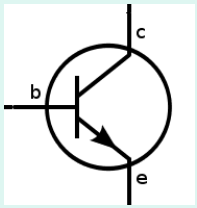


ELEC 301 - Electronic Circuits

L03 - Sep 09

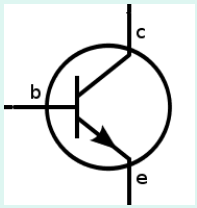
Instructor: Edmond Cretu





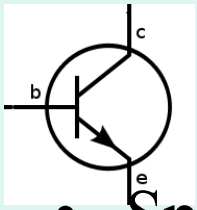
Last time - system level perspective

- Key performance indicators for a system
- Information processing - Shannon channel capacity - link B, S,
- Structured electronic circuits design from information flow perspective - design by separate optimizations for N, B, S
- Open loop vs. closed loop systems

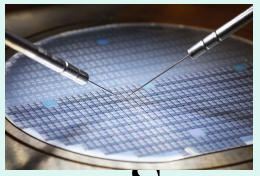


Physical implementation perspective

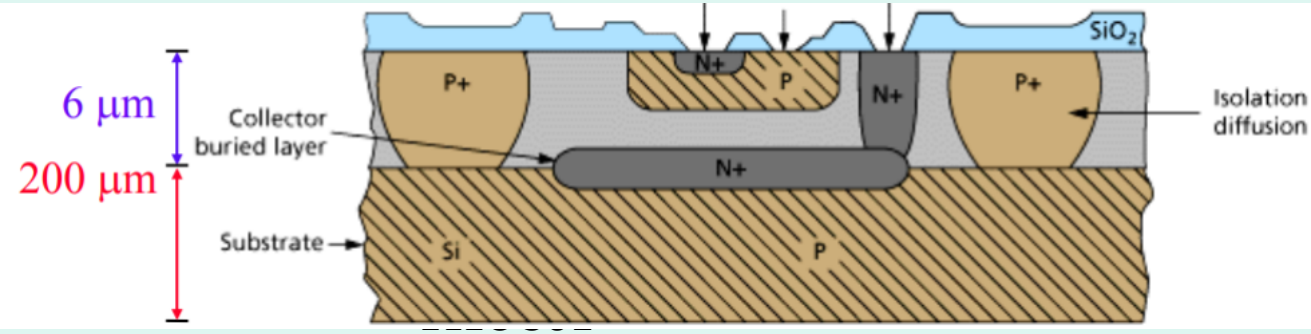
- PCB vs. ASIC design
- The circuit design strategy can vary significantly, depending on the final design target



ASIC design

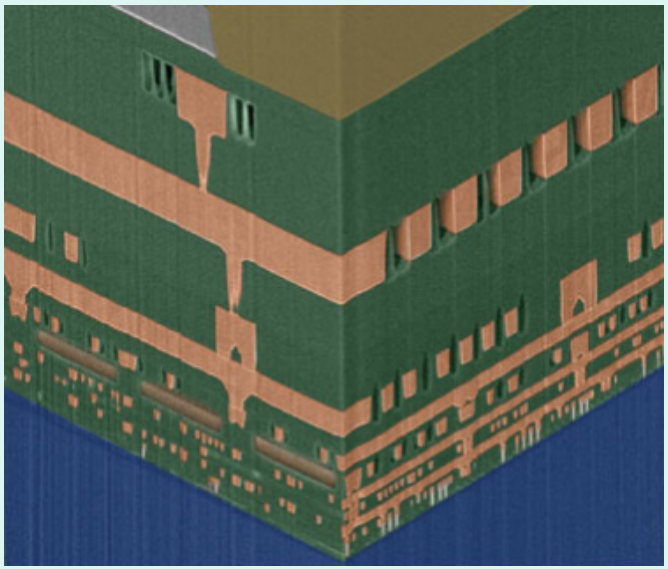


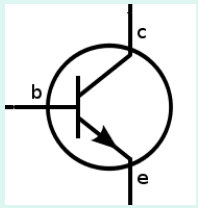
- Specialized (costly) microfabrication technologies: Si CMOS/bipolar for signal processing, SiC or GaN for power/radiation resistant applications, GaAs for HF, Si photonics (PICs)
- International Roadmap for devices and systems - CMOS downscaling: 5nm process (gate length = 18nm)
- Usually surface components (2..10um region of Si wafer)
- Advanced technologies: 3D structures, TSV, TGV
- For interconnects: 6-15 metal layers (Cu), min interconnect widths ~ 10-25nm



IBM Airgap technology

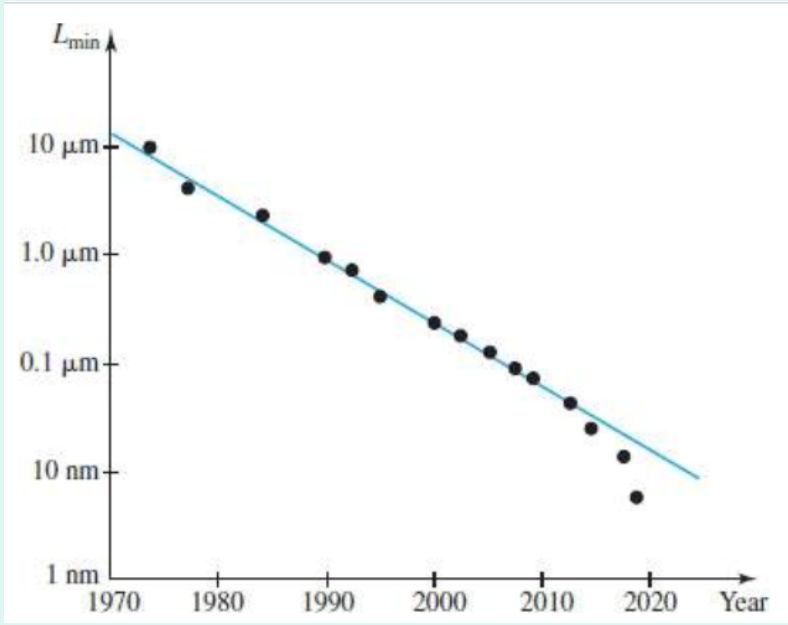
- IBM Airgap technology, to minimize parasitic capacitances – present microelectronics is constrained by the **transmission of information (scaling problem)**
- Some chips contain more than 500km of metal interconnects!!!





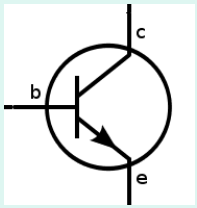
Scaling “laws”

- Moore’s law: with every new technology generation, the transistor area (MOSFET) has been reduced by a factor of about 2 - lasted for about of almost 50 years (MOSFET channel length reduced by a factor of 2 about every 5 years)
- “More than Moore” - use different approaches than just geometry scaling



Structural innovations in Si-based transistors

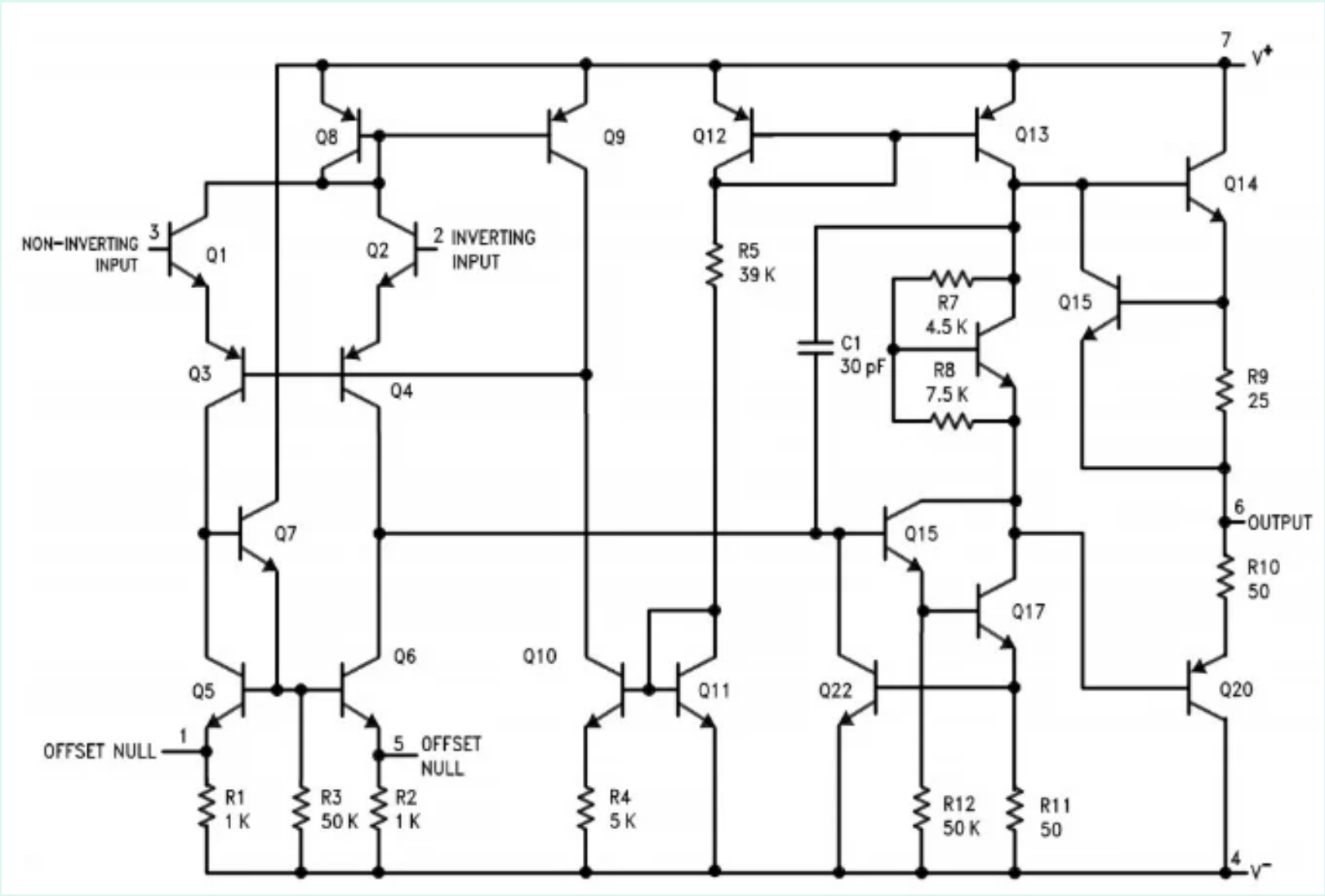
Source: https://www.semiconductor-digest.com/new-structure-transistors-for-advanced-technology-node-cmos-ics

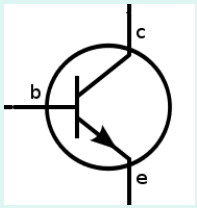


ASIC challenges and design strategies

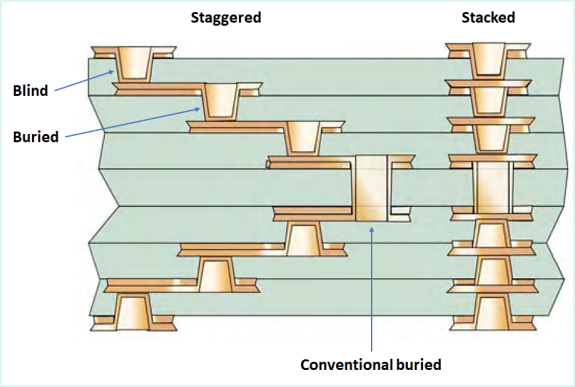
- Challenges:
  - large individual tolerances (10%), but very good matching of component pairs (<1%) (improved through physical layout)
  - Downscaling makes 2nd order effect to become more important - need for complex simulation tools
  - Technology optimized for one dominant component: BJT. CMOS, MOSFET - microelectronics progress driven by technology advances
  - poor L, poor high R - large area, minimize their use
  - insulation between blocks/components through reversed biased junctions (voltage-depending C coupling) - signal integrity aspects
- Design strategies:
  - All blocks rely on the optimized component: resistor as transistor in the linear region, voltage source (PTAT), current mirrors (Widlar)
  - Specific techniques: switched-capacitor, current mode amplifiers
  - Minimize chip area, use differential transistor pairs

Texas Instruments - LM741



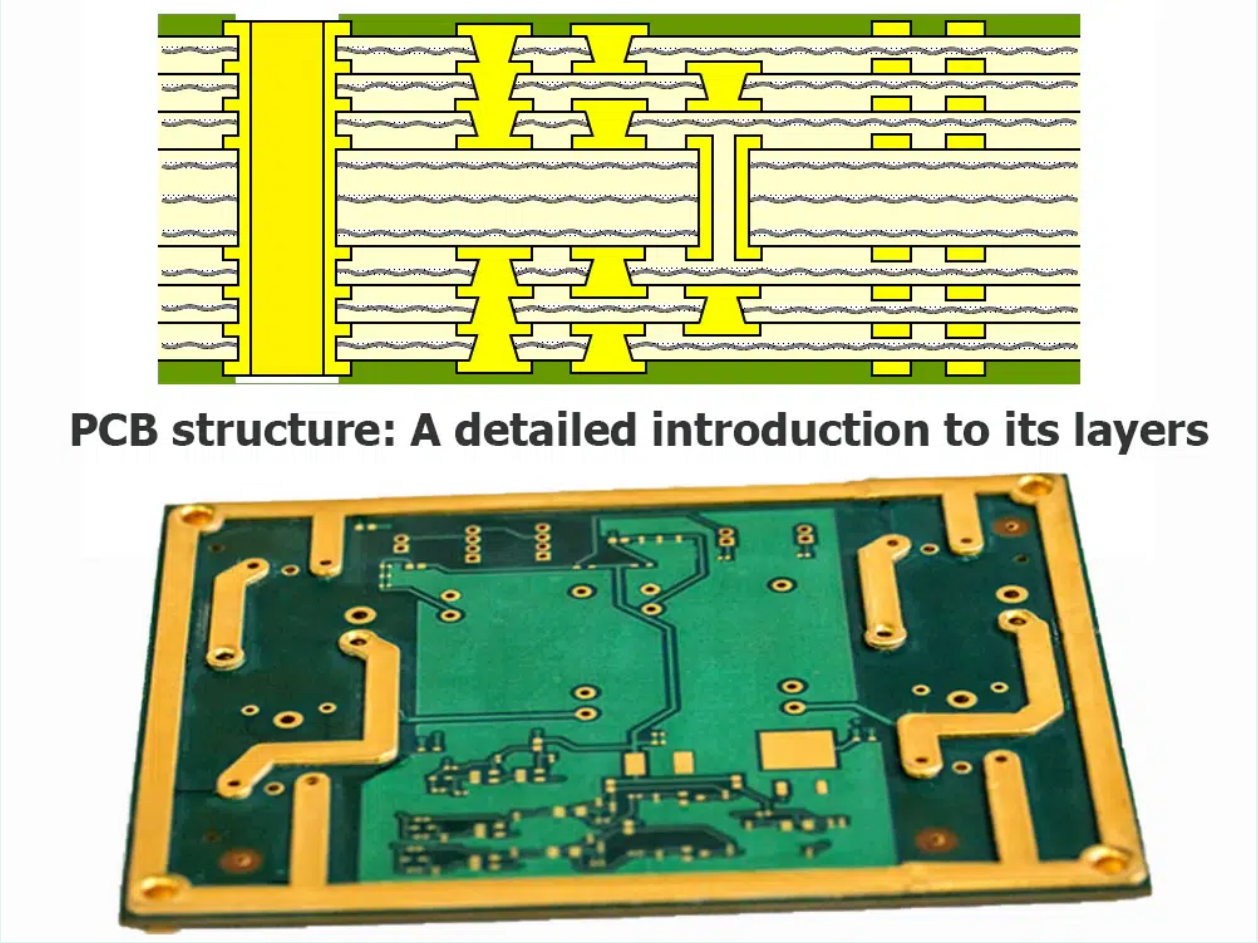


PCB - based design

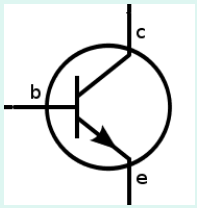


- Features:
  - off-the-shelf components
  - poor differential matching as individual OTS devices
  - trade-off tolerance/cost
  - good R,L,C, D, transformers - discrete components
  - **4-124 layers** (7.6mm thick) PCB, rigid or flexible
  - Minimum trace width - std is 6mils (0.152mm), depends on Cu thickness, 4mils (0.101mm) achievable
  - Different insulating material layers - trade-off performance/cost (dielectric constant (DK), dissipation factor (DF), thermal conductivity (TC), CTE
  - Materials: FR4, flexible polyimide, rigid polyimide - PTFE/glass, PTFE/ceramic, etc.
  - innovation in high-density interconnect (HDI), microvias, optical interconnects

PCB structure



Source: https://www.pcbaaa.com/pcb-structure

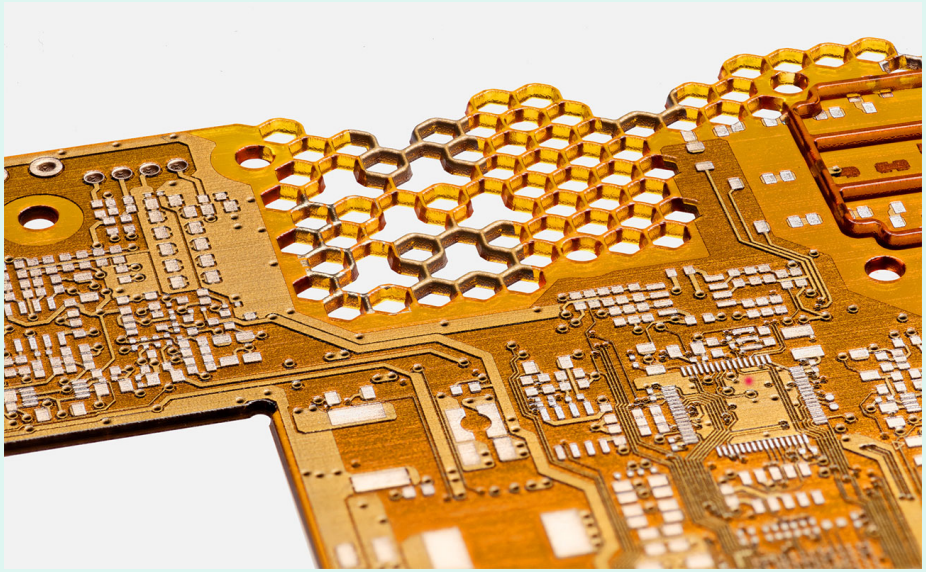


PCB design

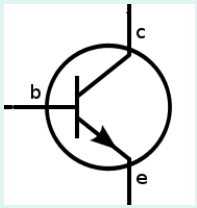
- Specialized software: Altium Designer, Cadence OrCAD, Siemens PADS, Zuken CADSTAR PCB, etc
- AI modules for optimizing routing, vias
- Differential/balanced traces, separation of digital and analog paths, ground planes shielding
- COTS Commercial off-the-shelf) components
- Focus on interconnects - components mounted top and bottom

NanoDimension - DragonFly

- Multimaterial, multi-layer 3D printer - substrate, conductive traces, passive components

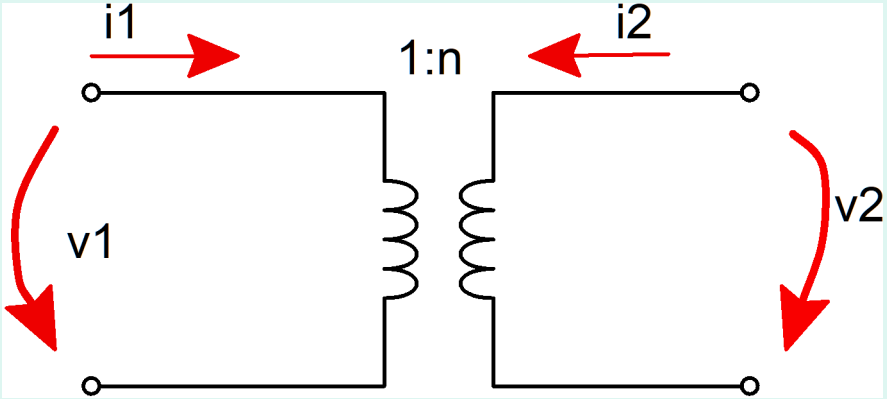


Source: https://www.nano-di.com/dragonfly-iv



Signal amplification principle

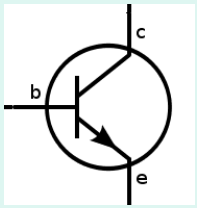
- Goal: signal energy amplification, not only the voltage/current amplitude
- A transformer is not an active device that provides power gain! (energy conservative diport)



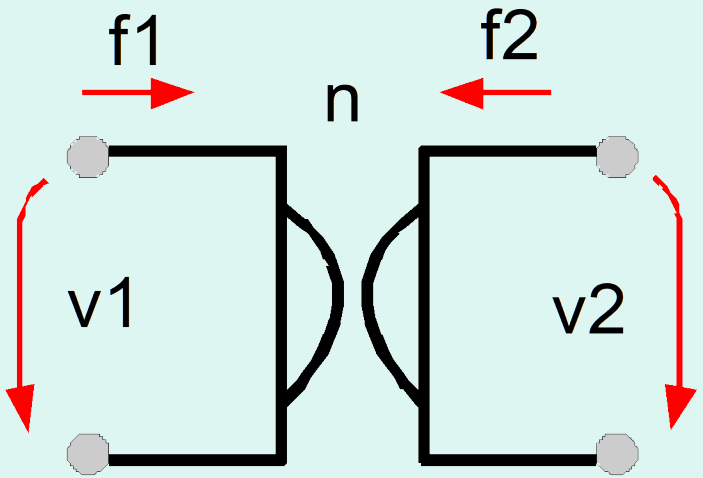
- n=transformer modulus/ratio
- voltage -> voltage
- Constitutive relations:

$$\begin{pmatrix} v_2 \\ i_2 \end{pmatrix} = \begin{pmatrix} n & 0 \\ 0 & -\frac{1}{n} \end{pmatrix} \begin{pmatrix} v_1 \\ i_1 \end{pmatrix}$$

Homework: what is a gyrator?



Generalized gyrator (across -> through)



$$f_1 v_1 + f_2 v_2 = 0$$

- n=gyrator modulus
- Across -> through
- Constitutive relations:

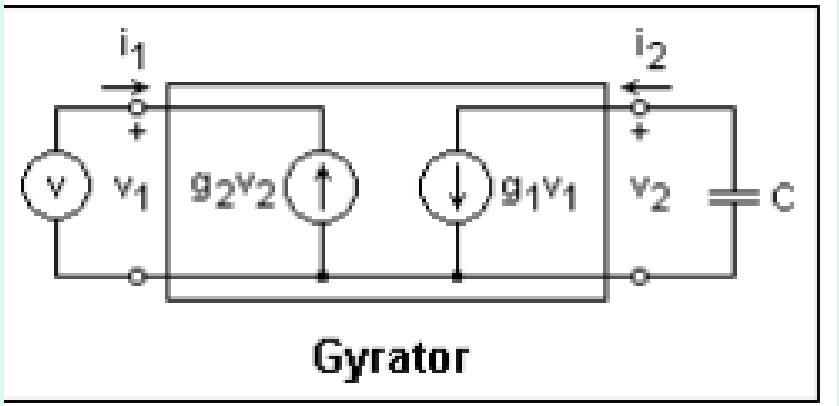
$$\begin{pmatrix} v_2 \\ f_2 \end{pmatrix} = \begin{pmatrix} 0 & n \\ -\frac{1}{n} & 0 \end{pmatrix} \begin{pmatrix} v_1 \\ f_1 \end{pmatrix}$$

- Two chained gyrators = transformer => gyrator is irreducible element
- Impedance transformation using transformers/gyrators

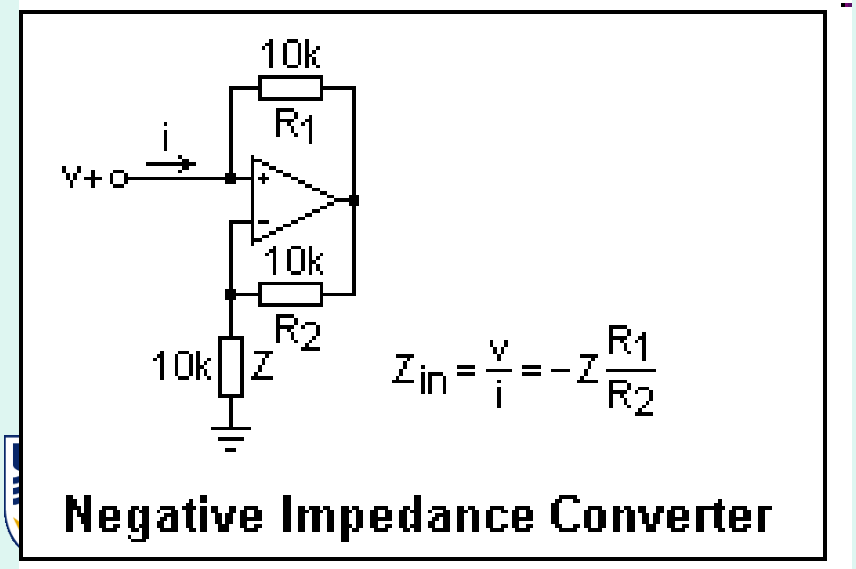
Gyrator as impedance converter

i1 = (g1g2/jωC)v, or Z = jω(C/g1g2) = jωL => a capacitive reactance is converted to an inductive reactance. The circuit effectively inverts its load impedance, changing 1/jωC into jωC.

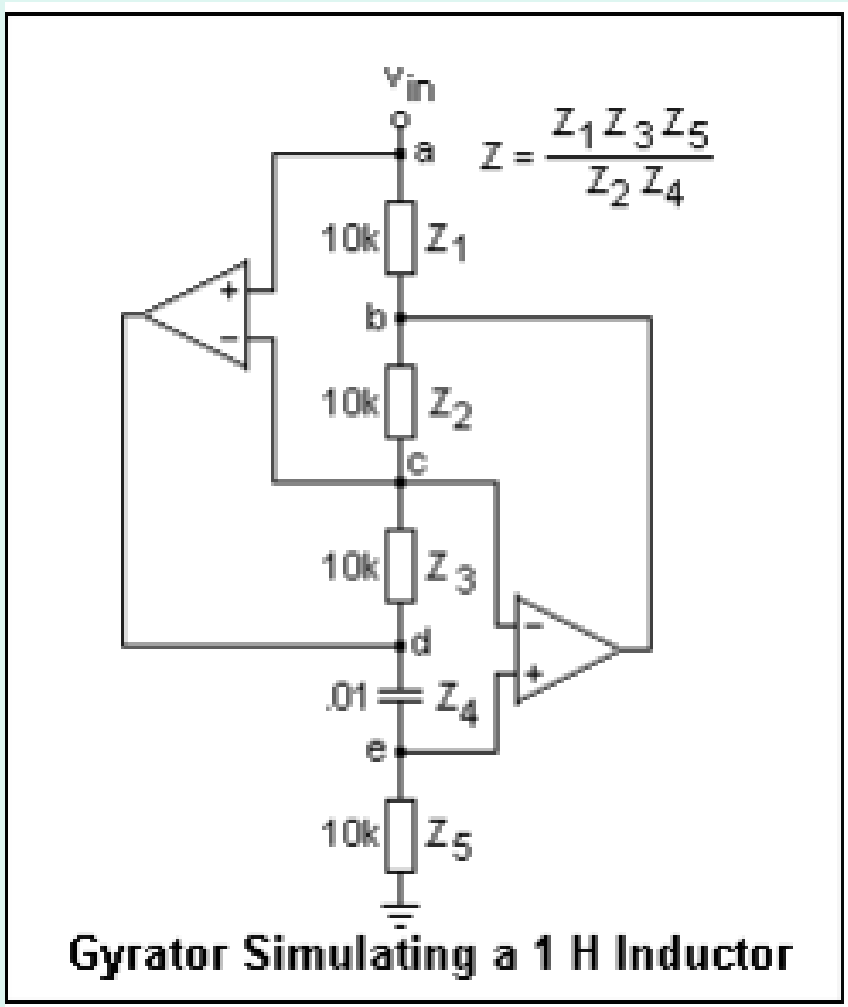
- Electronic implementation: **GIC (Generalized Impedance Converter)** (with op amps)



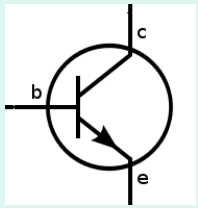
Gyrator



Negative Impedance Converter

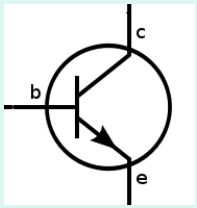


Gyrator Simulating a 1 H Inductor



Signal amplification

- Requirements:
- separation input-output => diport for signal propagation
- min. absorption input signal energy
- $p_{out} = v_{out} * i_{out} > p_{in} = v_{in} * i_{in}$
- Energy conservation: where do we get the extra power?



Amplification principle

- Transfer of energy from DC to signal - it is required to have a nonlinear device!
- Amplification is a nonlinear process!

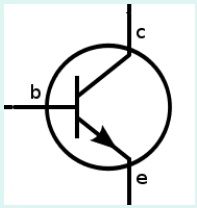
$$y = f(u)$$

$$\begin{cases} u(t) = U_{DC} + \Delta u(t) = U_{DC} + u_{ac}(t), \ |u_{ac}| \ll U_{DC} \\ y(t) = Y_{DC} + \Delta y(t) = Y_{DC} + y_{ac}(t), \ |y_{ac}| \ll Y_{DC} \end{cases}$$

Small signal model:

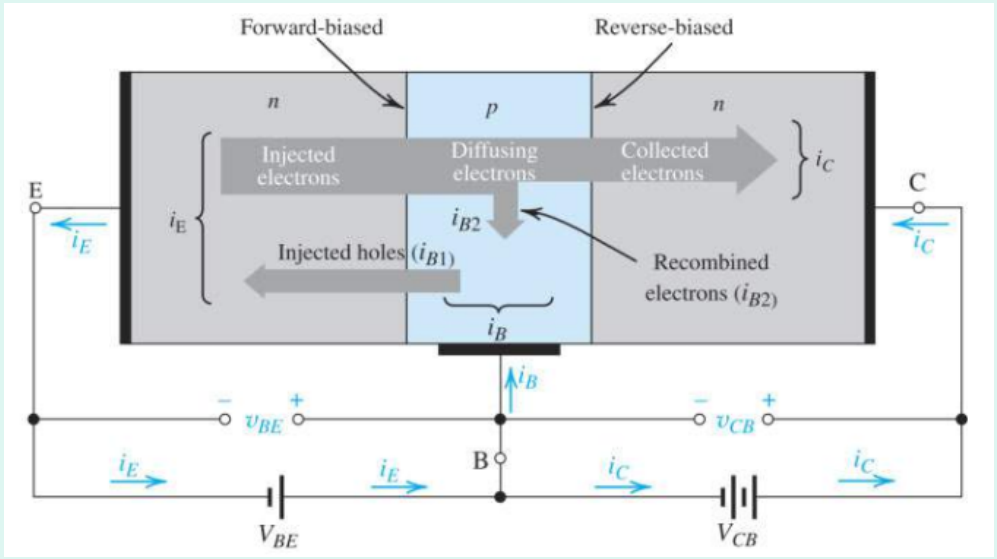
$$Y_{DC} + y_{ac} = f(U_{DC} + u_{ac}) \approx \underbrace{f(U_{DC})}_{Y_{DC}} + \underbrace{\left.\frac{\partial f}{\partial u}\right|_{u=U_{DC}} u_{ac}}_{y_{ac}}$$

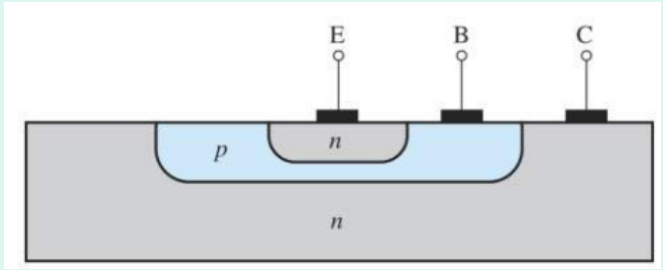
$$y_{ac}(t) = \left.\frac{\partial f}{\partial u}\right|_{u=U_{DC}} u_{ac}$$

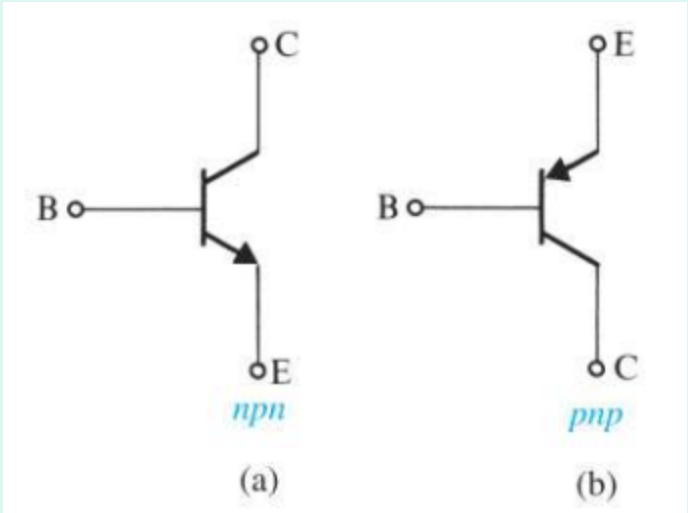


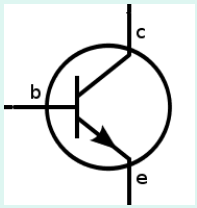
Example - Bipolar junction transistor (BJT)

- Active mode of operation: BE junction forward biased, BC junction reverse biased



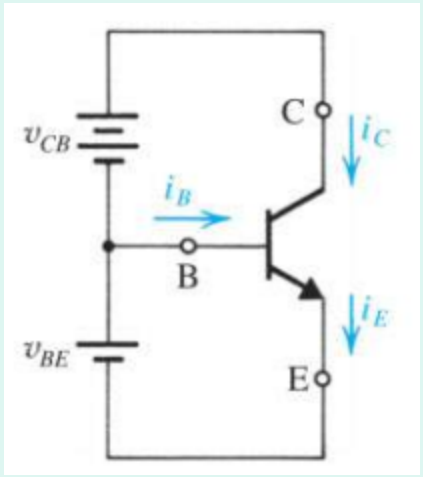


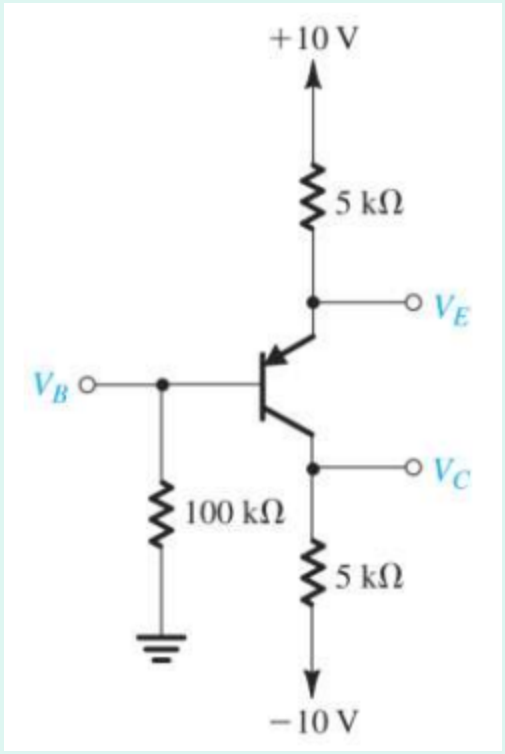


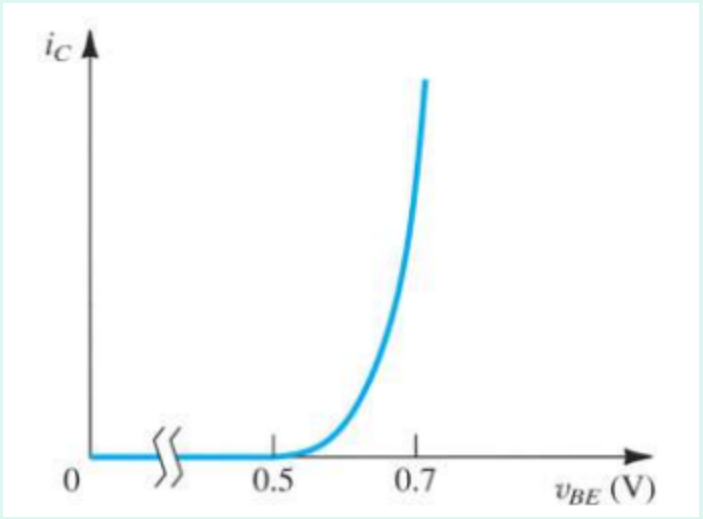


Signal amplification operation

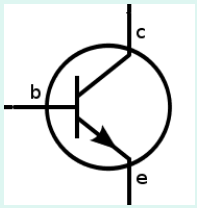
- input signal: v_{be}, output signal i_c



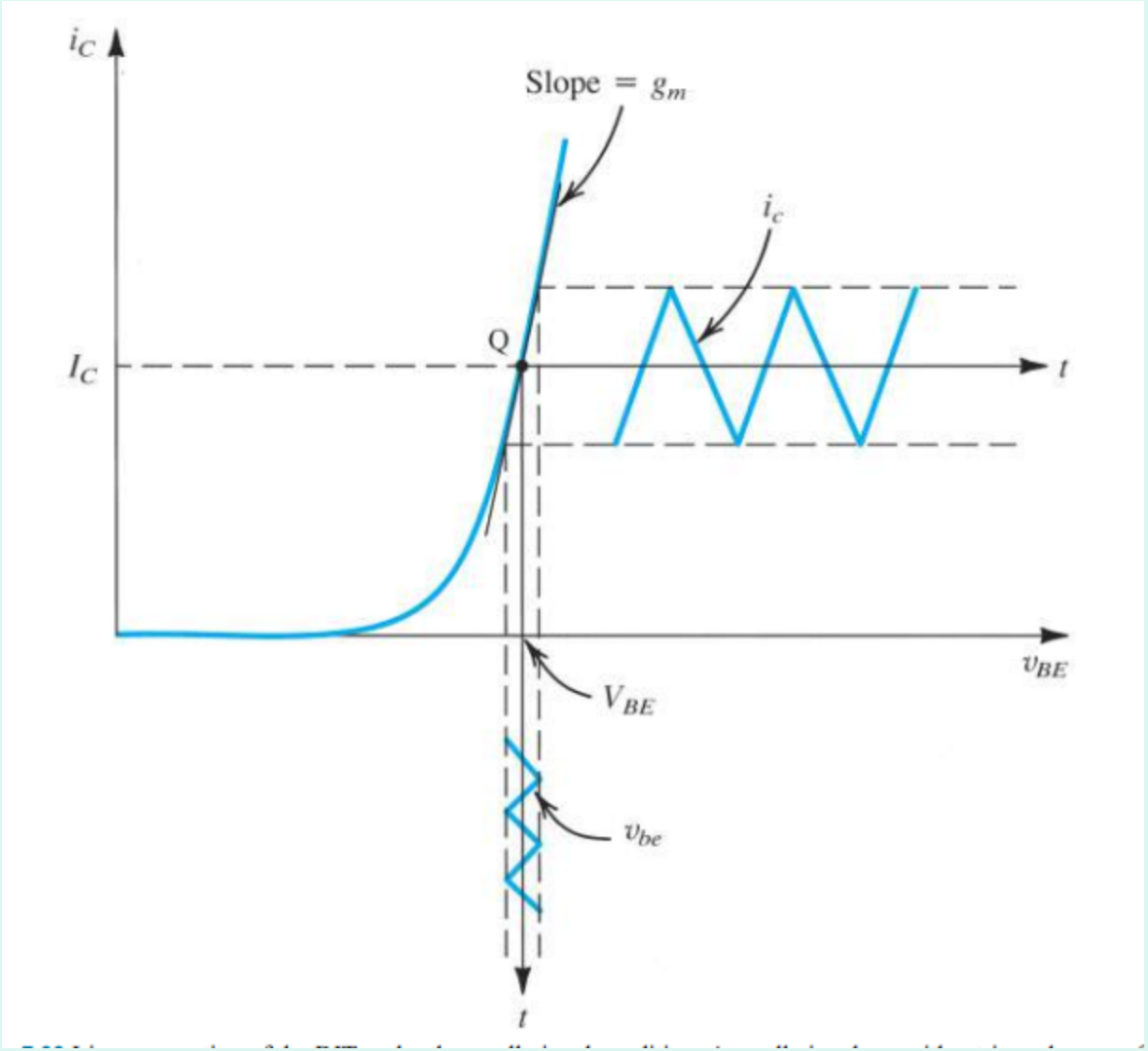


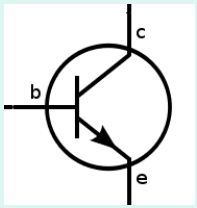


$$i_C(t) = I_S e^{v_{BE}/V_T} \Rightarrow i_C \approx \underbrace{I_S e^{V_{BE}/V_T}}_{I_{C0}} + \underbrace{\frac{I_S e^{V_{BE}/V_T}}{V_T}}_{g_m = I_{C0}/V_T} v_{be}(t)$$



Amplification



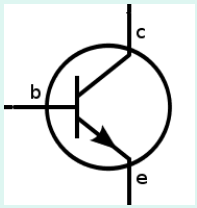


Amplification principle

- We need separate input output ports
- Energy is transferred from DC (battery) to signal through the inherent nonlinearity of the device
- **Question**: is this the best we can do? DC levels are very prone to noise
- Comparison BJT vs MOSFET:

$$i_C(t) = I_S e^{v_{BE}/V_T} \Rightarrow i_C \approx \underbrace{I_S e^{V_{BE}/V_T}}_{I_{C0}} + \underbrace{\frac{I_S e^{V_{BE}/V_T}}{V_T}}_{g_m = I_{C0}/V_T} v_{be}(t)$$

$$i_D(t) = \frac{1}{2}k'\frac{W}{L}\left(v_{GS}(t) - V_T\right)^2 \approx \underbrace{\frac{1}{2}k'\frac{W}{L}\left(V_{GS} - V_T\right)^2}_{I_{D0}} + \underbrace{k'\frac{W}{L}\left(V_{GS} - V_T\right)}_{g_m} \cdot v_{gs}(t)$$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