ELEC 301 - Differential amplifier

L18 - Oct 21

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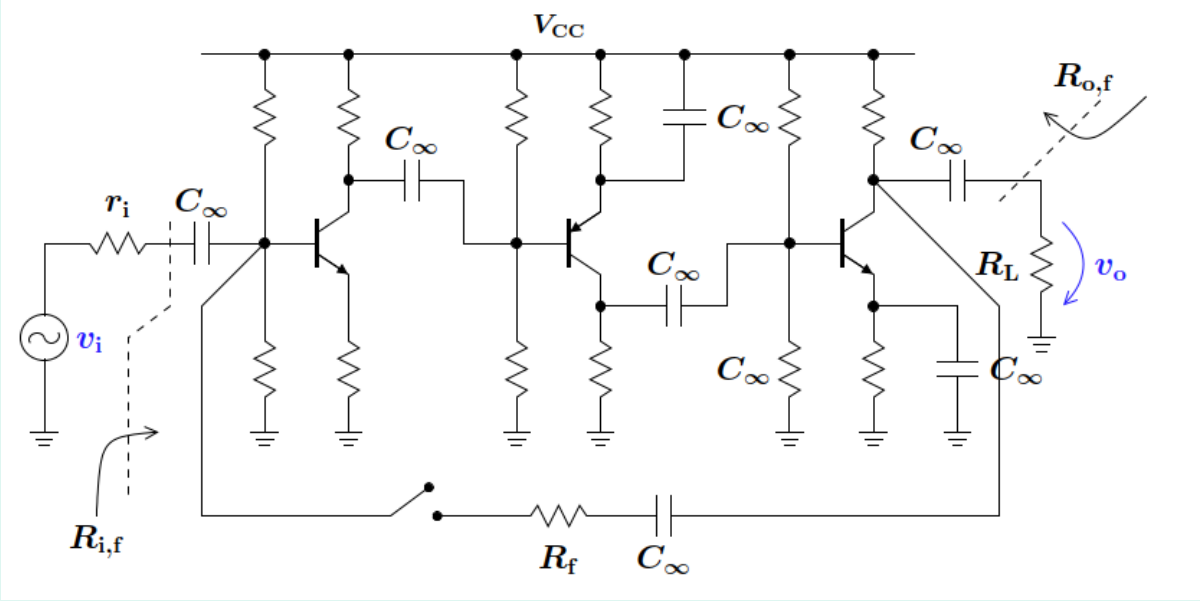
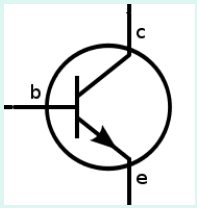
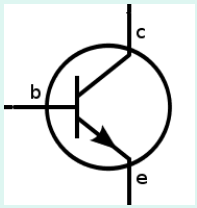




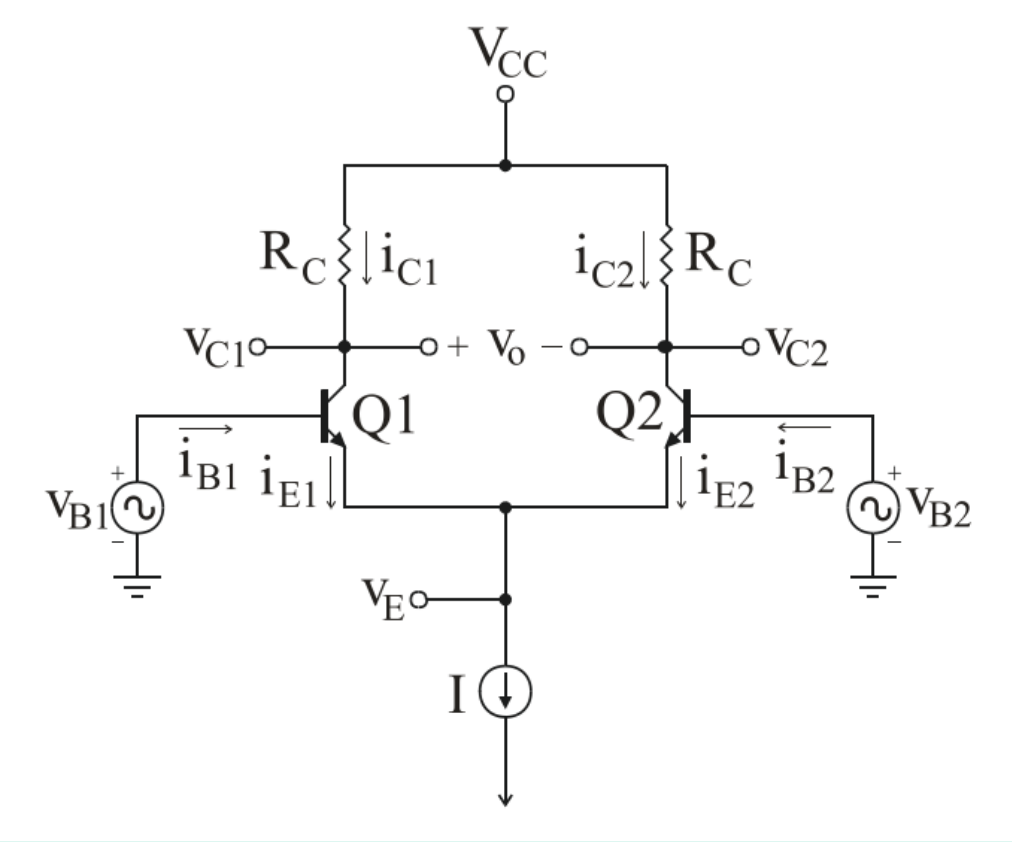
Last time

- Review for midterm + Midterm
- Single-transistor amplifier stages
  - CE: workhorse, general purpose gain stage
  - CB: small R_{in}, large R_{out}, unity A_i, A_v similar to CE
  - CC (Emitter follower): large R_{in}, small R_{out}, unity A_v, same A_i as CE
- Power gain: $A_p = A_i * A_v$



Today: Differential amplifier

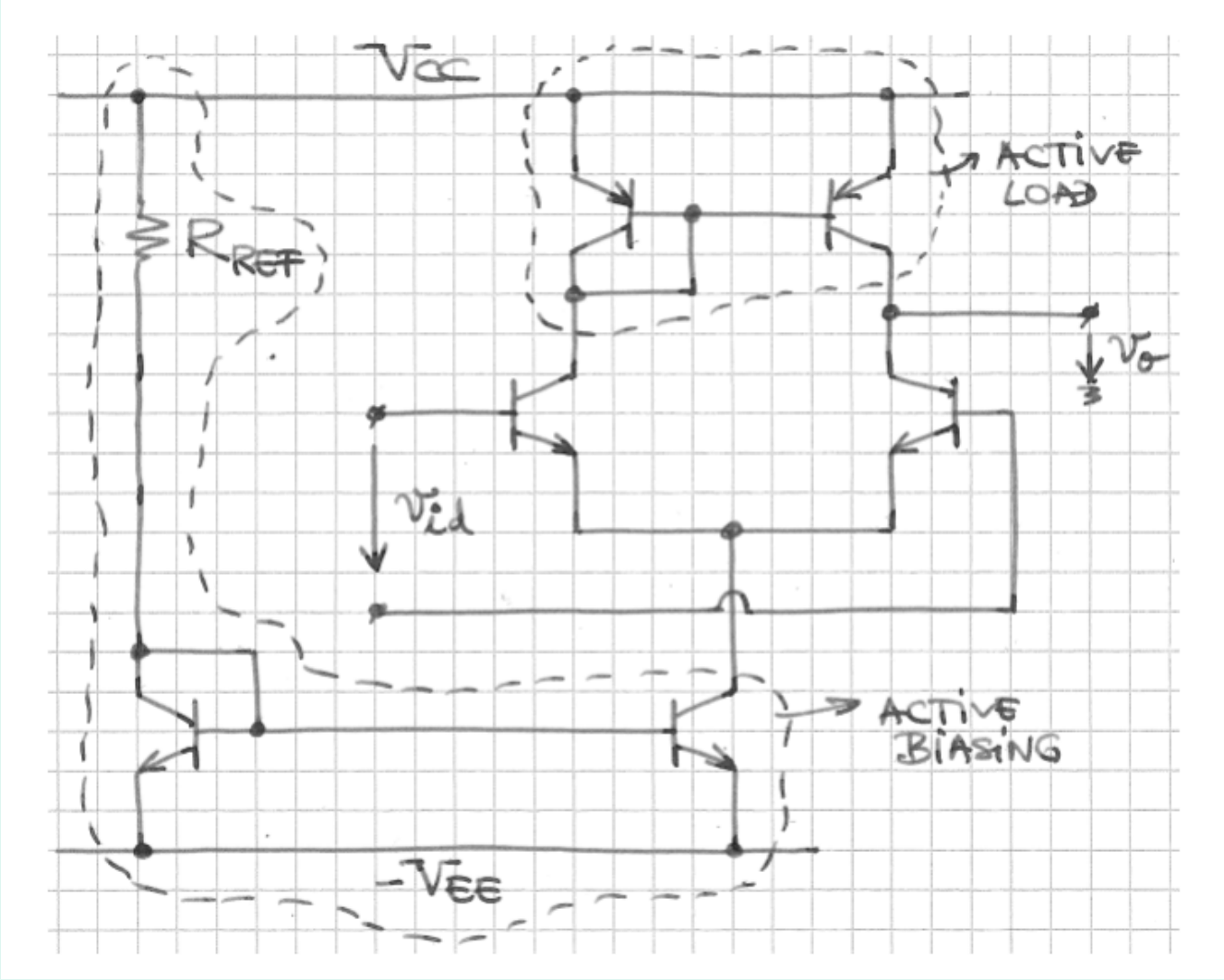
- The bypass capacitors used in the previous single stage transistor amplifiers had a detrimental effect regarding the LF response
- Differential amplifier - able to be DC-coupled (no additional bypass capacitors)



Basic building block for ICs - the operation relies on the very good matching L-R sections (symmetry is essential)

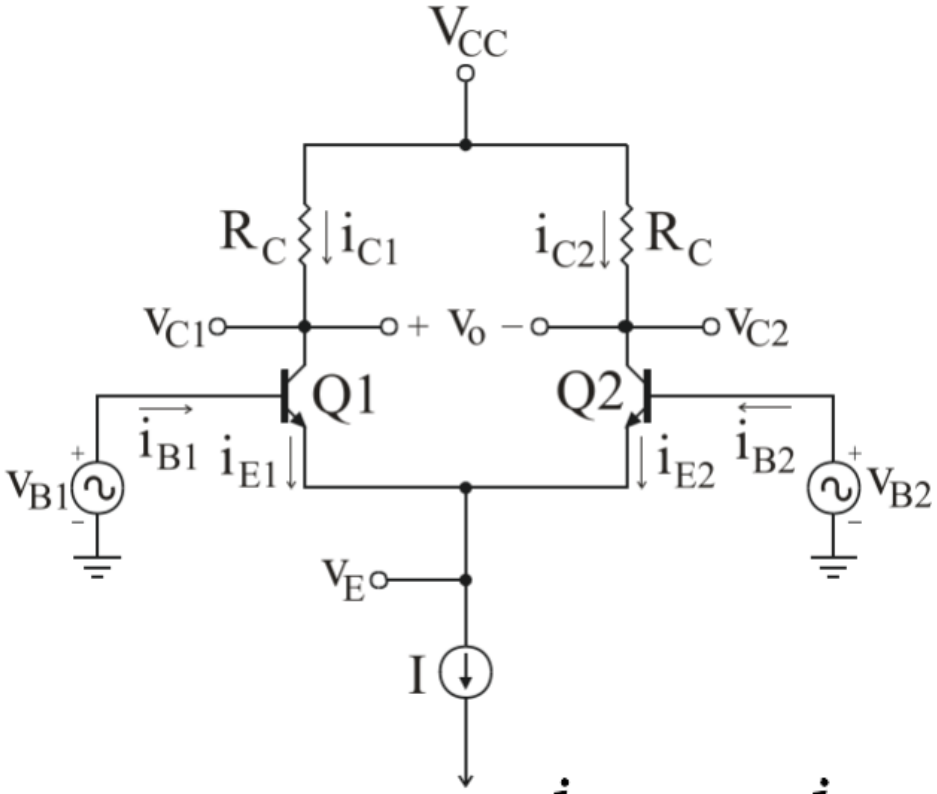
Typical implementation as opamp block

- in IC: active load active biasing (current source)



Basic (large signal) analysis

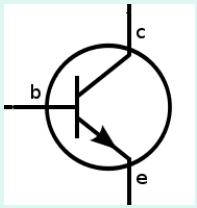
- We assume we have identical transistors



$$v_{B1} = v_{B2} \Rightarrow v_{BE1} = v_{BE2} \Rightarrow \begin{cases} i_{E1} = i_{E2} = \dfrac{I}{2} \\ i_{C1} = i_{C2} = \alpha \dfrac{I}{2} \end{cases}$$

$$i_{E1} = \frac{I_S}{\alpha} e^{(v_{B1} - v_E)/V_T}, i_{E2} = \frac{I_S}{\alpha} e^{(v_{B2} - v_E)/V_T}$$

$$\frac{i_{E1}}{I} = \frac{i_{E1}}{(i_{E1} + i_{E2})} = \frac{1}{\left(1 + \dfrac{i_{E2}}{i_{E1}}\right)} = \frac{1}{\left[1 + e^{(v_{B2} - v_{B1})/V_T}\right]}$$

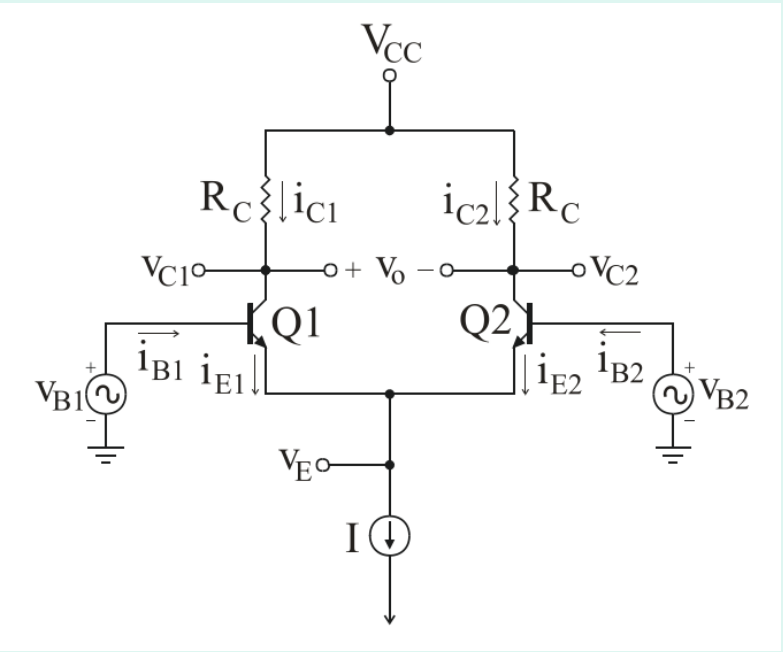


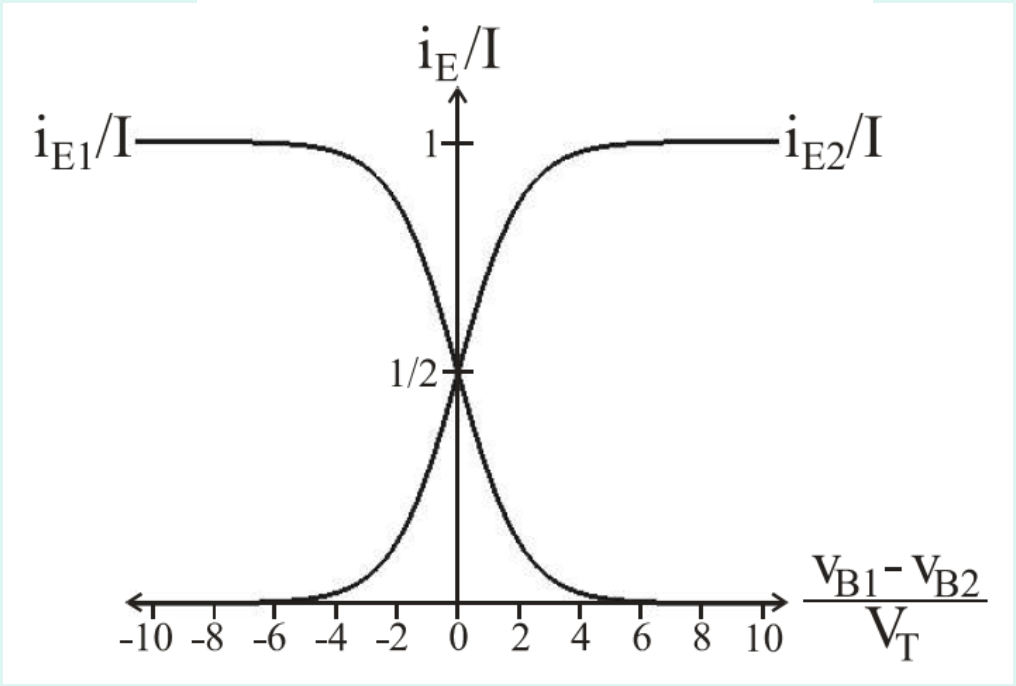
Basic analysis (2)

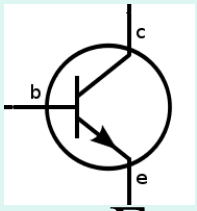
- Equivalent transistors

$$i_{E1} = \frac{I}{1 + e^{(v_{B2} - v_{B1})/V_T}}$$

$$i_{E2} = \frac{I}{1 + e^{(v_{B1} - v_{B2})/V_T}}$$







Signal decomposition

- For arbitrary input voltage v_{B1}, v_{B2}, we can decompose the signals into a common-mode and differential voltage components
- This is useful for separately analyzing the **common-mode gain** A_c and the differential-mode gain (**differential gain**) A_d

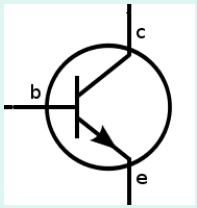
$$\begin{cases} v_{InC} = \dfrac{v_{B1} + v_{B2}}{2} \\ v_{InD} = v_{B1} - v_{B2} \end{cases} v \Leftrightarrow \begin{cases} v_{B1} = v_{InC} + \dfrac{v_{InD}}{2} \\ v_{B2} = v_{InC} - \dfrac{v_{InD}}{2} \end{cases}$$

For small signal analysis, we can define the common-mode rejection ratio (CMMR) as the ratio between A_d and A_c

$$CMMR = \frac{A_d}{A_c} \Leftrightarrow CMMR_{dB} = 20\log\frac{A_d}{A_c}$$

$$\text{Differential gain} : A_d = \frac{v_o}{v_{id}}$$

$$\text{Common-mode gain} : A_c = \frac{v_o}{v_{ic}}$$

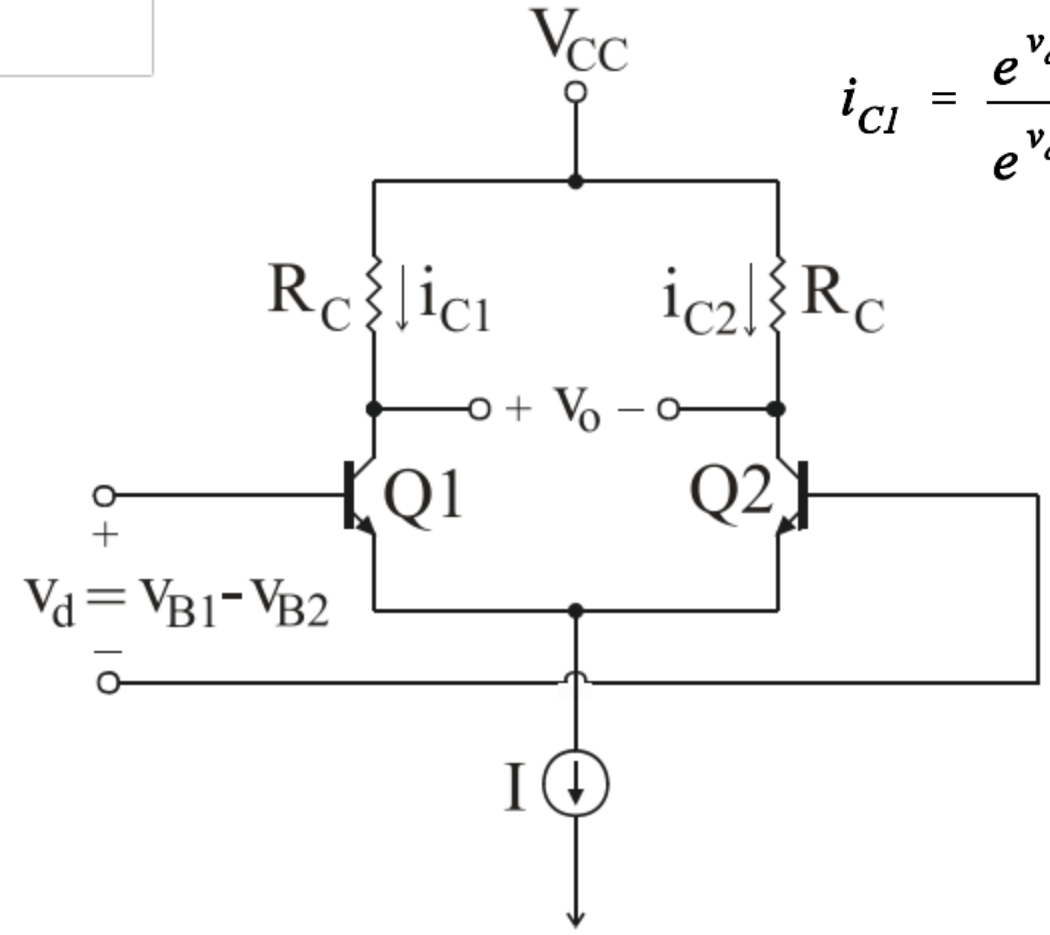


Small signal operation

- The differential voltage:

$$|v_d| = |v_{B1} - v_{B2}| \ll 2V_T$$

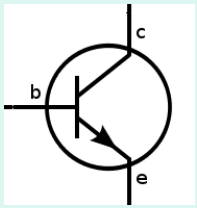
$$i_{C1} = \alpha i_{E1} = \frac{\alpha I}{1 + e^{-v_d/V_T}}$$



$$i_{C1} = \frac{e^{v_d/2V_T}}{e^{v_d/2V_T}} \times \frac{\alpha I}{1 + e^{-v_d/V_T}} = \frac{\alpha I e^{v_d/2V_T}}{e^{v_d/2V_T} + e^{-v_d/2V_T}}$$

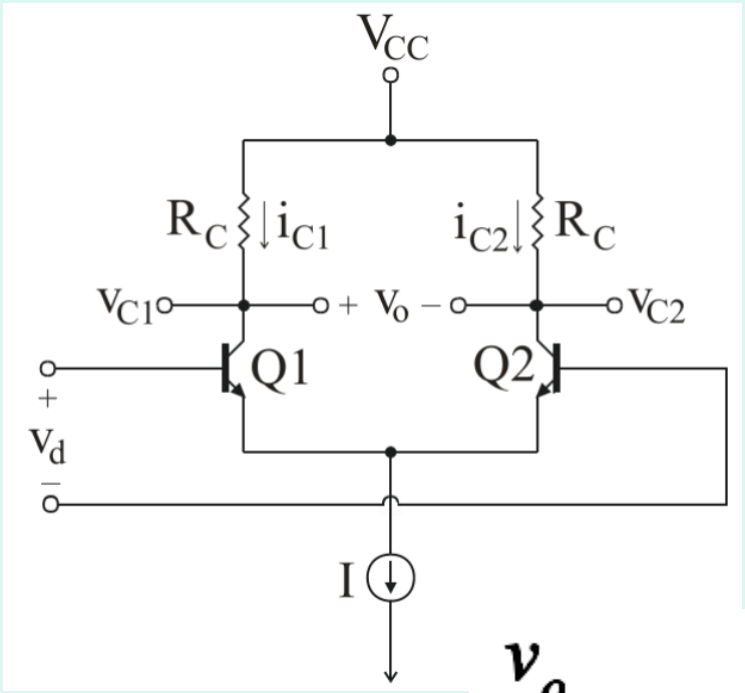
$$i_{C1} \approx \frac{\alpha I \left(1 + \frac{v_d}{2V_T}\right)}{1 + \frac{v_d}{2V_T} + 1 - \frac{v_d}{2V_T}} = \frac{\alpha I}{2}\left(1 + \frac{v_d}{2V_T}\right)$$

$$i_{C2} \approx \frac{\alpha I \left(1 - \frac{v_d}{2V_T}\right)}{1 - \frac{v_d}{2V_T} + 1 + \frac{v_d}{2V_T}} = \frac{\alpha I}{2}\left(1 - \frac{v_d}{2V_T}\right)$$



Differential voltage gain

- We assume no input common-mode voltage => v_d is evenly distributed, $\pm v_d/2$ across each transistor



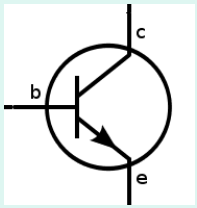
$$i_C = \frac{\alpha I}{2} \pm \frac{\alpha I}{2V_T}\frac{v_d}{2} = I_C \pm g_m \frac{v_d}{2}$$

$$g_m = \frac{\alpha I}{2V_T} \qquad i_c = g_m \frac{v_d}{2}$$

$$v_{C1} = V_{CC} - I_C R_C - g_m R_C \frac{v_d}{2}$$

$$v_{C2} = V_{CC} - I_C R_C + g_m R_C \frac{v_d}{2}$$

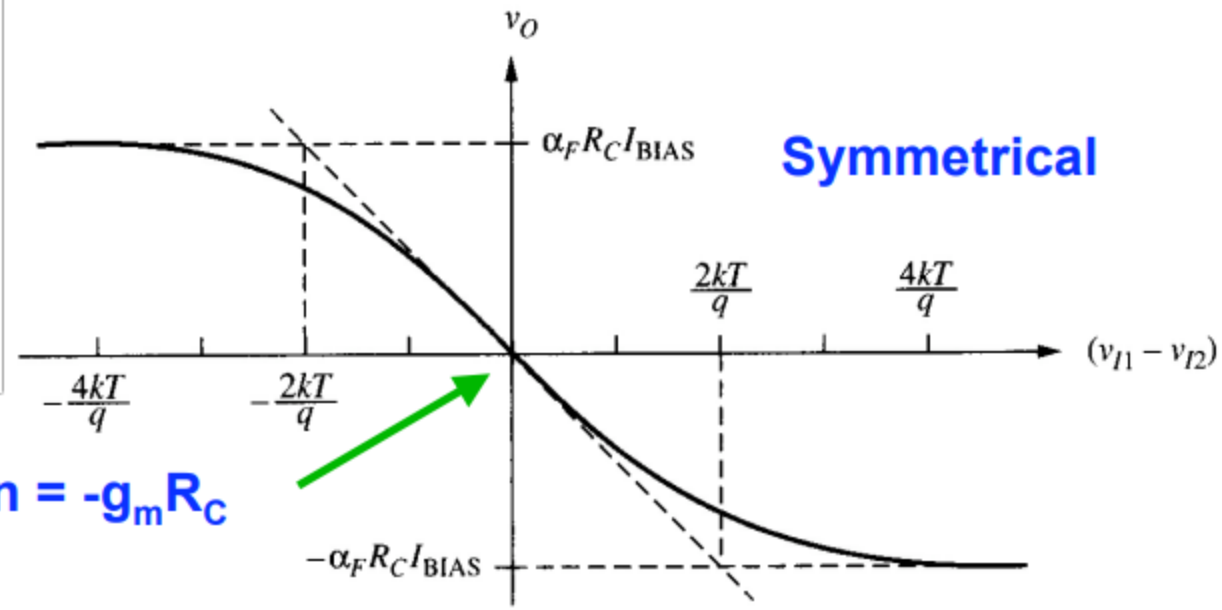
$$\frac{v_o}{v_d} = -g_m R_C$$



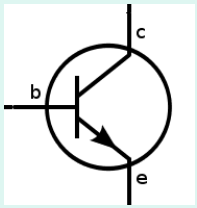
Differential voltage gain

- Only the difference between inputs matters

$$v_O = -\alpha R_C I_B \tanh\left(\frac{v_{B1} - v_{B2}}{2V_T}\right)$$

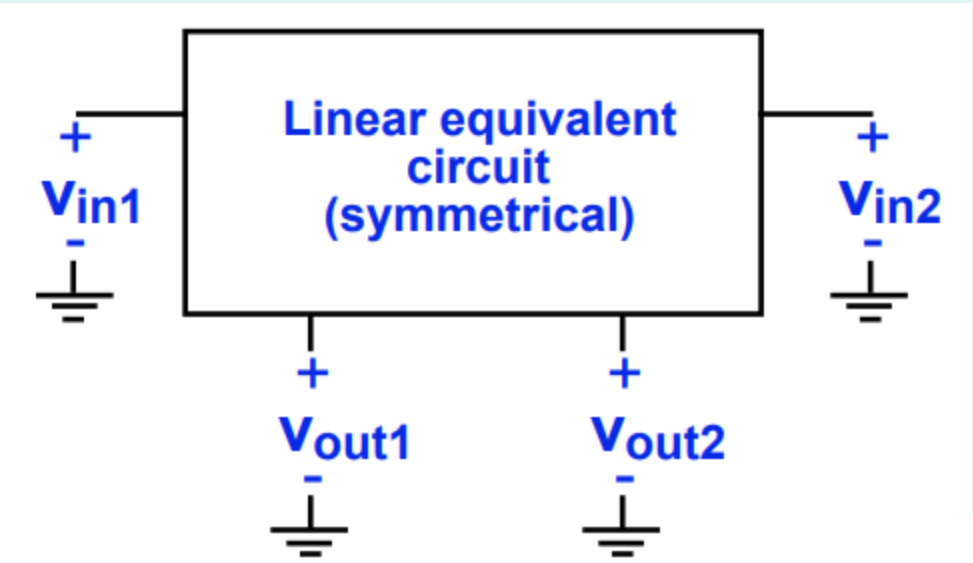


Slope around origin = $-g_m R_C$

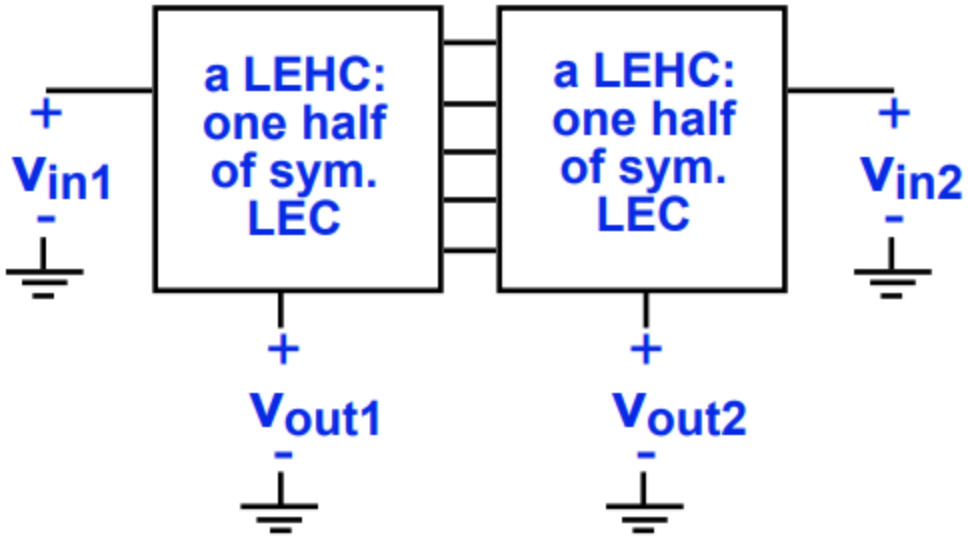


Differential amplifier analysis

- Exploit symmetry and superposition

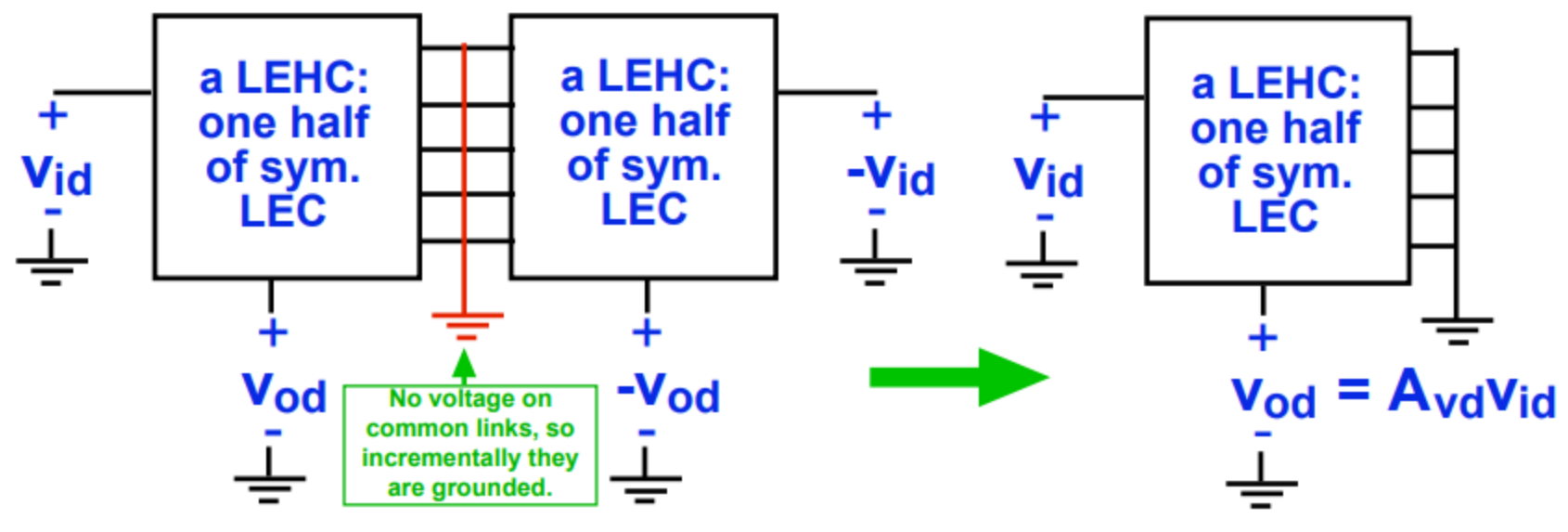


(Source: MIT OCW)



Differential amplifier analysis (2)

- antisymmetric inputs on B1, B2



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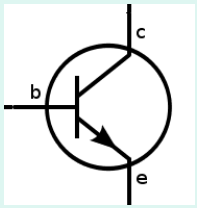
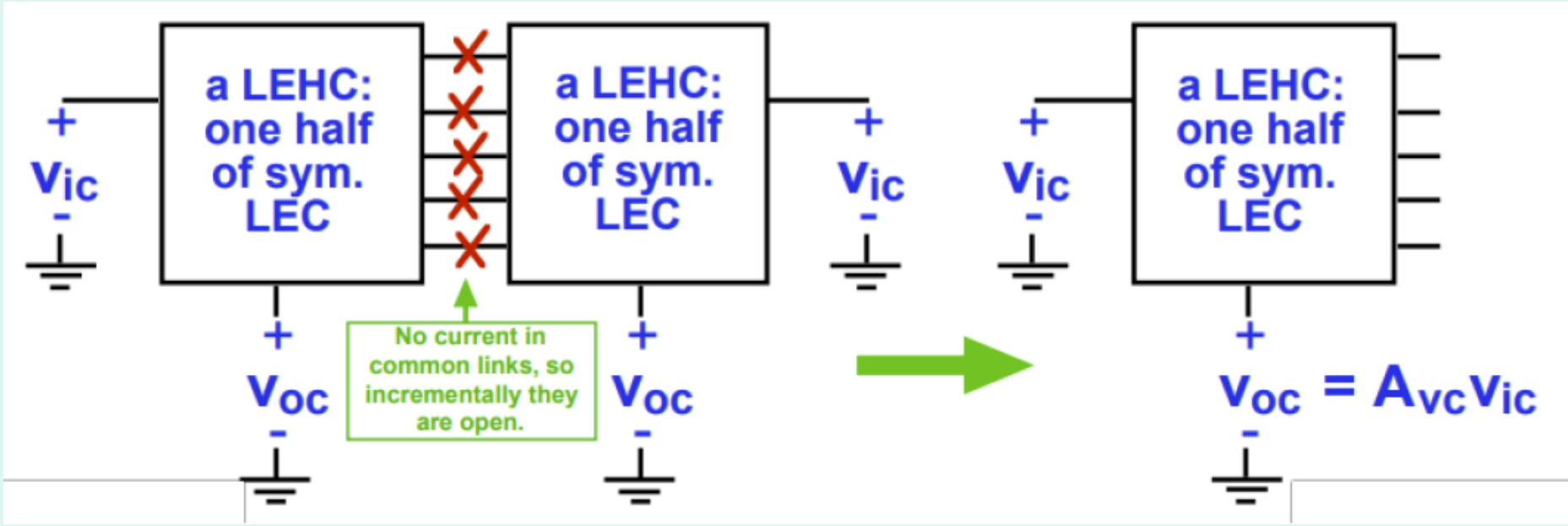


Common-mode voltage inputs

- no current flow on the wire linking the two sections



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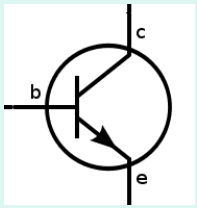
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