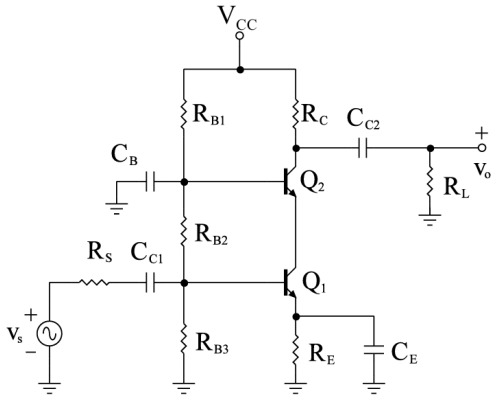
ELEC 301 - Project 2

P1. Multi-transistors amplifier circuits

A cascode amplifier is a two-stage amplifier that combined a common-emitter stage with a common-base stage, to achieve high bandwidth and voltage gain while minimizing the Miller effect.

The following cascode circuit implementation will be used for your design:



Introduce the circuit schematics into your Spice simulator software, using the 2N3904 model for the transistors. The minimum specifications for this amplifier are presented below:

R_{out} (value at midband)	R_{in} (minimum value at midband)[1]	$\|A_M\|$ (minimum value at midband	$\omega_{L,3dB}$ (maximum value for low-frequency cut-in)
2.5kΩ±250Ω	3.5kΩ	50V/V	1200 rad/s

Assume the source resistance Rs=50Ω, that V_{cc}=20V and that the output load resistance R_L=50kΩ.

You are required to design the cascode circuit to meet the above specifications.

Start by calculating the resistor values needed to bias the transistors Q_1 and Q_2. Once you have computed the values of the bias resistors, change them to closest commonly available resistance values. Assuming a large capacitance value for C_B (use C_B=200μF), you should obtain values for all of the other capacitances (use commonly/standard available values in your final design). Compute the small-signal parameters for your circuit.

A. Measure the DC operating point for the cascode amplifier

B. Plot the Bode plots for magnitude and phase and compare your estimates of the locations of ω_{L3dB} and ω_{H3dB} with your calculated values.

C. Using the magnitude Bode plot, pick a midband frequency. Using this frequency for the input voltage, adjust the amplitude of of the input signal until you see that the output signal (viewed in the time domain) is becoming non-linear (you can vary the amplitude of the input signal, at the constant frequency, and plot the voltage transfer curve, the amplitude of v_o vs, v_s).

D. Measure the input impedance of your amplifier at midband (not including the source resistor R_s=50Ω) and compare this with the input impedance that you designed for.

Please include your comparison between measurements and your computations, your interpretations and insights.

P2. The circuit shown below is a common-base followed by a common-collector amplifier stage. It is used as a repeater in an analog 50Ω coaxial cable system. It should be designed so that at midband it has an input impedance R_i=50Ω±5Ω, and a similar output impedance R_o=50Ω±5Ω. Choose 2N3904 for the transistors Q1 and Q2.

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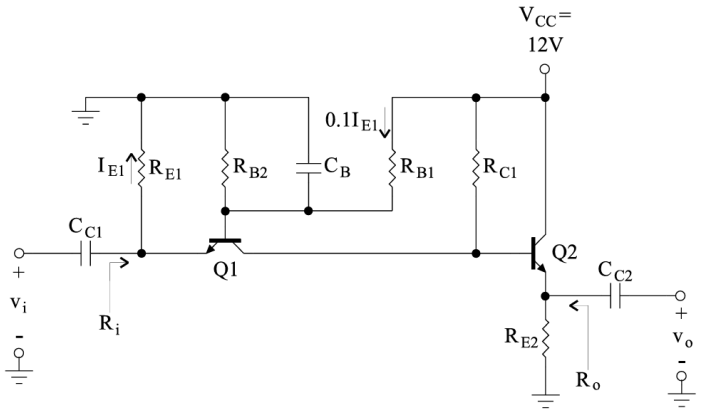
[1] Remark: you may have to add a component to achieve this input resistance; the question is where?

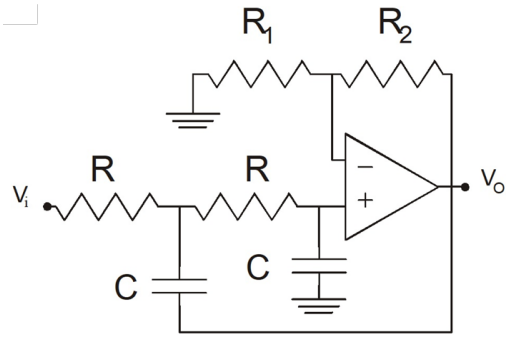


A. Use V_{CC}=12V and the ⅓ rule such that $V_{E1}=V_{CC}/3$ and $I_1=0.1I_{E1}$ (as shown), the design criteria that at midband $R_i=R_o=50\Omega\pm5\Omega$, and that the low-frequency cut-in (the low-frequency 3dB point)occurs at, or below 1000Hz, to obtain design values for R_{E1},R_{C1}, R_{B1}, R_{B2}, R_{E2}, C_{C1}, C_B and C_{C2}. (Hint: assuming that the source has an output impedance of 50Ω and that the repeater will be attached to a 50Ω load, C_{C1} and C_{C2} will both "see" similar resistance values - you can design them together to place the low frequency cut-in at 1000Hz and then design C_B so that it is as small as possible without changing the low frequency cut-in value.
B. Using standard available resistor and capacitor values that are closest to your design values, implement the schematic and measure R_i and R_o at midband. Measure the midband gain $A_M=v_o/v_s$ of your amplifier, without a load resistance and without a source impedance (set R_S=0).
C. Attach a voltage source with an output impedance of 50Ω to the amplifier input and a 50Ω load to the output. Obtain the amplitude and phase Bode plots. Find the low-frequency cut-in and the high-frequency cut-off points. Adjust any low frequency capacitors accordingly to meet the specifications.

In your report, discuss your observations, compare your simulation results with your computation, and discuss any gained insights.

P3. The following circuit is used as a 2nd order low-pass active filter. The transfer function is:

$$H(s)=A_M\frac{1/(RC)^2}{s^2+s\frac{3-A_M}{RC}+\frac{1}{(RC)^2}}$$



Here, A_M is the pass-band gain (and also the DC gain), given by $A_M=1+R_2/R_1$. The transfer function has two poles. By varying AM, you can also control the damping ratio, so that the two poles can be made complex. This low-pass filter can be made into a 2nd order Butterworth filter by placing the poles at specific locations on a circle, centered at the origin in the s-plane.
Using an UA741 as the op-amp and a ±15V power supply, introduce the circuit in your Spice program, setting R and R_1+R_2 equal to 10kΩ
A. Calculate the values of C and A_M that will make the filter a 2nd order low-pass Butterworth filter with a 3dB cut-

off frequency of 10kHz. Plot the magnitude and phase Bode plots of the circuit for the computed values for C and A_M, and show where your poles are located in the s-plane.

B. Keeping $R_1+R_2=10k\Omega$, change R_1 and R_2 slowly to increase A_M. At what value of AM does your circuit start to oscillate? (You can check for oscillations by removing the source and grounding the input). Plot the output v_O when the circuit starts to oscillate and report the R_1, R_2 values at this point. At what value of AM did you expect your circuit to start to oscillate? Why? Measure and report the oscillation frequency. Describe what is happening to your poles in the s-plane when you change AM (I.e. draw the root locus for your active filter and explain the behavior).