THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 401 – Analog CMOS Integrated Circuit Design
Final Exam
Due: Wednesday, December 9th, 2020 at 8:30 am (Pacific Time)

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone except the instructor. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

Good luck!

This exam book including the cover page consists of 16 pages. Please check that you have a complete copy. You may use both sides of each sheet if needed.

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

Surname First name

Student Number

READ THIS

IMPORTANT NOTE:

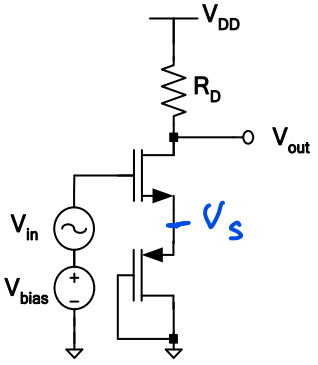
Candidates guilty of any of the following, or similar, dishonest practices shall be liable to disciplinary action:

Speaking or communicating with other candidates or non-candidates regarding the exam questions.

Purposely exposing their solution to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. In the following circuit, assuming the NMOS transistor is operating in the saturation region:
Assume $\lambda_{NMOS} = \lambda_{PMOS} = 0$, $\gamma_{NMOS}= 0.5\ V^{1/2}$, $\gamma_{PMOS}= 0\ V^{1/2}$, $V_{TH0(NMOS)}= 0.4V$, $V_{TH0(PMOS)}= -0.6V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox}=500\ \mu A/V^2$, $(W/L)_{NMOS} = 80$, $(W/L)_{PMOS} = 50$, and $V_{DD}=3V$.



Note: $2\Phi_F = 0.64\ V$

a) Find the required V_{bias} for which the dc bias current of the circuit is 0.5 mA. **[5 marks]**
Note: Please pay attention to γ for the NMOS and the PMOS transistor.

$I = 0.5\ mA$

For the PMOS (which is operating in saturation since it is diode connected), we have:

$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{PMOS}\left(V_{SG} - |V_{th(pmos)}|\right)^2$$

$$0.5 = \frac{1}{2}\,0.5\frac{mA}{V^2}(50)\ V_S - 0 - 0.6)^2 \Rightarrow (V_S - 0.6)^2 = 0.04$$

$$V_S - 0.6 = \pm 0.2 \Rightarrow V_S = 0.8\ V$$

negative not acceptable as $V_{SG} > |V_{th}|$

For NMOS we have:

$$V_{th} = V_{tho} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) = 0.4 + 0.5\left(\sqrt{0.64+0.8} - \sqrt{0.64}\right)$$

$$V_{Th} = 0.4 + 0.5\left(\sqrt{1.44} - \sqrt{0.64}\right)$$

$$V_{Th} = 0.6V$$

Write your answer in this box

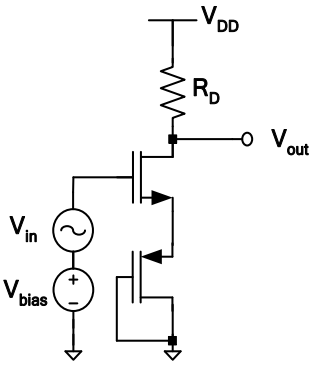
$V_{bias} =$ 1.51 V

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{NMOS}\left(V_{GS} - V_{th}\right)^2$$

$$0.5 = \frac{1}{2}\,1\frac{mA}{V^2}(80)\left(V_{GS} - 0.6\right)^2 \Rightarrow (V_{GS} - 0.6)^2 = \frac{1}{80} \Rightarrow V_{GS} - 0.6 = \pm 0.11$$

$$V_{GS} = 0.71 \Rightarrow V_{bias} - V_S = 0.71 \Rightarrow V_{bias} = 1.51\ V$$

b) If $R_D = 0.2\ k\Omega$, find the small-signal gain of the circuit.
For your convenience the circuit and its parameters are duplicated below:
$\lambda_{NMOS} = \lambda_{PMOS} = 0$, $\gamma_{NMOS} = 0.5\ V^{1/2}$, $\gamma_{PMOS} = 0\ V^{1/2}$, $V_{TH0(NMOS)} = 0.4V$, $V_{TH0(PMOS)} = -0.6V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 500\ \mu A/V^2$, $(W/L)_{NMOS} = 80$, $(W/L)_{PMOS} = 50$, and $V_{DD} = 3V$. **[5 marks]**



Given that $\lambda_{NMOS} = \lambda_{PMOS} \approx 0$

$$A_V = \frac{-R_D}{\frac{1}{g_{m(NMOS)}} + \frac{1}{g_{m(PMOS)}}}$$

$$A_V = \frac{-R_D}{\frac{1}{g_{m(NMOS)}} + (1+\eta)R_S} = \frac{-R_D}{\frac{1}{g_{m(NMOS)}} + (1+\eta)\frac{1}{g_{m(PMOS)}}}$$

$$g_{m(NMOS)} = \frac{2I_D}{eff_{NMOS}} = \frac{2 \times 0.5}{0.11} = 9.09\ mV$$

$$g_{m(PMOS)} = \frac{2I_D}{Veff_{PMOS}} = \frac{2 \times 0.5}{0.2} = 5m$$

$$\eta = \frac{\gamma}{2\sqrt{|2\Phi_F + V_{SB}|}} = \frac{0.5}{2\sqrt{0.64 + 0.8}} = 0.21$$

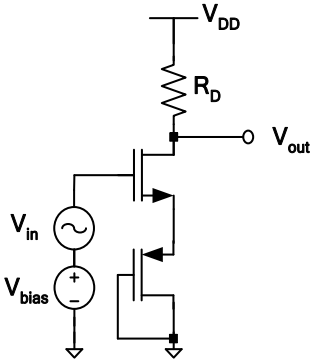
$$A_V = \frac{-0.2}{0.11 + 0.2} = -0.65$$

$$A_V = \frac{-0.2}{0.11 + (1+0.21)0.2} = -0.57\ V/V$$

Write your answer in this box

$A_V =$ ~~-0.65~~ -0.57 V/V

c) Find R_D such that the magnitude of the small-signal gain of the circuit is 10.
For your convenience the circuit and its parameters are duplicated below:
$\lambda_{NMOS} = \lambda_{PMOS} = 0$, $\gamma_{NMOS}= 0.5\ V^{1/2}$, $\gamma_{PMOS}= 0\ V^{1/2}$, $V_{TH0(NMOS)}= 0.4V$, $V_{TH0(PMOS)}= -0.6V$, $\mu_nC_{ox} = 1\ mA/V^2$, $\mu_pC_{ox}=500\ \mu A/V^2$, $(W/L)_{NMOS} = 80$, $(W/L)_{PMOS} = 50$, and $V_{DD}=3V$. **[5 marks]**



$$\left|\frac{-R_D}{\frac{1}{g_{m(NMOS)}}+\frac{1}{g_{m(PMOS)}}}\right| = 10 \Rightarrow \frac{R_D}{0.1+0.2} = 10$$

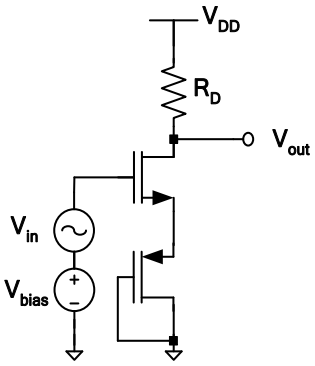
$$R_D = 3.1\ K\Omega$$

Write your answer in this box

R_D= 3.1 KΩ

d) **Designer X** would argue with you that the value of R_D that you have calculated in part (c) is not a good engineering choice and the gain of your circuit would not be as expected. Please state your reason whether or not you agree with **Designer X**? **[5 marks]**

For your convenience the circuit and its parameters are duplicated below:
$\lambda_{NMOS} = \lambda_{PMOS} = 0$, $\gamma_{NMOS}= 0.5\ V^{1/2}$, $\gamma_{PMOS}= 0\ V^{1/2}$, $V_{TH0(NMOS)}= 0.4V$, $V_{TH0(PMOS)}= -0.6V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox}=500\ \mu A/V^2$, $(W/L)_{NMOS} = 80$, $(W/L)_{PMOS} = 50$, and $V_{DD}=3V$.



If $R_D = 3.1k\Omega$

$V_{out} = V_{DD} - R_D I_D = 3 - 3.1 \times 0.5 = 1.45\ V$

For the NMOS we have

$V_{GT} = V_{bias} - V_{out} = 1.51 - 1.45 = 0.06 < V_{th}$ (0.6)

Thus NMOS is in saturation

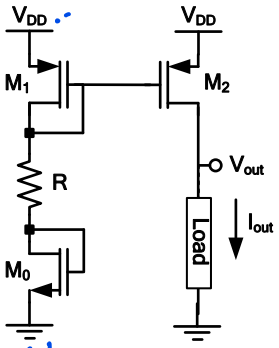
Alternatively, we can say

$V_{DS} = V_{out} - V_S = 1.45 - 0.8 = 0.65 > V_{eff_{NMOS}}$ (0.11)

Therefore, the circuit should work as expected contrary to what Designer X thinks.

2. In the following circuit assume that:
$\lambda_{(NMOS)}=\lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3.3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox}=1$ mA/V^2, and $\mu_p C_{ox}=0.25$ mA/V^2.
Furthermore, assume all transistors have the same size and M_2 is operating in saturation. Given that R = 1.7 kΩ and $I_{out} = 1$ mA

a) Find the aspect ratio of transistor M_0, i.e., $(W/L)_0$? **[15 marks]**
b) What is the maximum voltage of V_{out} for which M_2 remains in saturation region? **[5 marks]**



Since M_1 and M_2 have the same size and are both operating in saturation and there is no channel-length modulation, we have

$I_1 = I_2 = I_{out} = 1$ mA and $I_1 = I_0 \Rightarrow I_1 = I_0 = 1$ mA

For the left branch we have:

$$V_{SG1} + RI_1 + V_{GS0} = V_{DD} \Rightarrow \left(\sqrt{\frac{2I_1}{\mu_p C_{ox}\left(\frac{W}{L}\right)}} + |V_{th2}|\right) + RI_1 + \sqrt{\frac{2I_1}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{th0} = 3.3$$

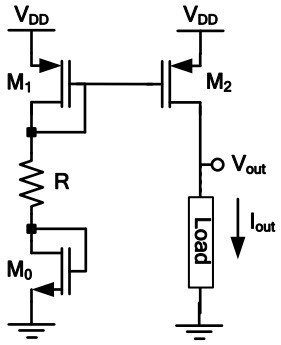
$$\sqrt{\frac{2}{0.25\times\left(\frac{W}{L}\right)}} + 0.5 + 1.7\times 1 + \sqrt{\frac{2}{1\times\left(\frac{W}{L}\right)}} + 0.5 = 3.3$$

$$\sqrt{\frac{2}{\left(\frac{W}{L}\right)}}\left(\sqrt{\frac{1}{0.25}} + 1\right) = 0.6 \Rightarrow \sqrt{\frac{2}{\left(\frac{W}{L}\right)}}(2+1) = 0.6$$

$$\Rightarrow \left(\frac{W}{L}\right) = 50$$

For M_2 we have $1\text{ mA} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{SG2} - |V_{th2}|\right)^2$

For your convenience he circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)}=\lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3.3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox}=1$ mA/V^2, and $\mu_p C_{ox}=0.25$ mA/V^2.
Furthermore, assume all transistors have the same size and M_2 is operating in saturation. Assuming that R = 1.7 kΩ and $I_{out} = 1$ mA



Thus:

$$\left(V_{SG_2}-|V_{th_2}|\right)^2 = \frac{2\times 1}{0.25\times 50} \Rightarrow V_{SG2}-|V_{th2}| = \pm 0.4\ V$$

negative solution not acceptable

$$V_{eff_2} = 0.4\ V$$

$$V_{SD} \geq V_{eff} \Rightarrow V_{DD}-V_{out} \geq 0.4$$

$$V_{out} \leq 3.3 - 0.4 \Rightarrow V_{out} \leq 2.9\ V$$

$$V_{out,max} = 2.9\ V$$

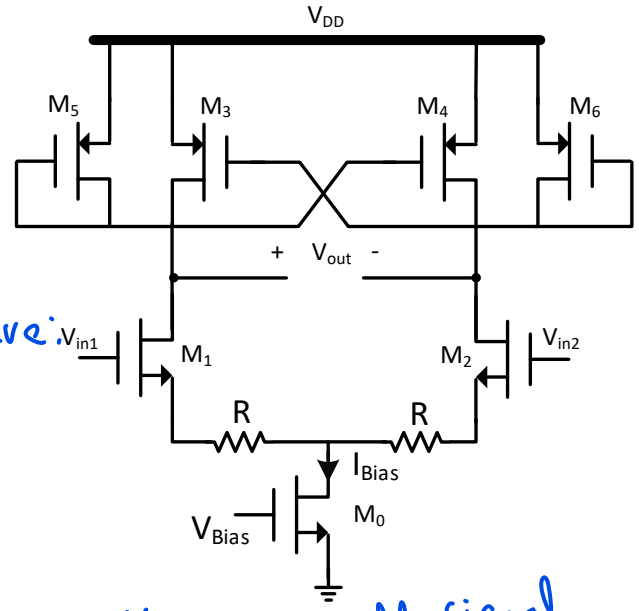
Write your answer in this box	Write your answer in this box
$(W/L)_0$=_____	$V_{out,max}$= _____ V

3. In the following symmetric circuit, assume all transistors are operating in saturation region, $\lambda = 0$, and $\gamma = 0$. **[20 marks]**

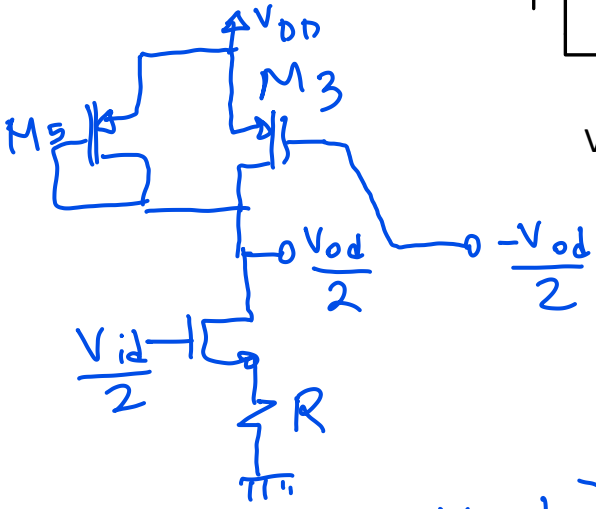
a) Find the small-signal differential voltage gain of the circuit, i.e., $V_{out}/(V_{in1}-V_{in2})$, in terms of transconductances of the relevant transistors and R.

b) What is the small-signal differential voltage gain if $(W/L)_5=2\times(W/L)_3$, $(g_{m1})\times R = 1$, and $(W/L)_1=2\times (W/L)_3$?

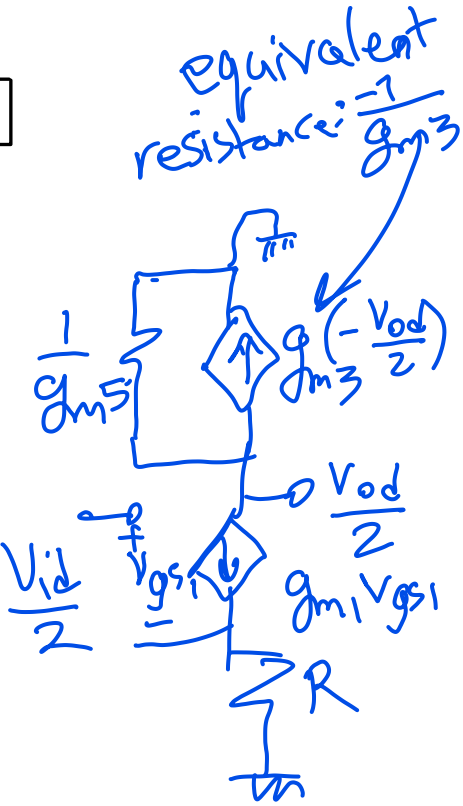
c) Given that M_5 and M_3 have the same effective voltage, find the relationship between $(W/L)_5$ and $(W/L)_3$ so that the maximum small-signal differential gain of the circuit is achieved. What is the value of this maximum gain?



Using half-circuit concept, we have:



small-signal model



$$A_v = \frac{-\left(\frac{1}{g_{m5}} \| \frac{-1}{g_{m3}}\right)}{R + \frac{1}{g_{m1}}} = \frac{\frac{-g_{m1}}{g_{m5}-g_{m3}}}{1 + g_{m1}R}$$

$$g_{m5} = \mu_p C_{ox} \left(\frac{W}{L}\right)_5 (V_{SG5} - |V_{thp}|)$$

$$g_{m3} = \mu_p C_{ox} \left(\frac{W}{L}\right)_3 (V_{SG3} - |V_{thp}|)$$

From DC standpoint

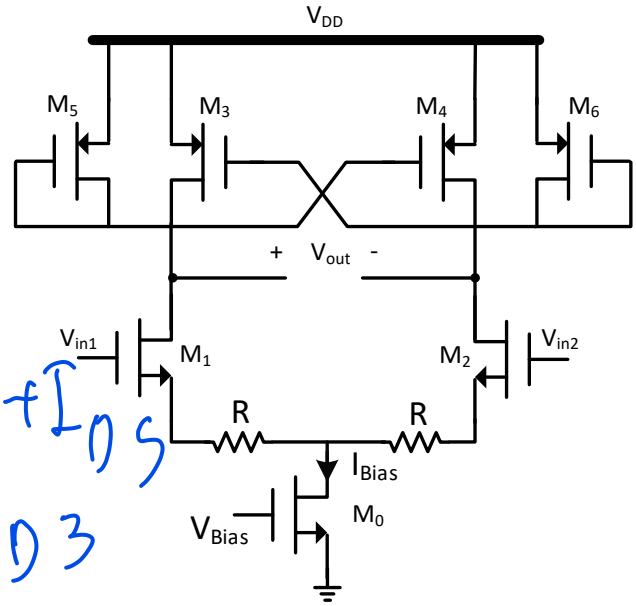
$$V_{SG5} = V_{SG3}$$

Thus if $\left(\frac{W}{L}\right)_5 = 2\left(\frac{W}{L}\right)_3 \Rightarrow g_{m5} = 2g_{m3}$

For your convenience the circuit and the assumptions and circuit parameters are duplicated below:

Also

$I_{D5} = 2I_{D3}$



$I_{D1} = I_{D3} + I_{D5}$

$I_{D1} = 3I_{D3}$

If $\left(\frac{W}{L}\right)_1 = 2\left(\frac{W}{L}\right)_3$

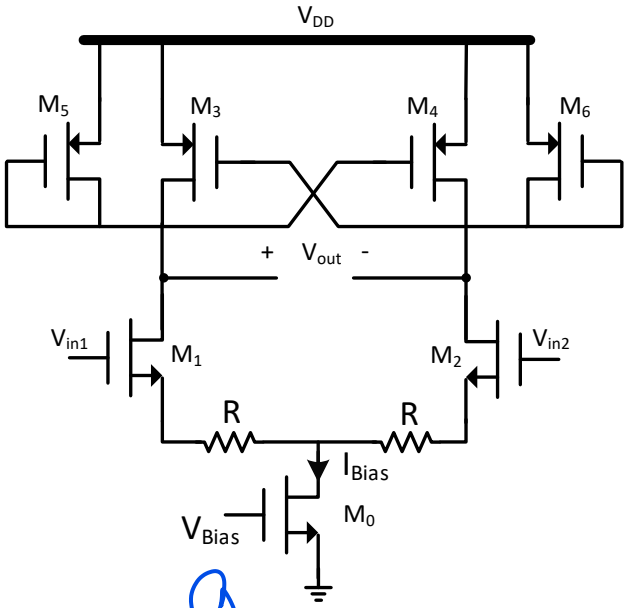
$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}}$$

$$g_{m3} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_3 I_{D3}}$$

$$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\mu_n}{\mu_p}\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3}\frac{I_{D1}}{I_{D3}}}$$

$$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\mu_n}{\mu_p} 2 \times 3} = \sqrt{6\frac{\mu_n}{\mu_p}}$$

For your convenience the circuit and the assumptions and circuit parameters are duplicated below:



$$A_v = \frac{-\frac{g_{m1}}{g_{m5}-g_{m3}}}{1+g_{m1}R} = \frac{-\frac{g_{m1}}{2g_{m3}-g_{m3}}}{1+1}$$

$$A_v = -\frac{g_{m1}}{2g_{m3}} = \frac{-1}{2}\sqrt{\frac{6\mu_n}{\mu_p}}$$

Expression for Differential gain = _____

Value of differential gain = _____

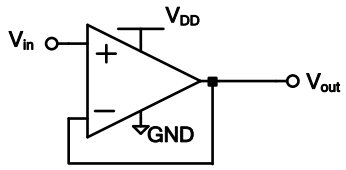
Relation between $(W/L)_5$ and $(W/L)_3$ for maximum gain = _____

Maximum gain = _____

Maximum $|A_v|$ is when $g_{m5}=g_{m3}$ and is ∞ $\Rightarrow \mu_p C_{ox}\left(\frac{W}{L}\right)_5 V_{effs} = \mu_p C_{ox}\left(\frac{W}{L}\right)_3 V_{effs}$

$\Rightarrow \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_3$

4. Find the required phase margin for an op-amp such that when it is configured in a unity-gain feedback (shown below), the magnitude frequency response of the closed-loop system shows no peaking (i.e., 0% peaking) at the gain crossover frequency (i.e., at the frequency where the magnitude of the open-loop gain of the opamp is 1)? **[20 marks]**



closed-loop gain: $\frac{A(j\omega)}{1+A(j\omega)}$

$|A(j\omega_t)| = 1$

no peaking @ ω_t

$$\left|\frac{A(j\omega_t)}{1+A(j\omega_t)}\right| = 1 \Rightarrow |A(j\omega_t)| = |1+A(j\omega_t)| \quad (1)$$

$$|A(j\omega_t)| = 1 = |A(j\omega_t)|\cos\theta + j|A(j\omega_t)|\sin\theta$$

$$= \cos\theta + j\sin\theta$$

from (1): $1 = |1+\cos\theta + j\sin\theta|$

$$1 = \sqrt{(1+\cos\theta)^2 + \sin^2\theta}$$

$$1 = (1+\cos\theta)^2 + \sin^2\theta = 1 + 2\cos\theta + \underbrace{\cos^2\theta + \sin^2\theta}_{1}$$

$$1 = 2 + 2\cos\theta \Rightarrow \cos\theta = \frac{-1}{2} \Rightarrow \theta = -120^\circ$$

$$PM = \theta + 180^\circ = 60^\circ$$

5. Design a two-stage op-amp based on the topology shown below with the following design specifications (Note that the gate of M_{10} is also connected to the gate of M_3):

- V_{DD}=1 V
- Total power consumption of 1 mW
- Total gain of 8000
- L=0.2 µm for all the devices
- W_9=W_{10}
- W_8=4W_7
- R=1 kΩ

$P = 1mW$, $V_{DD} = 1V$

$W_9 = W_{10} \Rightarrow I_9 = I_{10} = 0.1$

$I_t = \frac{P}{V_{DD}} = 1mA$ ← total current

$I_t = I_0 + I_5 + I_9 + I_{10}$

$1mA = 2I_0 + 0.1 + 0.1 \Rightarrow I_0 = I_5 = 0.4mA$

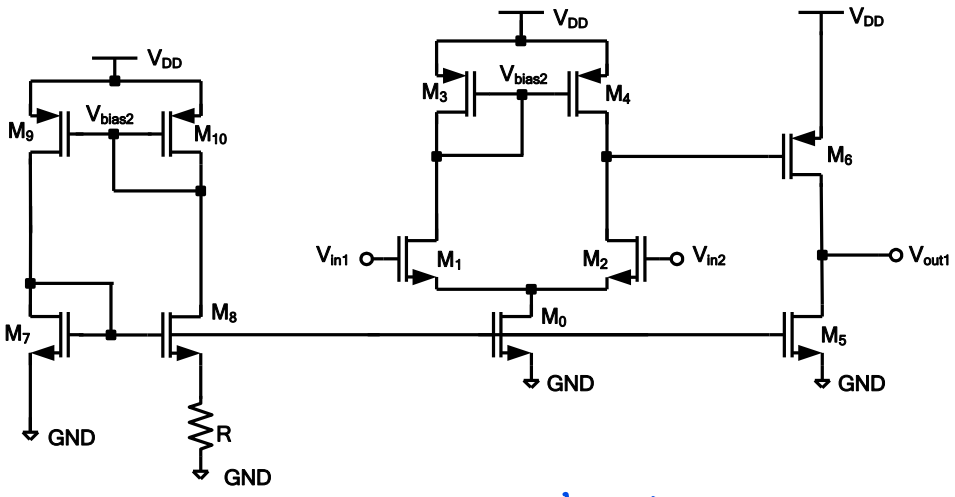
Use the following assumptions for your design

- The differential stage is symmetric
- The bias currents of the first and second stage are equal (i.e., I_0=I_5) and I_{10} is 0.1 mA.
- The magnitude of overdrive voltages of M_4, M_5, and M_6 are equal

$I_4 = \frac{1}{2} I_0 = 0.2mA$

The technology parameters are:
$\lambda_{(NMOS)}$=$\lambda_{(PMOS)}$=0.05V^{-1}, $\gamma = 0$, V_{DD}=1V, $V_{TH(NMOS)}$=|$V_{TH(PMOS)}$|=0.4V, $\mu_n C_{ox}$=1 mA/V^2, $\mu_p C_{ox}$=0.5 mA/V^2.

Note: Use the parameter λ only for calculating the r_o of the transistors. **<u>Do not</u>** use λ (that is assume λ = 0) in any other calculation including for calculating bias currents.



$r_{o2} = \frac{1}{\lambda_p I_4} = 100k\Omega$

$r_{o4} = \frac{1}{\lambda_n I_4} = 100k\Omega$

$r_{o5} = \frac{1}{\lambda_p I_5} = 50k\Omega$

$r_{o6} = \frac{1}{\lambda_n I_5} = 50k\Omega$

$|A_v| = g_{m1}(r_{o2} \| r_{o4})\, g_{m6}(r_{o5} \| r_{o6}) = g_{m1}(100 \| 100)\, g_{m6}(50 \| 50) < 8000$

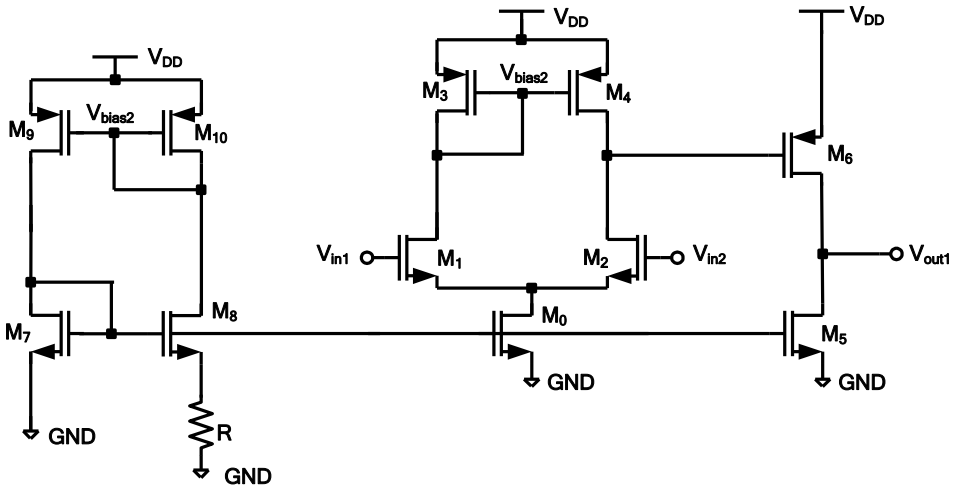
a) Find the widths of all transistors (namely, W_0,W_1, W_2, W_3, W_4, W_5, W_6, W_7, W_8, W_9, W_{10}). **[12 marks]**

b) What is the maximum peak-to-peak swing of the output signal? **[4 marks]**

c) Assuming that we have the maximum output swing (output is a symmetrical sinusoidal signal), what should be the output common-mode level (i.e., the DC level of the output signal for maximum swing)? **[4 marks]**

$g_{m1} \times g_{m6} = \frac{8000}{50 \times 25} = 6.4 (m\Omega)^2$

For your convenience the circuit diagram and transistor parameters is replicated here:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.05V^{-1}$, $\gamma = 0$, $V_{DD}=1V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_nC_{ox}=1$ mA/V^2, $\mu_pC_{ox}=0.5$ mA/V^2.



For the bias circuit we have:

$$I_{10}=\frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_7}\frac{1}{R^2}\left(1-\frac{1}{\sqrt{\left(\frac{W}{L}\right)_8/\left(\frac{W}{L}\right)_2}}\right)^2$$

$$0.1\,mA=\frac{2}{1\left(\frac{W}{L}\right)_7}\times\frac{1}{1^2}\left(1-\frac{1}{\sqrt{4}}\right)^2$$

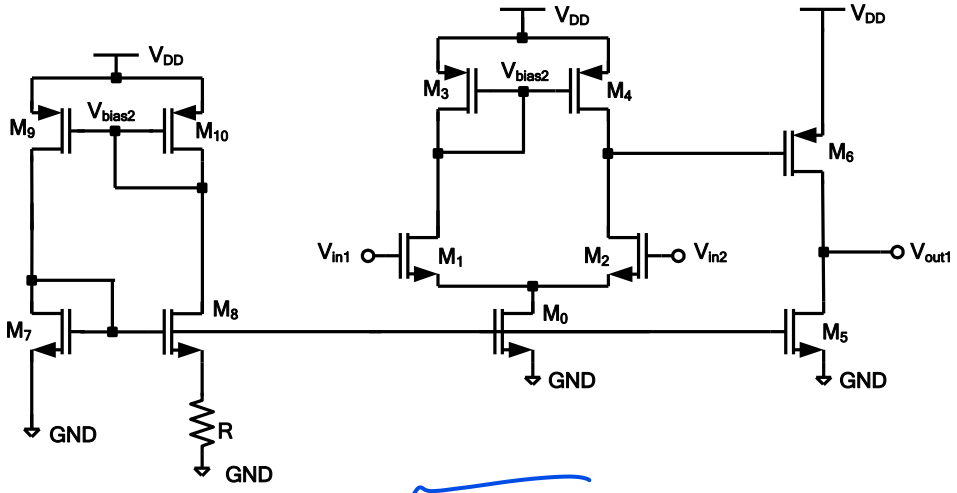
$$0.1=\frac{2}{\left(\frac{W}{L}\right)_7}\frac{1}{4}\Rightarrow\left(\frac{W}{L}\right)_7=5$$

$$W_7=5L_7=5\times0.2=1\,\mu m$$

$$W_8=4W_7=4\,\mu m$$

$$V_{GS7}=\sqrt{\frac{2I_{10}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_7}}+V_{th7}=\sqrt{\frac{2\times0.1}{1\times5}}+0.4=0.6V$$

For your convenience the circuit diagram and transistor parameters is replicated here:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.05V^{-1}$, $\gamma = 0$, $V_{DD}=1V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_nC_{ox}=1$ mA/V^2, $\mu_pC_{ox}=0.5$ mA/V^2.



$V_{GS7}=V_{GS0}=0.6V \Rightarrow V_{GS0}=\sqrt{\frac{2I_0}{\mu_nC_{ox}(\frac{W}{L})_0}}+V_{th0} \Rightarrow 0.6=\sqrt{\frac{2\times0.4}{1\times(\frac{W}{L})_0}}+0.4$

$(\frac{W}{L})_0=20 \Rightarrow W_0=20\times0.2=4\mu m$

$V_{GS7}=V_{GS5}=0.6V \Rightarrow V_{GS5}=\sqrt{\frac{2I_5}{\mu_nC_{ox}(\frac{W}{L})_5}}+V_{th5} \Rightarrow (\frac{W}{L})_5=20 \Rightarrow W_5=4\mu m$

$V_{eff5}=V_{eff6}=0.2 \Rightarrow V_{eff6}=\sqrt{\frac{2I_6}{\mu_pC_{ox}(\frac{W}{L})_6}}$

$0.2=\sqrt{\frac{2\times0.4}{0.5\times(\frac{W}{L})_6}} \Rightarrow (\frac{W}{L})_6=40 \Rightarrow W_6=8\mu m$

W_0 = 4 µm, W_1= 1.28 µm, W_2= 1.28 µm, W_3= 4 µm,

W_4= 4 µm, W_5= 4 µm, W_6= 8 µm, W_7= 1 µm,

W_8= 4 µm, W_9= 2 µm, W_{10}= 2 µm,

Maximum peak-to-peak output swing=_____V, Output DC level=_____

$$V_{eff6}=0.2V \Rightarrow g_{m6}=\frac{2I_{D6}}{V_{eff6}}=\frac{2\times0.4}{0.2}=4\ mS$$

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$$g_{m1}\times g_{m6}=6.4 \Rightarrow g_{m1}=\frac{6.4}{4}=1.6mS=\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_1}$$

$$1.6=\sqrt{2\times1\times\left(\frac{W}{L}\right)_1\times0.2} \Rightarrow \left(\frac{W}{L}\right)_1=6.4 \Rightarrow W_1=1.28$$

$$\Rightarrow W_2=1.28\mu m$$

$$V_{eff4}=V_{eff6}=0.2V \Rightarrow 0.2=\sqrt{\frac{2I_4}{\mu_p C_{ox}\left(\frac{W}{L}\right)_4}}$$

$$\Rightarrow W_4=4\mu$$

$$V_{SG4}=V_{SG10} \Rightarrow V_{eff4}=V_{eff10}=0.2V \Rightarrow 0.2=\sqrt{\frac{2I_{10}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{10}}}$$

$$\Rightarrow W_{10}=2\mu m \Rightarrow W_9=W_{10}=2\mu m$$

$$V_{o\,p\text{-}p}=V_{DD}-V_{eff6}-V_{effs}=1-0.2-0.2$$
$$=0.6V$$

Since $V_{effs}=V_{eff6}$ for maximum output swing the DC level of the output should be

$$\frac{V_{DD}}{2}=0.5V$$