THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 401 – Analog CMOS Integrated Circuit Design
Final Exam
Due: Monday, December 8th, 2025 at 11:59 pm (Pacific Time)

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone before the due date shown above. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

Good luck!

This exam has 5 questions and including the cover page consists of 16 pages.

Surname First name

Student Number

Student Number

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

READ THIS

Candidates who commit to any of the following, or similar, dishonest practices shall be liable to disciplinary action:

Speaking or communicating with other candidates or non-candidates regarding the exam questions.

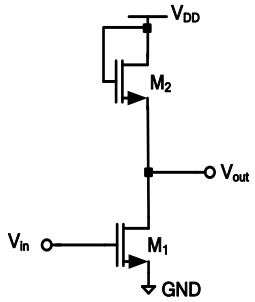
Purposely exposing their solution to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. Design a common-source amplifier with a diode-connected load based on the schematic shown below with the following design specifications:

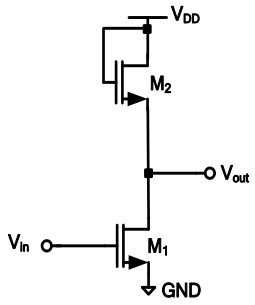
- Transistor M_1 is in saturation
- The minimum possible output voltage to keep M1 in saturation is 0.25V
- Total DC power consumption of the amplifier is 3mW
- Both transistors have L=0.5μm
- DC level of the output is 1.5 V

The technology parameters are:
λ(NMOS) = 0, γ = 0, V_{DD}=3V, V_{TH}(NMOS) = 0.5V, $\mu_n C_{ox}$=0.5 mA/V^2



Find the following values:
a) Width of the transistors, i.e., W_1 and W_2 **[5 marks]**,
b) DC level of the input **[5 marks]**,
c) Small-signal gain **[5 marks]**.
d) Maximum symmetric output signal swing while both transistors stay in saturation **[5 marks]**.

For your convenience the circuit and its parameters are duplicated below:
The technology parameters are:
λ(NMOS) = 0, γ = 0, V_{DD}=3V, V_{TH}(NMOS) = 0.5V, $\mu_n C_{ox}$=0.5 mA/V^2



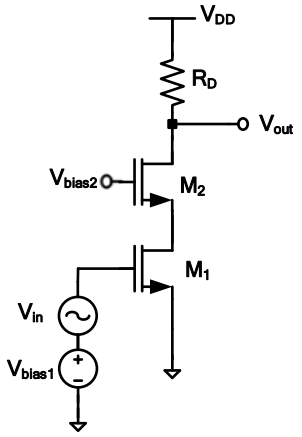
DC level of output =_____ V, W_1=_____μm, W_2=_____μm,

small-signal gain A_V=_____V/V,

maximum output swing (for a symmetric swing) =_____V,

2. In the following cascode circuit, V_{bias1} and V_{bias2} are DC voltage sources used for biasing transistors M_1 and M_2 respectively and V_{in} is a small-signal source. Assume that both transistors M1 and M2 are ideal transistors with no channel-length modulation and no body effect, that is, that is, λ and γ are zero. Furthermore, assume that:

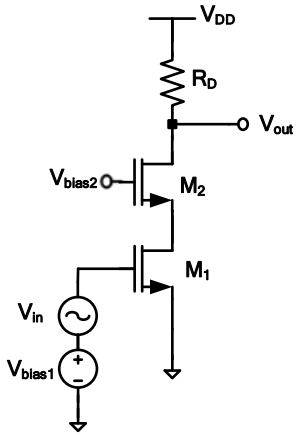
$\mu_n C_{ox}$=1 mA/V^2, V_{TH}=0.5 V, $(W/L)_1$=50, $(W/L)_2$=100, R_D=1 kΩ, and V_{DD}=3 V.



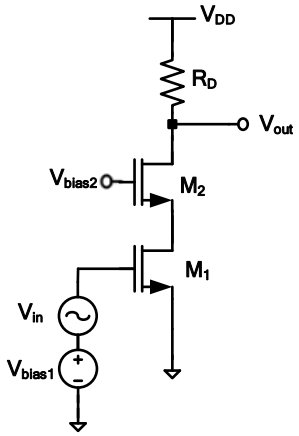
Assuming that M_1 is biased at the edge of the saturation region (that is, at the boundary between saturation and triode regions) and the small-signal gain of the circuit is -10 V/V, that is, $V_{out}/V_{in} = -10$ V/V:

a) Find V_{bias1} **[5 marks].**
b) If we assume M_2 is operating in saturation, find V_{bias2}. **[5 marks]**
c) Given V_{bias2} that you have found in part b, is M_2 indeed in saturation? Why? **[5 marks]**
d) What is the DC power consumption of circuit (that is, the power that is drawn from V_{DD})? **[5 marks]**

For your convenience the circuit diagram and circuit and transistor parameters is replicated here: $\mu_n C_{ox}$=1 mA/V^2, V_{TH}=0.5 V, $(W/L)_1$=50, $(W/L)_2$=100, R_D=1 kΩ, and V_{DD}=3 V, λ and γ are zero.



For your convenience the circuit diagram and circuit and transistor parameters is replicated here: $\mu_n C_{ox}$=1 mA/V^2, V_{TH}=0.5 V, $(W/L)_1$=50, $(W/L)_2$=100, R_D=1 kΩ, and V_{DD}=3 V, λ and γ are zero..

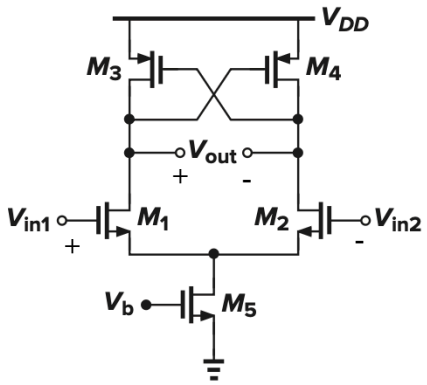


V_{bias1}= _____V, V_{bias2}=_____V, P_{DC} =_____mW

Is M_2 in saturation? Why? _____

3. In the following symmetric circuit, assume all transistors are operating in saturation region, and are ideal and they have neither channel-length modulation nor body effect.

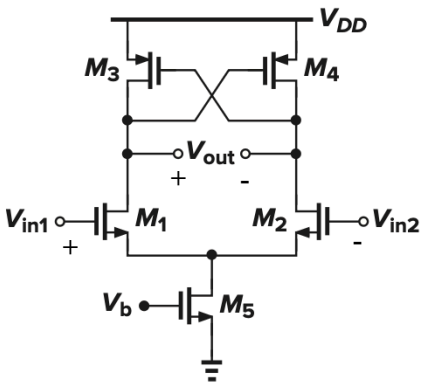
Assume that: $\lambda_{(NMOS)}=\lambda_{(PMOS)}=0V^{-1}$, $\gamma = 0$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_n C_{ox}=0.5\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.



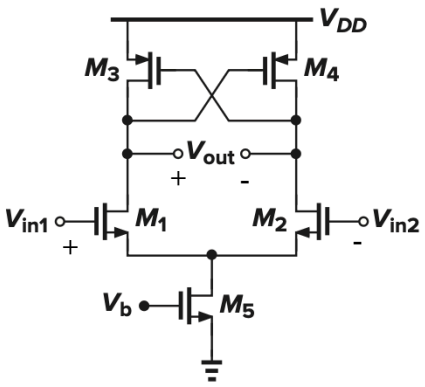
a) Find the small-signal differential voltage gain of the circuit, that is, $V_{out}/(Vi_{n1}-V_{in2,})$, in terms of transconductances of the relevant transistors. **[15 marks]**

b) If the aspect ratio, that is (W/L) of the NMOS transistors is twice that of the PMOS transistors, that is, (W/L)NMOS=2(W?Lwhat is the numerical value of the small-signal differential voltage gain of the circuit. **[5 marks]**

For your convenience the circuit diagram and transistor parameters is replicated here:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0V^{-1}$, $\gamma = 0$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_n C_{ox}=0.5\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$. $(W/L)_{NMOS}=2(W/L)_{PMOS}$.



For your convenience the circuit diagram and transistor parameters is replicated here:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0V^{-1}$, $\gamma = 0$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_n C_{ox}=0.5\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.
$(W/L)_{NMOS}=2(W/L)_{PMOS}$.



Differential gain in terms of relevant transconductance: _____

Numerical value of the differential gain= _____

4. Design a two-stage op amp based on the topology shown below with the following design specifications (note that the horizontal wire at the bottom of the circuit connects the gates of M_0, M_5 and M_6 to V_{bias1}. That wire is only connected to the gates of the aforementioned transistors and is not connected to the body of M_0):

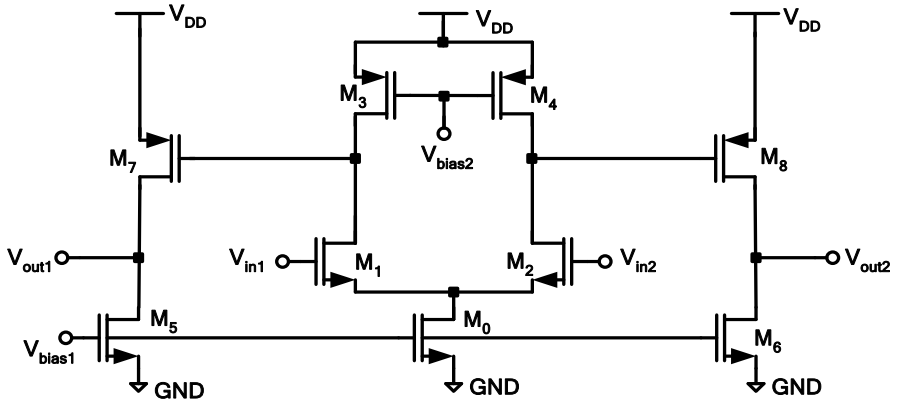
- V_{DD}=1.8V
- Total power consumption of 2.7 mW
- Minimum V_{out2} for which M_6 is in saturation and below which will go in triode is 0.2 V.
- L=0.5 μm for all the device

Use the following assumptions for your design

- The circuit is symmetric
- The bias current of the first stage is twice that of the second stage, i.e., $I_{0,DC}=2(I_{5,DC}+I_{6,DC})$.
- The magnitude of overdrive voltages of M_2, M_4, M_6, and M_8 are equal

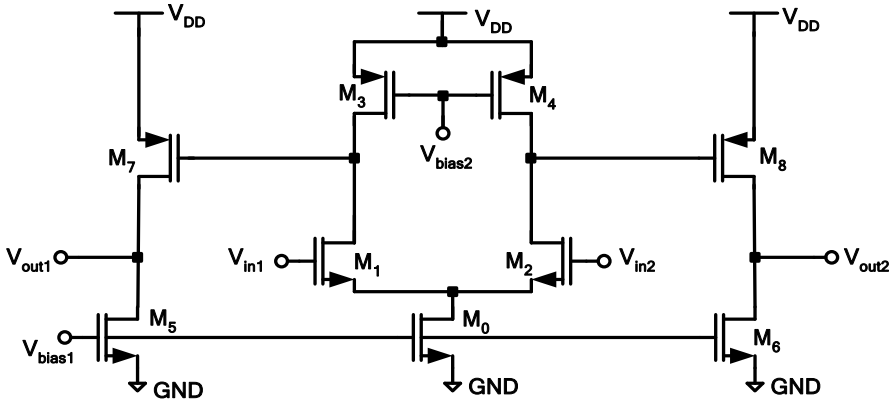
The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.1V^{-1}$, $\gamma = 0$, $V_{DD}=1.8V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_n C_{ox}=0.5\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.

Note: Use the parameter λ only for calculating the r_o of the transistors. **<u>Do not</u>** use λ in any other calculation including your bias currents.

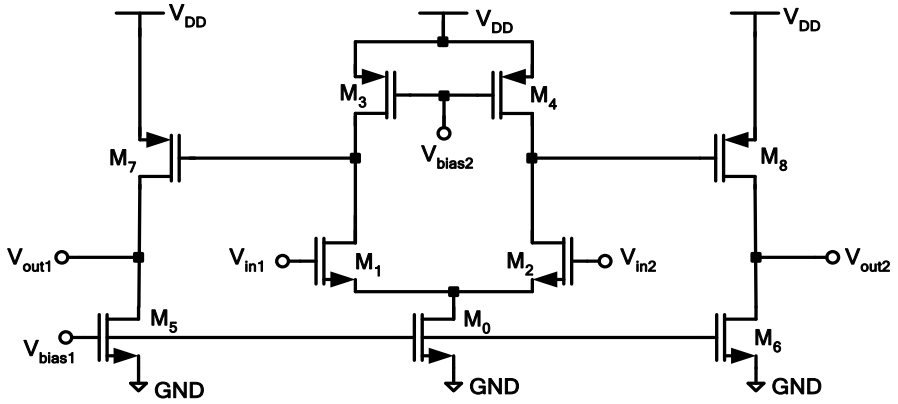


a) Find V_{bias1}, V_{bias2}, and the width of all transistors (i.e., W_0,W_1, W_2, W_3, W_4, W_5, W_6, W_7, and W_8). **[12 marks]**
b) What is the magnitude of the differential gain of the circuit? **[4 marks]**
c) What is the peak-to-peak differential output swing? **[4 marks]**

For your convenience the circuit diagram and transistor parameters is replicated here:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.1V^{-1}$, $\gamma = 0$, $V_{DD}=1.8V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_n C_{ox}=0.5\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.



For your convenience the circuit diagram and transistor parameters is replicated here: $\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.1V^{-1}$, $\gamma = 0$, $V_{DD}=1.8V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_n C_{ox}=0.5\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.



V_{bias1}= _____V, V_{bias2}=_____V, W_0=_____μm, W_1=_____μm,

W_2=_____μm, W_3=_____μm, W_4=_____μm, W_5=_____μm,

W_6=_____μm, W_7=_____μm, W_8=_____μm

|differential gain|=_____, Peak-to-peak differential output swing=_____

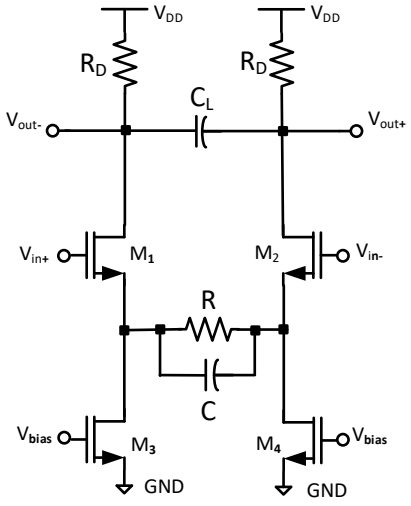
5. In the following circuit assume:

$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, V_{bias}=0.7 V, $V_{TH(NMOS)} = 0.5$ V, $\mu_n C_{ox}$=1 mA/V^2, $(W/L)_1=(W/L)_2$=128, $(W/L)_3=(W/L)_4$=50, R=0.5 kΩ, R_D=0.5kΩ, C=10pF, C_L=20pF.

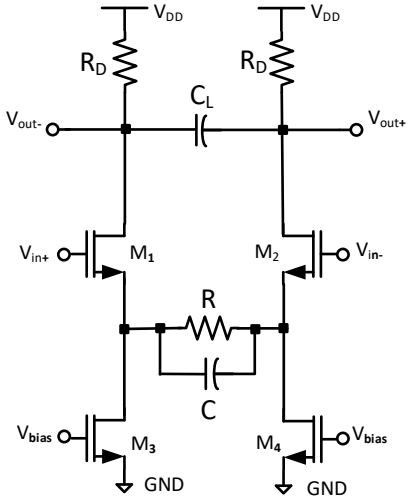
a) Ignoring all other parasitic device capacitances, and only taking into account the capacitors shown in the schematic diagram of the circuit, find the transfer function of the small-signal differential gain of the circuit, that is, $H(s) = \frac{V_{out+}(s)-V_{out-}(s)}{V_{in+}(s)-V_{in-}(s)}$ (where s is complex frequency in the Laplace domain). **[15 marks]**

b) Plot the bode plot of the magnitude of the frequency response, that is, Bode plot of $|H(j\omega)|$ as a function of ω. Please note that ω is the angular frequency in radian per second (For the frequency axis of your Bode plot, please use ω instead of f in Hz). Use $\omega = 1$ Mega radians per second as the starting angular frequency of your Bode plot, and plot $|H(j\omega)|$ up to $\omega = 10$ Giga radians per seconds. Use asymptotic approximation for your Bode plot (straight lines to show the segments the bode plot. Provide the numerical value of the key angular frequencies, i.e., angular frequency of the pole(s). **[5 marks]**

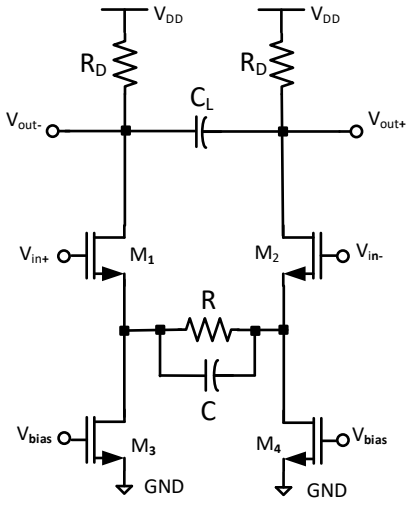
Hint 1: For finding the transfer function, you may want to analyze the associated small-signal model in the Laplace domain, that is, use impedance of the components in your analysis.
Hint 2: Please be mindful of the polarity of the signals. You may want to use the half-circuit analysis to find the transfer function of the small-signal differential gain.



For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{bias}=0.7$ V, $V_{TH(NMOS)} = 0.5$ V, $\mu_n C_{ox}=1$ mA/V^2, $(W/L)_1=(W/L)_2=128$, $(W/L)_3=(W/L)_4=50$, R=0.5 kΩ, R_D=0.5kΩ, C=10pF, C_L=20pF.



For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{bias}=0.7$ V, $V_{TH(NMOS)} = 0.5$ V, $\mu_n C_{ox}=1$ mA/V^2, $(W/L)_1=(W/L)_2=128$, $(W/L)_3=(W/L)_4=50$, R=0.5 kΩ, R_D=0.5kΩ, C=10pF, C_L=20pF.



This page is intentionally blank.