THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
ELEC 401 – Analog CMOS Integrated Circuit Design
Take-Home Midterm Exam
Due: Monday, October 18th, 2021 at 11:59 pm

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

Good luck!

This exam consists of 6 – 6/6 (= 5) questions and including the cover page has 6+6(=12) pages. Please check that you have a complete copy.

Surname First name

Student Number

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

READ THIS

IMPORTANT NOTE:

Candidates guilty of any of the following, or similar, dishonest practices shall be liable to disciplinary action:

Speaking or communicating with other candidates or non-candidates regarding the exam questions.

Purposely exposing their solution to the view of other candidates.

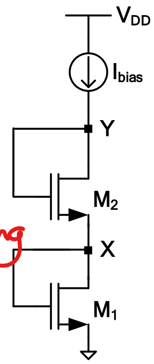
The plea of accident or forgetfulness shall not be received.

1. In the following circuit assume that the bulks of the two NMOS transistors are connected to ground, and furthermore assume that the current source is ideal with I_{bias}=4 mA, and for both transistors we have $\lambda = 0$, $\gamma = 1\ V^{1/2}$, $2\Phi_F$=0.64 V, $V_{TH0} = 0.4$ V, $\mu_n C_{ox} = 500\ \mu A/V^2$, and (W/L) = 100.

a) Find the voltage of node X? **[8 marks]**

b) Find the voltage of node Y? **[10 marks]**

c) If we were to implement the current source with a single PMOS transistor which would had a effective voltage of 0.5 (i.e., $V_{SG}-|V_{THP}| = 0.5$ V), then, what was the minimum required V_{DD} for the circuit to operate properly? **[2 marks]**



Sin e transistors M_1 and M_2 are diode-connected, and they are "on" they are operating in saturation region:

a) $I_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS_1} - V_{th_1})^2$

no body effect

$4mA = \frac{1}{2}\, 0.5\frac{mA}{V^2}(100)(V_X - V_{th_1})^2 \Rightarrow (V_X - 0.4)^2 = 0.16\ V^2$

$V_X - 0.4 = \pm 0.4 \Rightarrow \boxed{V_X = 0.8\ V}$

negative answer is not acceptable.

b) M_2 experiences body-effect as it's source voltage is $V_X = 0.8$ V

Thus, $V_{Th2} = V_{Tho} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$
$= 0.4 + 1\left(\sqrt{0.64+0.8} - \sqrt{0.64}\right) = 0.8\ V$

$I_2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{Th2})^2 = \frac{1}{2}0.5(100)(V_{GS2} - 0.8)^2$

$(V_{GS2} - 0.8)^2 = 0.16\ V \Rightarrow V_{GS2} - 0.8 = \pm 0.4\ V$

not acceptable.

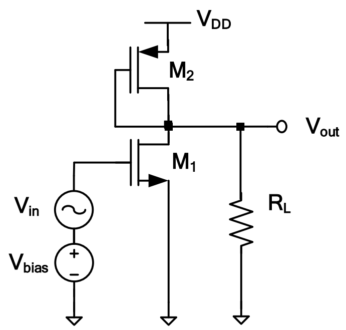
$V_{GS2} = V_Y - V_X = 1.2\ V \Rightarrow \underline{V_Y = V_X + 1.2 = \boxed{2.0\ V}}$

c) $V_{DD} \geq V_{eff}(PMOS) + V_Y \Rightarrow V_{DD} \geq 2.5\ V$

Voltage of Node X: 0.8 V, Voltage of Node Y: 2.0 V

Minimum required V_{DD} = 2.5 V

2. In the following circuit, assume that V_{DD} = 3V and the total dc power consumption of the circuit is 2.25mW, and the dc level of the output is 1.5 V. Furthermore, assume that M_1 is operating in saturation region, and for transistors we have $\lambda = 0$, $V_{TH0(NMOS)}$= 0.5V, $V_{TH0(PMOS)}$= – 0.5V, $\mu_n C_{ox}$ = 200 $\mu A/V^2$, $\mu_p C_{ox}$=100 $\mu A/V^2$, and $(W/L)_1$ =80.



a) Find the required V_{bias} for which the dc bias current of M_1 is 0.5 mA. **[4 marks]**
b) Find $(W/L)_2$. **[4 marks]**
c) Find R_L. **[4 marks]**
d) What is the small-signal gain of the circuit? **[4 marks]**
e) Is the assumption that M1 is operating in saturation correct. If so, why? **[2 marks]**
f) What is the maximum peak-to-peak symmetric signal swing of the output? **[2 marks]**

a) $I_1 = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS_1} - V_{Th})^2$

$0.5 = \frac{1}{2} \times 0.2 \frac{mA}{V^2}(80)(V_{bias} - V_{th})^2 \Rightarrow (V_{bias} - V_{Th})^2 = \frac{1}{16}$

$V_{bias} - V_{th_1} = \pm 0.25V \Longrightarrow V_{bias} = 0.75V$

negative not accepable

b) $P = I_2 V_{DD} \Rightarrow 2.25mW = 3 \times I_2 \Longrightarrow I_2 = 0.75mA$

M_2 is diode connected so it is in saturation:

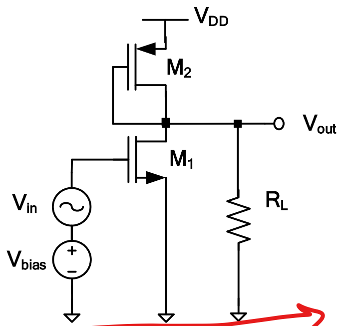
$I_2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2(V_{SG2} - |V_{th2}|)^2 \Rightarrow 0.75 = \frac{1}{2} \times 0.1 \times \left(\frac{W}{L}\right)_2 (3 - 1.5 - 0.5)^2$

$\left(\frac{W}{L}\right)_2 = 15$

c) $I_2 = I_1 + I_R \Longrightarrow 0.75 = 0.5 + I_L \Longrightarrow I_L = 0.25\,mA$

$I_L = \frac{V_{out,DC}}{R_L} = \frac{1.5}{R_L} = 0.25\,mA \Longrightarrow R_L = 6k\Omega$

For your convenience the circuit and its parameters are duplicated below:
V_{DD} = 3V and the total dc power consumption of the circuit is 2.25mW, and the dc level of the output is 1.5 V. Furthermore, $\lambda = 0$, $V_{TH0(NMOS)} = 0.5V$, $V_{TH0(PMOS)} = -0.5V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, and $(W/L)_{NMOS} = 80$.



d) $A_v = -g_{m1}\left(R_L \| \frac{1}{g_{m2}}\right)$

$g_{m1} = \frac{2I_{D1}}{V_{eff1}} = 4\ mS$

$g_{m2} = \frac{2I_{D2}}{V_{eff2}} = 1.5\ mS$

$A_v = -4 \times \left(6 \| \frac{1}{1.5mS}\right) \Rightarrow A_v = 2.4\ V/V$

e) $V_{eff1} = V_{GS} - V_{Th1} = 0.75 - 0.5 = 0.25V$

$V_{DS1} = V_{out,DC} = 1.5V \Rightarrow V_{eff1} < V_{DS1}$

$\Rightarrow M_1$ is in saturation

f) $V_{out,min} = V_{eff1} = 0.25V$

for $V_{out,max}$, note that for M_2 to be ON $V_{SG2} \geq |V_{Th2}| \Rightarrow V_{DD} - V_{out} \geq 0.5$

$V_{out} \leq 3 - 0.5 = 2.5V$

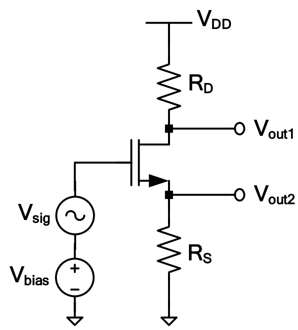
symmetric swing = 1V peak
2V peak to peak

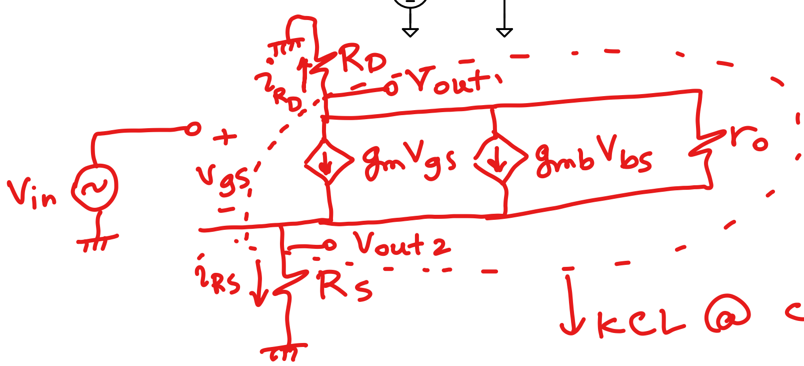
(3, 2.5, 1V, 1.5, 1.25V, 0.25, 0)

V_{bias} = 0.75V. $(W/L)_2$ = 15, R_L = 6KΩ

small-signal gain 2.4V/V, region of operation of M_1 = saturation output symmetric peak-to-peak signal swing= 2V ,

3. In the following circuit, assuming that the transistor is biased properly so that it is not operating in the cut-off region, show that in the small-signal domain, even when $\lambda > 0$ and $\gamma > 0$ (i.e., in the presence of channel length modulation and body effect), V_{out1} and V_{out2} are related by: $V_{out1}/V_{out2} = -R_D/R_S$. **[20 marks].**





KCL @ closed boundary:

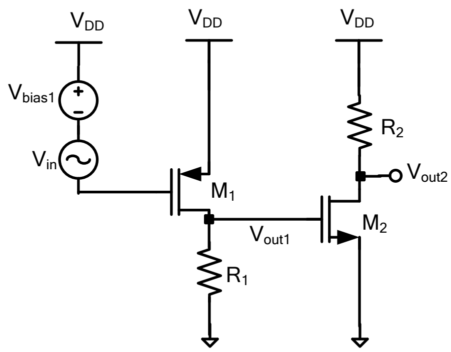
$i_{RD} + i_{RS} = 0$

$$\Rightarrow i_{RD} = -i_{RS} \Rightarrow \frac{V_{out1} - 0}{R_D} = -\frac{V_{out2} - 0}{R_S} \Rightarrow \frac{V_{out1}}{V_{out2}} = -\frac{R_D}{R_S}$$

4. Design the following two-stage amplifier with the schematic shown below and these design specifications:

- V_{DD}=1.8 V
- Total power consumption of the amplifier is 1.8 mW
- V_{bias1} and the level of V_{out1} and V_{out2} are all 0.9 V
- L=0.25 µm for both transistors
- The output impedance of the circuit, that is the impedance seen at V_{out2} is 1.8 kΩ

Assume the following technology parameters:
λ=0, V_{DD}=1.8V, $V_{TH(NMOS)}$ =0.4V, $V_{TH(PMOS)}$ =–0.4V, μ_nC_{ox}=500 µA/V², μ_pC_{ox}=250 µA/V². Furthermore, assume that V_{in} is a small-signal source.



a) Find R_1, R_2, W_1 and W_2. **[12 marks]**
b) What is the overall gain of the system, i.e., V_{out2}/V_{in}. **[3 marks]**
c) What is the maximum symmetric peak-to-peak output swing. **[3 marks]**
d) If the input V_{in} is a small-signal sinusoid, what would be the maximum amplitude of the input signal for which the circuit operates as expected. **[2 marks]**

a) $P = I_{D1}V_{DD} + I_{D2}V_{DD} = 1.8\,mW \Longrightarrow I_{D1}+I_{D2} = \frac{1.8\,mW}{1.8\,V} = 1\,mA$

Given that $\lambda=0$, the output impedance is R_2, thus, $R_2 = 1.8\,k\Omega$

$\frac{V_{DD}-V_{out2,DC}}{R_2} = I_{D2} \Longrightarrow I_{D2} = \frac{1.8-0.9}{1.8} = 0.5\,mA$

Both transistors are in saturation since:

For M_1: $V_{SD_1} = 1.8 - 0.9 = 0.9$ ($\uparrow V_{out1,DC}$) $V_{SG_1} = 1.8 - 0.9 = 0.9$ ($V_{DD}-V_{bias1}$) $\Rightarrow V_{SG}-|V_{th1}| < V_{SD1}$

For M_2: $V_{DS2} = 0.9\,V$ ($\uparrow V_{out2,DC}$), $V_{GS2} = V_{out1} = 0.9V \Rightarrow V_{GS2}-V_{th2} < V_{DS2}$

$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2}-V_{th2})^2 \Longrightarrow 0.5 = \frac{1}{2}\,0.5\left(\frac{W}{L}\right)_2 (0.9-0.4)^2$

$\left(\frac{W}{L}\right)_2 = 8 \Longrightarrow W_2 = 8\times L_1 = 8\times 0.25 = 2\,\mu m$

$I_{D1} + I_{D2} = 1\,mA$, $I_{D2} = 0.5\,mA \Longrightarrow I_{D1} = 0.5\,mA$

$I_{D1} = \frac{V_{out1}}{R_1} \Rightarrow 0.5 = \frac{0.9}{R_1} \Rightarrow$ $\boxed{R_1 = 1.8\,k\Omega}$

$I_{D1} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{SG1} - |V_{th}|)^2$

$0.5 = \frac{1}{2}\, 0.25 \left(\frac{W}{L}\right)_1 (1.8 - 0.9 - 0.4)^2$

$\left(\frac{W}{L}\right)_2 = 16 \Longrightarrow W_2 = 16 \times L_2 = 16 \times 0.25 = 4\,\mu m$

b) $A_V = \frac{V_{out1}}{V_{in}} \times \frac{V_{out2}}{V_{out1}} = (-g_{m1} R_1) \times (-g_{m2} R_2)$

$g_{m1} = \frac{2 I_{D1}}{V_{eff1}} = \frac{2 \times 0.5}{0.9 - 0.4} = 2\,mS$

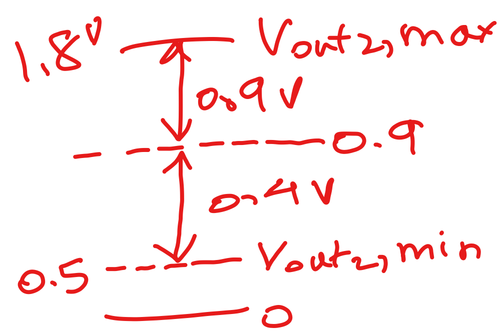
$g_{m2} = \frac{2 I_{D2}}{V_{eff2}} = \frac{2 \times 0.5}{0.9 - 0.4} = 2\,mS$

$A_V = (-2 \times 1.8)(-2 \times 1.8) = \boxed{12.96\ V/V}$

c) $V_{out2,min} = V_{eff2} = 0.5\,V$

$V_{out2,max} = V_{DD} = 1.8\,V$

$V_{peak\text{-}to\text{-}peak} = 2 \times 0.4 = 0.8\,V$ (symmetric)



d) Max amplitude of input

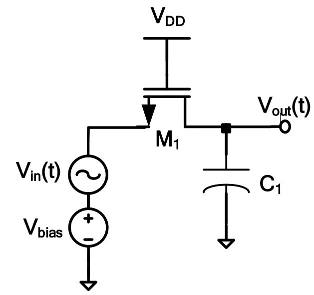
$V_{in,max} = \frac{V_{out,p\text{-}p}/2}{A_V} = \frac{0.8/2}{12.96} = 0.031\,mV$

W_1= 4 μm, W_2= 2 μm, R_1= 1.8 kΩ, R_2= 1.8 kΩ,

V_{out2}/V_{in}= 12.96 V/V, Maximum pea-to-peak symmetric output swing= 0.8 V

Maximum amplitude of the small-signal input sinusoid = 31 mV

5. Consider the following circuit:



The technology parameters are:
$\lambda_{(NMOS)}$=0 V^{-1}, γ=0, V_{DD}=3.3 V, $V_{TH(NMOS)}$=0.5V, $\mu_n C_{ox}$=0.1 mA/V^2, and C_{ox}= 5 fF/μm^2.

Assume C_1 = 2 pF and for the transistor we have: L_1= 0.5 μm and W_1= 5 μm.
a) If V_{bias}=0.8 V, what is the region of operation of the transistor and why**? [6 marks]**
b) If the input signal, $V_{in}(t)$, is a step function with a small magnitude of 10 mV (i.e., V_{in} abruptly changes from 0 V to 10 mV at time t = 0), what is $V_{out}(t)$ for $t \geq 0$? **[6 marks]**
c) Repeat parts (a) and (b) for V_{bias}=1.8V. **[8 marks]**

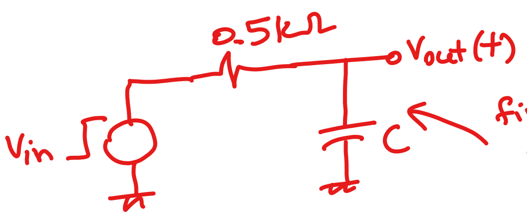
a) $V_{GS1} = V_{DD} - V_{bias} = 3.3 - 0.8 = 2.5V > V_{th}$

So transistor is on; since its current is zero (drain is open circuit) therefore the transistor is in deep triode. $I_D=0 \Rightarrow V_{DS}=0 \Rightarrow V_D=V_S$

b) In deep triode transisor can be modelled by a resistor of value

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS_1}-V_{th})} = \frac{1}{0.1\frac{mA}{V^2} \times \frac{5}{0.5}(2.5-0.5)} = 0.5k\Omega$$

small-signal model:



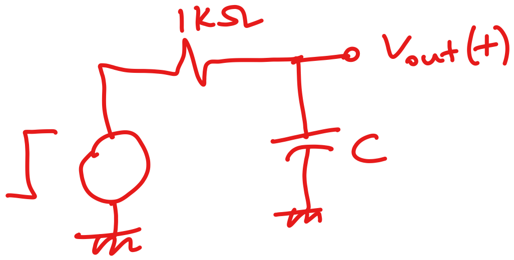
$$V_{out}(t) = [V_{out}(0) - V_{out}(\infty)]e^{-t/RC} + V_{out}(\infty)$$
$$= [0 - 10mV]e^{-t/1ns} + 10mV$$
$$= 10mV(1-e^{-t/1ns})$$

$$V_{out,total}(t) = V_{out,DC} + V_{out}(t) = 0.8V + 10\,mV(1-e^{-t/1ns})$$

c) For $V_{bias} = 1.8V \Rightarrow V_{GS_1} = V_{DD} - V_{bias} = 3.3 - 1.8 = 1.5 > V_{th}$

Transistor is still in deep triode

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS_1}-V_{th})} = \frac{1}{0.1\frac{mA}{V^2} \frac{5}{0.5}(1.5-0.5)} = 1k\Omega$$



$$V_{out}(t) = [V_{out}(0^+) - V_{out}(\infty)]e^{-t/RC} + V_{out}(\infty)$$

$$V_{out}(t) = [0 - 10mV]e^{-t/2ns} + 10mV$$

$$= 10mV(1 - e^{-t/2ns})$$

$$V_{out,total}(t) = V_{out,DC} + V_{out}(t) = 1.8V + 10mV(1 - e^{-t/2ns})$$

For V_{bias}=0.8V: Region of operation of M_1: ____________, $V_{out}(t)$=________________

For V_{bias}=1.8V: Region of operation of M_1: ____________, $V_{out}(t)$=________________

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