THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 401 – Analog CMOS Integrated Circuit Design
Take-Home Midterm Exam
Due: Monday, November 8th, 2021 at 11:59 pm

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

Good luck!

This exam consists of 6 – 6/6 (= 5) questions and including the cover page has 6+6(=12) pages. Please check that you have a complete copy.

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

Surname First name

Student Number

READ THIS

IMPORTANT NOTE:

Candidates guilty of any of the following, or similar, dishonest practices shall be liable to disciplinary action:

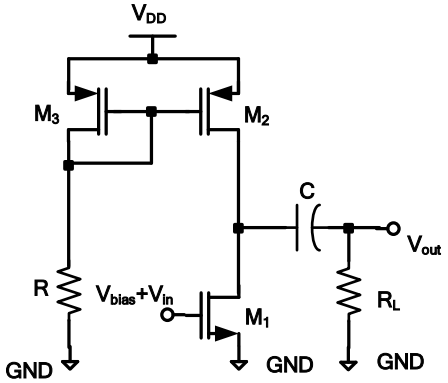
Speaking or communicating with other candidates or non-candidates regarding the exam questions.

Purposely exposing their solution to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. In the following amplifier, assume the decouple capacitor C is large enough so that it can be considered a short circuit for the small-signal analysis. Furthermore, assume that:

$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_nC_{ox}=1mA/V^2$, $\mu_pC_{ox}=0.25\ mA/V^2$, $(W/L)_3=8$, and $(W/L)_2=32$, R=8 kΩ and R_L=10 kΩ. The DC component of the input signal is V_{bias} and the small-signal component of the input is V_{in}.



a) Assuming that the magnitude of the small-signal gain (magnitude of V_{out}/V_{in}) is 40 V/V find V_{bias} and $(W/L)_1$ **[14 marks]**
b) For this circuit, for transistors M_1 and M_2 to operate in saturation, find the minimum and maximum voltage level at the drain of M_1. **[6 marks]**.

$|A_v|=|-g_{m1}R_L|=g_{m1}R_L=40 \Rightarrow g_{m1}=\frac{40}{R_L}=\frac{40}{10}=4mU$

For M_3 we have (note that M_3 is diode-connected so if it is on, it operates in saturation region) which is the case here

$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_3\left(V_{SG_3}-|V_{thp}|\right)^2=I_{D3}$, $V_{SG3}=V_{DD}-RI_{D3}=3-8I_{D3}$

$\frac{1}{2}0.25(8)(3-8I_{D3}-0.5)^2=I_{D3} \Rightarrow (2.5-8I_{D3})^2=I_{D3}$

$6.25+64I_{D3}^2-40I_{D3}=I_{D3} \Rightarrow 64I_{D3}^2-41I_{D3}+6.25=0$

$\Rightarrow I_{D3}=0.25\,mA$ or $I_{D3}=\frac{25}{64}\,mA$

$I_{D3}=\frac{25}{64}$ mA is not acceptable since $RI_{D3}=8\times\frac{25}{64}=3.125V$ >3V

$I_{D3}=0.25mA$

$$\frac{I_{D2}}{I_{D3}}\approx\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_3}\Longrightarrow I_{D2}=\frac{32}{8}\times0.25=1mA$$

$I_{D1}=I_{D2}=1mA$

$$g_{m1}=\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}}\Longrightarrow 4=\sqrt{2\times1\times\left(\frac{W}{L}\right)_1\times1}$$

$$\left(\frac{W}{L}\right)_1=8$$

$$g_{m1}=\frac{2I_{D1}}{V_{eff1}}\Longrightarrow V_{eff1}=\frac{2I_{D1}}{g_{m1}}=\frac{2\times1}{4}=0.5V$$

$$V_{GS1}=0.5+V_{th1}=0.5+0.5=1V$$

$$\Longrightarrow V_{bias}=1V$$

For M_1 being in saturation:

$V_{DS1}\geq V_{eff1}\Longrightarrow V_{DS1,min}=V_{eff1}=0.5V$

For M_2 being in saturation V_{SG2}

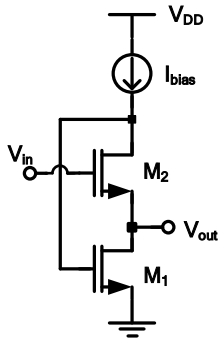
$$V_{SD2}\geq V_{eff2}\Longrightarrow V_{DD}-V_{DS1}\geq\left(V_{DD}-RI_{D3}\right)-|V_{th2}|$$

$V_{bias}=$ _____ V, $(W/L)_1=$ _____, $V_{DS1,min}=$ _____ V, $V_{DS1,max}=$ _____ V

$$V_{DS1}\leq RI_{D3}+|V_{th2}|\Longrightarrow V_{DS1,max}=8\times0.25+0.5=2.5V$$

2. In the follwing circuit assume that:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 1.8V$, $I_{bias} = 32mA$, $V_{TH(NMOS)} = 0.4V$, and $\mu_n C_{ox} = 1\ mA/V^2$.
Furthermore, assume that both transistors are supposed to operate in saturation region and their sizes are: $(\frac{W}{L})_1 = 100$ and $(\frac{W}{L})_2 = 400$.

a) Find the minimum and maximum dc voltage levels at node V_{out}. **[8 marks]**
b) Find the allowable minimum and maximum dc voltage level of the input node. **[8 marks]**
c) If γ was not zero, would the allowable input signal swing range change, and if so, why? **[4 marks]**



For M_1 to be in saturation

$V_{out} \geq V_{eff1}$ $\quad V_{eff1} = \sqrt{\frac{2I_{D1}}{\mu C_{ox}(\frac{W}{L})_1}} = \sqrt{\frac{2 \times 32mA}{1 \times 100}} = \sqrt{0.64} = \pm 0.8$

negative not acceptable as $V_{eff} \geq 0$

Thus, $V_{out} \geq 0.8V$ (1)

$V_{GS1} = V_{eff1} + V_{th1} = 0.8 + 0.4 = 1.2V$

For M_2 to be in saturation

$V_{DS2} \geq V_{eff2} \Rightarrow V_{D2} - V_{S2} \geq V_{eff2} \Rightarrow V_{GS1} - V_{out} \geq V_{eff2}$

$V_{out} \leq V_{GS1} - V_{eff2}$

$V_{eff2} = \sqrt{\frac{2I_{D2}}{\mu C_{ox}(\frac{W}{L})_2}} = \sqrt{\frac{2 \times 32}{1(400)}} = \sqrt{\frac{64}{400}} = 0.4V$

$V_{out} \leq 1.2 - 0.4 \Rightarrow V_{out} \leq 0.8\ V$ (2)

From (1) and (2) $V_{out} = 0.8\ V$

$V_{in,min} = V_{out,min} + V_{GS2} = 0.8 + (V_{eff2} + V_{th2})$

$= 0.8 + 0.4 + 0.4$

$= 1.6\ V$

($V_{out,min}$ = V_{eff1})

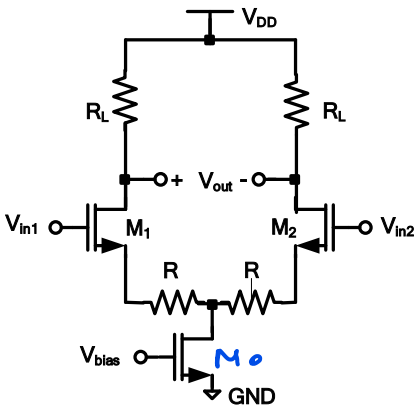
$V_{GD2} \leq V_{th2} \Rightarrow V_{in} - V_{GS1} \leq 0.4$

$V_{in} \leq V_{GS1} + 0.4 \Rightarrow V_{in,max} = 1.6\ V$

$V_{out,min}$= _____V, $V_{out,max}$ =_____, $V_{in,min}$= _____V, $V_{in,max}$= _____V

For $\gamma \neq 0$ would allowable input signal swing range change and why?

3. Consider the following differential amplifier.

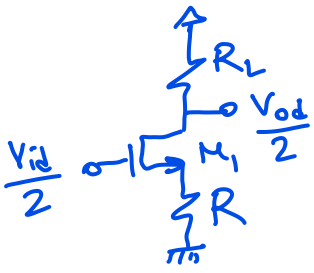


Assume all transistors are operating in saturation region and $\lambda=\gamma=0$, $V_{DD}=3$ V, $V_{TH(NMOS)}=0.5$ V, $\mu_n C_{ox}=1$ mA/V^2, R=100 Ω, $(W/L)_1=(W/L)_2=16$ and $(W/L)_0=32$. Also, assume that the $V_{bias}=0.75$ V and the circuit is symmetric.

a) What should the value of R_L be if the magnitude of the differential voltage gain of the circuit is 4 V/V **[10 marks]**
b) For the circuit to operate properly (i.e., all transistors operate in their saturation region), what are the minimum and maximum values of the input common-mode voltage (i.e., input DC voltage) **[10 marks]**

Using half circuit concept

Since $\lambda=0$ and $\gamma=0$ the gain will be:



$$A_v = \frac{\frac{V_{od}}{2}}{\frac{V_{id}}{2}} = \frac{-R_L}{\frac{1}{g_{m1}} + R}$$

To find g_{m1} since we have the size of M_1 and the information for finding its bias current, we will proceed by finding I_{D1} : $I_{D0} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 (V_{bias}-V_{th})^2$

$I_{D0} = \frac{1}{2}\times 1 \times 32 (0.75-0.5)^2 = 1\text{ mA}$

$\Rightarrow I_{D1} = \frac{I_{D0}}{2} = 0.5\text{ mA}$

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2 \times 1 \frac{mA}{V^2} \times 16 \times 0.5} = 4\ mS$$

$$\text{Thus, } |A_v| = 4 = \frac{R_L}{\frac{1}{g_{m1}} + R_S} \Rightarrow 4 = \frac{R_L}{\frac{1}{4} + 0.1}$$

$$\Rightarrow R_L = 1.4\ k\Omega$$

$$V_{in,min} = V_{GS1} + R_S I_{D1} + \underbrace{V_{DS0,min}}_{V_{eff0}}$$

$$V_{in,min} = \underbrace{\sqrt{\frac{2I_{D1}}{\mu C_{ox}\left(\frac{W}{L}\right)_1}} + V_{th}}_{V_{GS1}} + 0.1 \times 0.5\ mA + 0.25$$

$$= 1.05\ V$$

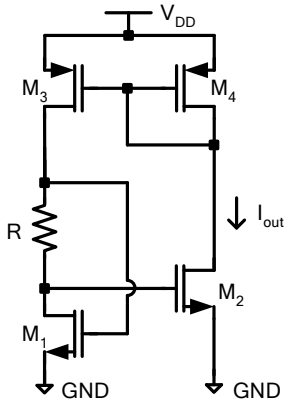
$$V_{in1} - V_{D1} < V_{th} \Rightarrow V_{in1} < V_{D1} + V_{th}$$

$$V_{in1} \lesssim V_{DD} - R_L I_{D1} + V_{th} \Rightarrow V_{in,cm\ max} = 3 - 1.4 \times 0.5 + 0.5 = 2.8\ V$$

R_L: 1.4kΩ, $V_{in,cm\ (min)}$: 1.05 V, $V_{in,cm\ (max)}$: 2.8V

4. In the following circuit, assuming that all transistors are in saturation, $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$, and $\lambda = \gamma = 0$:

i) Find an expression for I_{out} in terms of R, transistor parameters (e.g., μ and C_{ox}), and transistor sizes **[10 marks].**
ii) What would be the percentage change in I_{out} if V_{DD} is increased by 10%. **[5 marks]**
iii)How would the expression for I_{out} derived in part (i) change if $\gamma \neq 0$ and why? **[5 marks]**



(i) Since $(\frac{W}{L})_3 = (\frac{W}{L})_4$ and $\lambda = 0 \Rightarrow I_{D3} = I_{D4} = I_{out}$

$V_{GS2} + R I_{out} = V_{GS1} \Rightarrow \sqrt{\frac{2I_{out}}{\mu C_{ox}(\frac{W}{L})_1}} + V_{th1} + R I_{out} = \sqrt{\frac{2I_{out}}{\mu C_{ox}(\frac{W}{L})_2}} + V_{th2}$

Since M_1 and M_2 do not experience any body effect: $V_{th1} = V_{th2}$

Thus $R I_{out} = \sqrt{\frac{2 I_{out}}{\mu_n C_{ox}(\frac{W}{L})_1}} \left(1 - \sqrt{\frac{(\frac{W}{L})_1}{(\frac{W}{L})_2}}\right)$

assuming $I_{out} \neq 0$

$$I_{out} = \frac{1}{R^2 \mu C_{ox}(\frac{W}{L})_1} \left(1 - \sqrt{\frac{(\frac{W}{L})_1}{(\frac{W}{L})_2}}\right)^2$$

(iii)

The source of all NMOS transistors is connected to ground so their bulk-source voltage, V_{BS} is 0.

The source of both pmos transistors is connected to V_{DD}, so their bulk-source is also 0. Thus, none of the transistors would experience body effect, so for $\gamma \neq 0$ the expression for I_{out} would be the same as part (i)

(ii) I_{out} is independent of V_{DD}, so if V_{DD} changes by 10%, I_{out} will not change.

5. The 5-transistor operational transconductance amplifier (that is, the differential to single-ended structure with active current mirror load that we discussed in class) is a popular choice in designing operational amplifiers. Consider the following two-stage amplifier based on the topology shown below (first stage is a differential to signle-ended amplifier followed by the second stage which is a common-source amplifier) with the following design specifications:

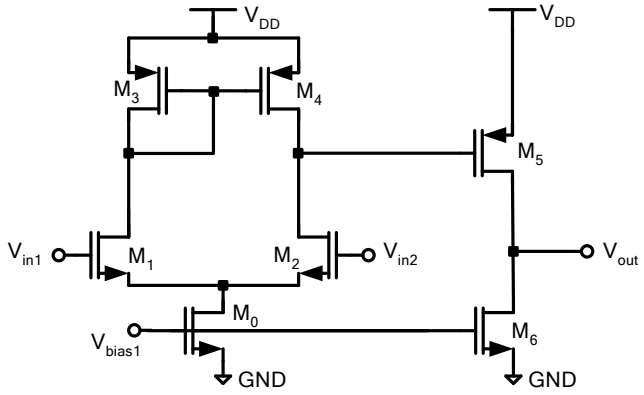
- V_{DD}=3 V
- Total power consumption of 3 mW
- Output swing of 2.6 V
- Magnitude of the overall gain: 1000 V/V
- L = 0.4μm for all the device

Use the following assumptions for the design:

- Allocate equal effective voltages for M_5 and M_6
- Assume the bias current of M_0 and M_6 are equal.
- For the purpose of DC analysis, assume V_{SG3}=V_{SG5}

The technology parameters are:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

Note: Use the parameter λ only for calculating the r_o of the transistors and for the small-signal gain. **<u>Do not</u>** use λ in any other calculation including for calculating bias currents.



Find V_{bias1}, and all the transistor widths (i.e., W_0, W_1, W_2, W_3, W_4, W_5, W_6). **[20 marks]**

$P_{total} = I_{total} \times V_{DD} \Rightarrow I_{total} = I_0 + I_6 = \frac{P_{total}}{V_{DD}} = \frac{3}{3} = 1mA$

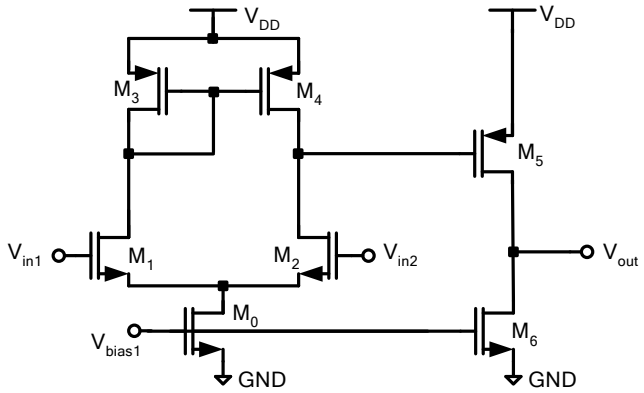
$I_0 = I_6$ and $I_0 + I_6 = 1mA \Rightarrow I_0 = I_1 = 0.5\,mA$

Output swing $= V_{DD} - V_{eff5} - V_{eff6}$ and $V_{eff5} = V_{eff6}$

$\Rightarrow V_{DD} - 2V_{eff6} = 2.6V \Rightarrow V_{eff6} = \frac{3-2.6}{2} = 0.2V$

$V_{bias} = V_{eff6} + V_{th} = 0.2 + 0.5 = 0.7V$

For your convenience the circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1$ mA/V^2, $\mu_p C_{ox} = 0.5$ mA/V^2.



$I_o = 0.5\,mA \Rightarrow 0.5 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_o (V_{bias} - V_{thn})^2 = \frac{1}{2}1\left(\frac{W}{L}\right)_o (0.7-0.5)^2$

$\left(\frac{W}{L}\right)_o = 25 \Rightarrow W_o = 25 \times L_o = 25 \times 0.4 = 10\,\mu m$

$I_6 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 (V_{bias} - V_{thn})^2 \Rightarrow 0.5 = \frac{1}{2}1\left(\frac{W}{L}\right)_6 (0.7-0.5)^2$

$\Rightarrow \left(\frac{W}{L}\right)_6 = 25 \Rightarrow W_6 = 25 \times L_6 = 10\,\mu m$

Since $V_{eff6} = V_{eff5} \Rightarrow V_{eff5} = 0.2V$

$I_5 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_5 (V_{eff5})^2 \Rightarrow 0.5 = \frac{1}{2}0.5\left(\frac{W}{L}\right)_5 (0.2)^2$

$\left(\frac{W}{L}\right)_5 = 50 \Rightarrow W_5 = 50 \times L = 20\,\mu m$

$I_o = 0.5\,mA \Rightarrow I_1 = I_3 = 0.25\,mA$ and $I_2 = I_4 = 0.25\,mA$

$V_{SG3} = V_{SG5} \Rightarrow V_{eff3} = V_{eff5} = 0.2$

$I_3 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_3 (V_{eff3})^2 \Rightarrow 0.25 = \frac{1}{2}0.5\left(\frac{W}{L}\right)_3 (0.2)^2 \Rightarrow \left(\frac{W}{L}\right)_3 = 25$

For your convenience the circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1$ mA/V^2, $\mu_p C_{ox} = 0.5$ mA/V^2.

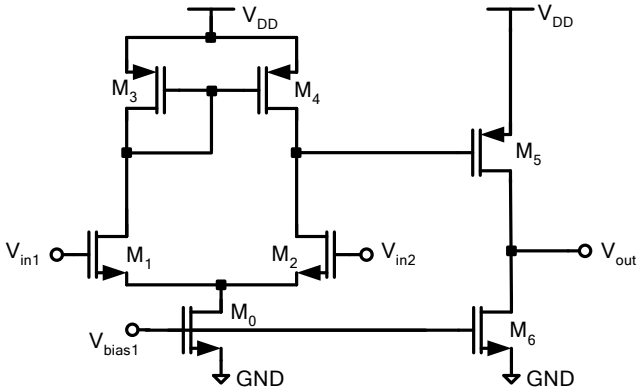
$W_3 = 2.5 L_3 = 10\mu m$

Similarly

$I_4 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_4 (V_{eff4})^2$

$0.25 = \frac{1}{2} 0.5 \left(\frac{W}{L}\right)_4 (0.2)^2$

$\Rightarrow W_4 = 10\mu m$



To find W_1 and W_2 we can use the information given about the gain and find $g_{m1} (= g_{m2})$ and from g_{m1} and I_{D1} find W_1. We have: $|A_v| = g_{m1}(r_{o2} \| r_{o4})\, g_{m5}(r_{o5} \| r_{o6})$

$r_o = \frac{1}{\lambda I_D}$ $\quad r_{o2} = \frac{1}{\lambda I_4} = \frac{1}{0.1 \times 0.25} = 40\ k\Omega$

$r_{o4} = \frac{1}{\lambda I_4} = \frac{1}{0.1 \times 0.25} = 40 k\Omega$, $r_{o5} = r_{o6} = \frac{1}{\lambda I_5} = \frac{1}{0.1 \times 0.5} = 20 k\Omega$

$\Rightarrow g_{m1}(40 \| 40) \frac{2I_5}{V_{effs}} (20 \| 20) = 1000 \Rightarrow g_{m1} = 1$ mU

$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} \Rightarrow 1 = \sqrt{2 \times 1 \times \left(\frac{W}{L}\right)_1 0.25} \Rightarrow \left(\frac{W}{L}\right)_1 = 2 \Rightarrow W_1 = 0.8\ \mu m$

$V_{bias1} =$ 0.7 V, $W_0 =$ 10 µm, $W_1 =$ 0.8 µm, $W_2 =$ 0.8 µm

$W_3 =$ 10 µm, $W_4 =$ 10 µm, $W_5 =$ 20 µm, $W_6 =$ 10 µm

$g_{m1} = g_{m2}$ and $I_{D1} = I_{D2} \Rightarrow W_2 = W_1 = 0.8\ \mu m$