THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
**ELEC 401 – Analog CMOS Integrated Circuit Design**
**Take-Home Midterm Exam**
**Due: Wednesday October 28th, 2020 at 11:59 pm**

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone except the instructor. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

**Good luck!**

**This exam consists of 5 questions and including the cover page has 16 pages. Please check that you have a complete copy.**

Surname First name

Student Number

| # | MAX | GRADE |
|---|---|---|
| 1 | 20 | |
| 2 | 20 | |
| 3 | 20 | |
| 4 | 20 | |
| 5 | 20 | |
| TOTAL | 100 | |

**READ THIS**

IMPORTANT NOTE:

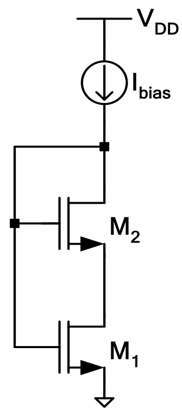
*Candidates guilty of any of the following, or similar, dishonest practices shall be liable to disciplinary action:*

*Speaking or communicating with other candidates or non-candidates regarding the exam questions.*

*Purposely exposing their solution to the view of other candidates.*

*The plea of accident or forgetfulness shall not be received.*

**1.** In the following circuit assume that the bulks of the two NMOS transistors are connected to ground, and furthermore for both transistors $\lambda=0$, and $\gamma\neq0$.
a) If $I_{bias} > 0$, what is the region of operation of transistors $M_1$ and $M_2$? **[14 marks]**
b) For $I_{bias} > 0$, does the region of operation of $M_1$ and $M_2$ depend on the size of the transistors. In other word, does it depend on any or all of the values of $W_1$, $W_2$, $L_1$, and $L_2$. Why? **[6 marks]**




a) With $I_{bias} > 0$ both transistors are on.

$M_2$ is diode connected so it is in saturation (Also its $V_{GD2} = 0 < V_{th2}$)

For $M_1$, we have

$V_{GD1} = V_{GS2}$

and since $M_2$ is on $V_{GS2} > V_{th2}$

Also due to body effect

$V_{Th2} > V_{Th1}$

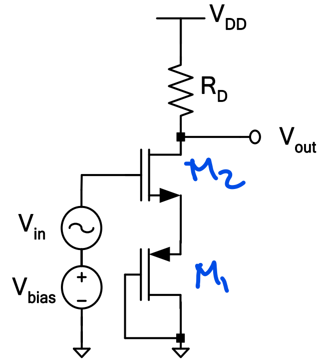
Thus, $V_{GD1} > V_{Th1}$, that is $M_1$ is in triode.

b) As mentioned above, irrespective of transistor sizing, when $I_D > 0$ both transistors are on and since $V_{GD2} = 0 < V_{Th2}$, $M_2$ is in saturation and since $V_{GD1} > V_{Th1}$ $M_1$ is in triode (independent of sizes of trasistors)

Region of operation of $M_1$:_______________, Region of operation of $M_1$:

Does the region of operation of $M_1$ and M2 depend on the sizing of transistors? __________ (your answer should be based on the justification presented in your solution)

**2.** In the following circuit, assuming the NMOS transistor is operating in the saturation region: Assume $\lambda = \gamma = 0$, $V_{TH0(NMOS)} = 0.5V$, $V_{TH0(PMOS)} = -0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $(W/L)_{NMOS} = 40$, $(W/L)_{PMOS} = 80$, and $V_{DD}=3V$.




a) Find the required $V_{bias}$ for which the dc bias current of the circuit is 1mA. **[5 marks]**

$I = 1mA \Rightarrow 1mA = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{SG1} - |V_{th1}|)^2$

$1mA = \frac{1}{2}\, 0.1\frac{mA}{V^2}(80)(V_{SG1} - 0.6)^2$

$\Rightarrow (V_{SG} - 0.6)^2 = \frac{1}{4} \Rightarrow V_{SG} - 0.6 = \pm 0.5$ -0.5 is not acceptable since transistor would be off.

$V_{SG} = 0.6 + 0.5 = 1.1\,V \leftarrow V_{S2}$ (Voltage of the source of M2)

For the NMOS transistor

$1mA = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{Th2})^2 = \frac{1}{2}\, 0.2\frac{mA}{V^2}(40)(V_{GS2} - V_{Th2})^2$

$(V_{GS2} - V_{Th2})^2 = \frac{1}{4} \Rightarrow V_{GS2} - V_{th2} = \pm 0.5\,V \Rightarrow V_{GS2} = 0.5 + 0.5 = 1V$

(negative not acceptable)

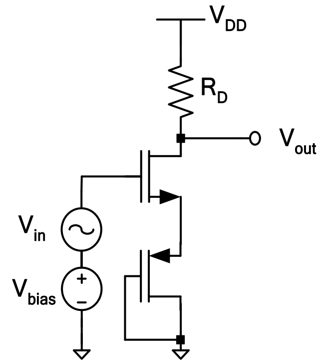
$V_{GS2} = V_{G2} - V_{S2} = V_{bias} - 1.1V = 1$

$V_{bias} = 2.1V$

Write your answer in this box

$V_{bias} =$ ________ V

b) Find $R_D$ such that the magnitude of the small-signal gain of the circuit is 1.
For your convenience the circuit and its parameters are duplicated below:
$\lambda = \gamma = 0$, $V_{TH(NMOS)}= 0.5V$, $V_{TH(PMOS)}= -0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox}=100\ \mu A/V^2$, $(W/L)_{NMOS}=40$, $(W/L)_{PMOS}= 80$, and $V_{DD}=3V$. **[5 marks]**




$$A_v = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$g_{m1} = \frac{2I_{D1}}{V_{eff1}} = \frac{2\times 1mA}{0.5} = 4mS$$

$$g_{m2} = \frac{2I_{D2}}{V_{eff2}} = \frac{2\times 1mA}{0.5} = 4mS$$

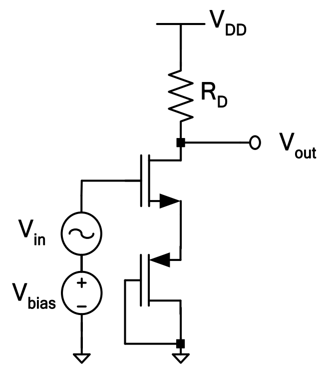
$$A_v = \frac{-R_D}{\frac{1}{4}+\frac{1}{4}} = -2R_D$$

Write your answer in this box

$R_D$= ________ Ω

$$|A_v| = 1 \Rightarrow 2R_D = 1$$
$$\Rightarrow R_D = 0.5 k\Omega$$

c) Find $R_D$ such that the magnitude of the small-signal gain of the circuit is 25.
For your convenience the circuit and its parameters are duplicated below:
$\lambda = \gamma = 0$, $V_{TH(NMOS)} = 0.5V$, $V_{TH(PMOS)} = -0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $(W/L)_{NMOS} = 40$, $(W/L)_{PMOS} = 80$, and $V_{DD} = 3V$. **[5 marks]**



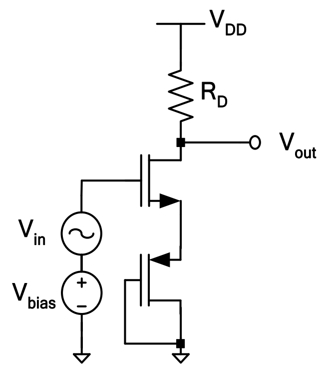

$|A_v| = 25 \Rightarrow 2R_D = 25 \Rightarrow R_D = 12.5k\Omega$

Write your answer in this box

$R_D =$ ________ $\Omega$

d) **Designer X** would argue with you that the value of $R_D$ that you have calculated in part (c) is not a good engineering choice and the gain of your circuit would not be as expected. Please state your reason whether or not you agree with **Designer X**? **[5 marks]**

For your convenience the circuit and its parameters are duplicated below:
$\lambda = \gamma = 0$, $V_{TH(NMOS)} = 0.5V$, $V_{TH(PMOS)} = -0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $(W/L)_{NMOS} = 40$, $(W/L)_{PMOS} = 80$, and $V_{DD} = 3V$.

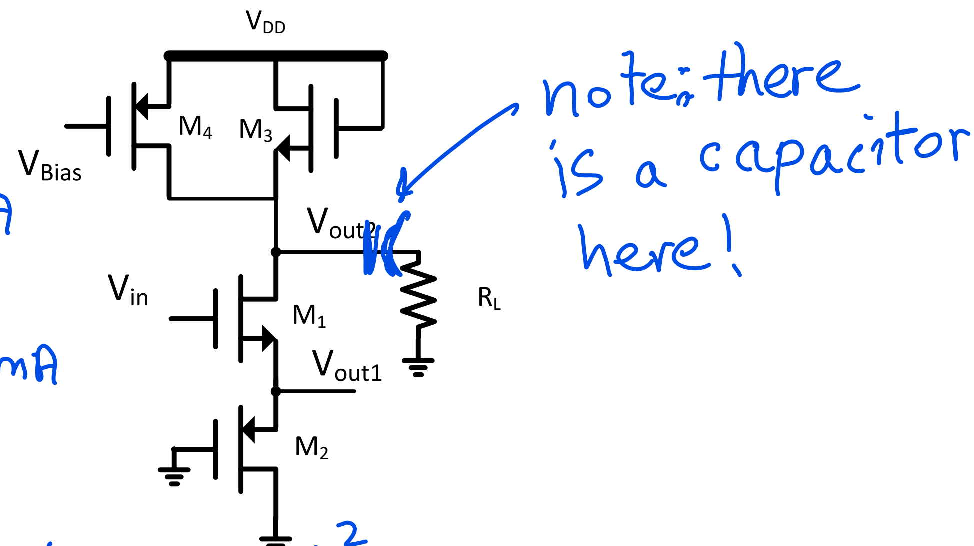



Designer X is correct, since if $R_D$ were to be 12.5kΩ then the voltage drop across $R_D$ would have been $12.5k\Omega \times 1mA = 12.5V$! which is not possible since $V_{DD}$ is 3V.

**3.** In the following circuit the DC current of M1 is 1 mA and M3 and M4 have equal DC (bias) currents. Assume all transistors are in saturation and the aspect ratio of transistors is as follows: $(W/L)_1 = 128$, $(W/L)_2 = 256$, $(W/L)_3 = 25$, and $(W/L)_4 = 50$.

The technology parameters are: $\lambda(NMOS)=\lambda(PMOS)=0$ $V^{-1}$, $V_{DD}=3.0$ V, $\gamma=0$, $V_{TH}(NMOS)=|V_{TH}(PMOS)|=0.5V$, $\mu_nC_{ox}=1$ mA/V$^2$, and $\mu_pC_{ox}=0.5$ mA/V$^2$.

a) Find DC value of $V_{out1}$, $V_{out2}$, $V_{in}$, and $V_{Bias}$. **[8 marks]**
b) Find $g_m$ of all transistors. **[4 marks]**
c) Assume $R_L=\infty$ and find the voltage gains: $V_{out1}/V_{in}$ and $V_{out2}/V_{in}$. **[4 marks]**
d) Choose $R_L$ such that $V_{out1} = -V_{out2}$. **[4 marks]**




a)

$I_{D1}=I_{D2}=1\,mA$

$I_{D3}=I_{D4}=0.5\,mA$

$I_{D4}=\frac{1}{2}\mu_pC_{ox}\left(\frac{W}{L}\right)_4(V_{SG4}-|V_{th4}|)^2$

$0.5\,mA=\frac{1}{2}0.5\frac{mA}{V^2}(50)(V_{DD}-V_{Bias}-0.5)^2 \Rightarrow (2.5-V_{Bias})^2=\frac{1}{25}$

$2.5-V_{Bias}=\pm\frac{1}{5} \Rightarrow V_{Bias}=2.5-0.2=2.3V$

$I_{D3}=\frac{1}{2}\mu_nC_{ox}\left(\frac{W}{L}\right)_3(V_{GS3}-V_{th3})^2 \Rightarrow 0.5=\frac{1}{2}1\times25(V_{DD}-V_{out2}-0.5)^2$

$(2.5-V_{out_2})^2=\frac{1}{25} \Rightarrow 2.5-V_{out_2}=\pm0.2 \Rightarrow V_{out_2}=2.3V$

negative not acceptable

$I_{D2}=\frac{1}{2}\mu_pC_{ox}\left(\frac{W}{L}\right)_2(V_{SG2}-|V_{th2}|)^2 \Rightarrow 1=\frac{1}{2}0.5(256)(V_{out_1}-0.5)^2$

$(V_{out_1}-0.5)^2=\frac{1}{64} \Rightarrow V_{out_1}-0.5=\pm0.125 \Rightarrow V_{out_1}=0.625$

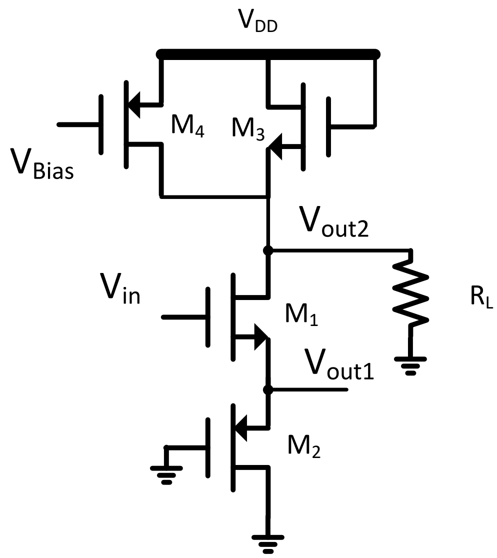
$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{th1})^2 \Rightarrow 1 = \frac{1}{2} 1 (128)(V_{in} - V_{out1} - 0.5)^2$$

$$(V_{in} - 0.625 - 0.5)^2 = \frac{1}{64} \Rightarrow V_{in} - 0.625 - 0.5 = \pm 0.125 \Rightarrow V_{in} = 1.25V$$

↑DC

For your convenience the circuit and the assumptions and circuit parameters are duplicated below:

$(W/L)_1 = 128$, $(W/L)_2 = 256$, $(W/L)_3 = 25$, and $(W/L)_4 = 50$.




The technology parameters are: $\lambda(NMOS)=\lambda(PMOS)=0$ $\mathbf{V^{-1}}$, $V_{DD}=3.0$ V, $\gamma=0$, $V_{TH}(NMOS)=|V_{TH}(PMOS)|=0.5V$, $\mu_n C_{ox}=1$ mA/V$^2$, and $\mu_p C_{ox}=0.5$ mA/V$^2$.

b)

$$g_{m1} = \frac{2I_{D1}}{V_{eff1}} = \frac{2\times1}{0.125} = 16\,mS$$

$$g_{m2} = \frac{2I_{D2}}{V_{eff2}} = \frac{2\times1}{0.125} = 16\,mS$$

$$g_{m3} = \frac{2I_{D3}}{V_{eff3}} = \frac{2\times0.5}{0.2} = 5\,mS$$

$$g_{m4} = \frac{2I_{D4}}{V_{eff4}} = \frac{2\times0.5}{0.2} = 5\,mS$$

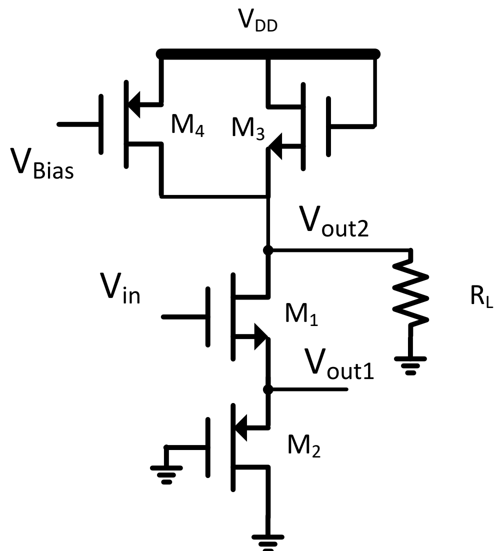
c) $R_L \to \infty$

$$\frac{V_{out1}}{V_{in}} = \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = \frac{\frac{1}{16}}{\frac{1}{16} + \frac{1}{16}} = 0.5\,V/V$$

$$\frac{V_{out2}}{V_{in}} = \frac{-\frac{1}{g_{m3}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = \frac{-\frac{1}{5}}{\frac{1}{16} + \frac{1}{16}} = -1.6\ V/V$$

For your convenience the circuit and the assumptions and circuit parameters are duplicated below:

$(W/L)_1 = 128$, $(W/L)_2 = 256$, $(W/L)_3 = 25$, and $(W/L)_4 = 50$.




The technology parameters are: λ(NMOS)=λ(PMOS)=0 $\mathbf{V^{-1}}$, $V_{DD}$=3.0 V, γ=0, $V_{TH}$(NMOS)=|$V_{TH}$(PMOS)|=0.5V, $\mu_n C_{ox}$=1 mA/$V^2$ , and $\mu_p C_{ox}$=0. 5 mA/$V^2$.

$R_L$

d) $$V_{out2} = \frac{-\left(\frac{1}{g_{m3}} \| R_L\right)}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in}$$

$$V_{out1} = \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in}$$

$$V_{out2} = -V_{out1} \Rightarrow +\left(\frac{1}{g_{m3}} \| R_L\right) = \frac{1}{g_{m2}}$$

$$\left(\frac{1}{5} \| R_L\right) = \frac{1}{16} \Rightarrow \frac{0.2 R_L}{R_L + 0.2} = \frac{1}{16} \Rightarrow 8 R_L = R_L + 0.2$$

$$R_L = \frac{0.2}{7}$$

$V_{out1\text{-}DC}$ =___________. $V_{out2\text{-}DC}$ =____________, $V_{in}$-DC=____________, $V_{Bias}$ =______________

$g_{m1}$ _____________ $g_{m2}$ =______________, $g_{m3}$ =______________ ,$g_{m4}$ =______________, $R_L = 28.6\Omega$

$V_{out1}/V_{in}$ = ___________ , $V_{out2}/V_{in}$ =___________ , $R_L$ such that $V_{out2}$= –$V_{out1}$ ___________

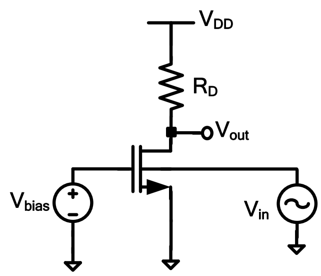
**4.** It is possible to use the <u>bulk terminal</u> of a transistor as an input of an amplifier. Consider the single-stage NMOS amplifier shown below where the small signal source $V_{in}$ is applied to the bulk node of the transistor. For $V_{bias}$=1 V:

a) What is the region of operation of the transistor? **[6 marks]**

b) Calculate the small-signal gain ($A_v=V_{out}/V_{in}$) of the amplifier. **Recall** $g_{mb}=\eta g_m$. **[8 marks]**

c) Would it be possible to resize the transistor, so that with the same circuit parameters the gain magnitude of the gain becomes 10? Why?

Assume, $\lambda = 0$, $\eta$=0.2, $V_{TH(NMOS)}$= 0.5V, $\mu_n C_{ox}$=800 $\mu A/V^2$, $R_D$=2 k$\Omega$, $(W/L)_{NMOS}$= 10, and $V_{DD}$=3V. **[10 marks]**




a) Assume the transistor is in saturation

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{Th})^2$$

$$I = \frac{1}{2}\, 0.8\,\frac{mA}{V^2}\times 10\,(1-0.5)^2 = 1\,mA$$

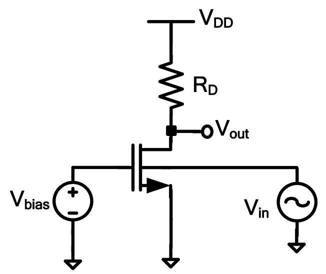
$$V_{out,DC} = V_{DD} - R_D I = 3 - 2\times 1 = 1\,V$$

$V_{GD} = 1-1 = 0 < V_{Th} \Longrightarrow$ The transistor is indeed in saturation

b)

For your convenience the circuit and the assumptions and circuit parameters are duplicated below:

Assume, $\lambda = 0$, $\eta=0.2$, $V_{TH(NMOS)}= 0.5V$, $\mu_n C_{ox}=800\ \mu A/V^2$, $R_D=2\ k\Omega$, $(W/L)_{NMOS}= 10$, and $V_{DD}=3V$. **[10 marks]**




$V_{bs}=V_{in}$

$g_m=\frac{2I_D}{V_{eff}}=\frac{2\times 1}{1-0.5}=4mS$

$\frac{V_{out}}{V_{in}}=-g_{mb}R_D$

$g_{mb}=\eta g_m=0.2\times 4=0.8\ mS$

$\frac{V_{out}}{V_{in}}=-0.8\times 2=-1.6\ V/V$

c) For increasing the gain by resizing the transistor $g_{mb}$ should be 5 or

Write your answer in this box

Region: ________

Write your answer in this box

$A_v=$ ________ V/V

c) Yes or No, because:

$g_m$ should be 25 $\Rightarrow$ $I=6.25mA$

which is not possible since the voltage drop across $R_D$ would need to be $6.25 \times 2 = 12.5V$!

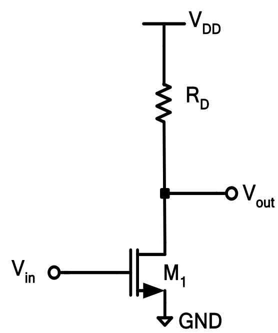
**5.** Design a common-source amplifier with a resistive load based on the schematic shown below with the following design specifications:

- $V_{DD}$=3 V
- Transistor $M_1$ is in saturation
- The minimum possible output voltage to keep $M_1$ in saturation is 0.2 V
- Total power consumption of the amplifier is 1.5 mW
- Absolute value of gain of 20
- L=0.4 μm for the transistor

The technology parameters are:

$\lambda_{(NMOS)} = 0.1$, $\gamma = 0$, $V_{DD}$=3 V, $V_{TH(NMOS)} = 0.4$ V, $\mu_n C_{ox}$=1 mA/V$^2$ .

**Note:** Use λ only for calculating the $r_o$ of the transistor. **Do not** use λ in any other calculation including your bias currents (for biasing consider λ to be 0).




Find the following values:

1) DC level (bias voltage) of the input **[4 marks]**
2) Width ($W_1$) of transistor $M_1$ **[4 marks]**
3) $R_D$ **[4 marks]**
4) Nominal dc level (bias level) of the output node **[4 marks]**
5) Maximum output signal swing for a symmetric output signal **[4 marks]**

1) Minimum output voltage to keep $M_1$ in saturation is 0.2V

$\Rightarrow V_{eff} = 0.2V \Rightarrow V_{in,DC} - V_{th} = 0.2v \Rightarrow V_{in,DC} = 0.6V$

2) $P = 1.5$ mW $\Rightarrow V_{DD} I = 1.5$mW $\Rightarrow I = \frac{1.5}{3} = 0.5$ mA

$I = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{eff})^2 \Rightarrow 0.5 = \frac{1}{2} \times 1 \frac{mA}{V^2} \left(\frac{W}{L}\right) (0.2)^2 \Rightarrow \frac{W}{L} = 25$

$W = 25L = 10 \mu m$

3) $A_v = g_m (R_D || r_o) \Rightarrow 20 = \frac{2I}{V_{eff}} (R_D || r_o)$

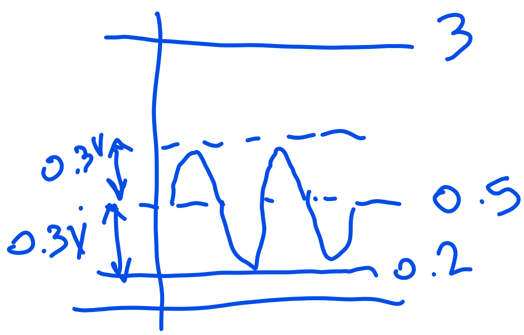
$R_D || r_o = 4$ kΩ $\quad r_o = \frac{1}{\lambda I_D} = \frac{1}{0.1 \times 0.5} = 20$kΩ

$$\frac{20 \times R_D}{20 + R_D} = 4 \Rightarrow 20R_D = 80 + 4R_D$$

$$16R_D = 80 \Rightarrow R_D = 5k\Omega$$

4) $V_{out,DC} = V_{DD} - R_D I = 3 - 5 \times 0.5 = 0.5V$

5)




Maximum symmetric swing:
amplitude: 0.3V
peak to peak: 0.6V

DC level of input= ___________V, $W_1$=___________μm, $R_D$=___________kΩ,

Nominal output DC level=__________V, Maximum symmetric output swing=________V

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