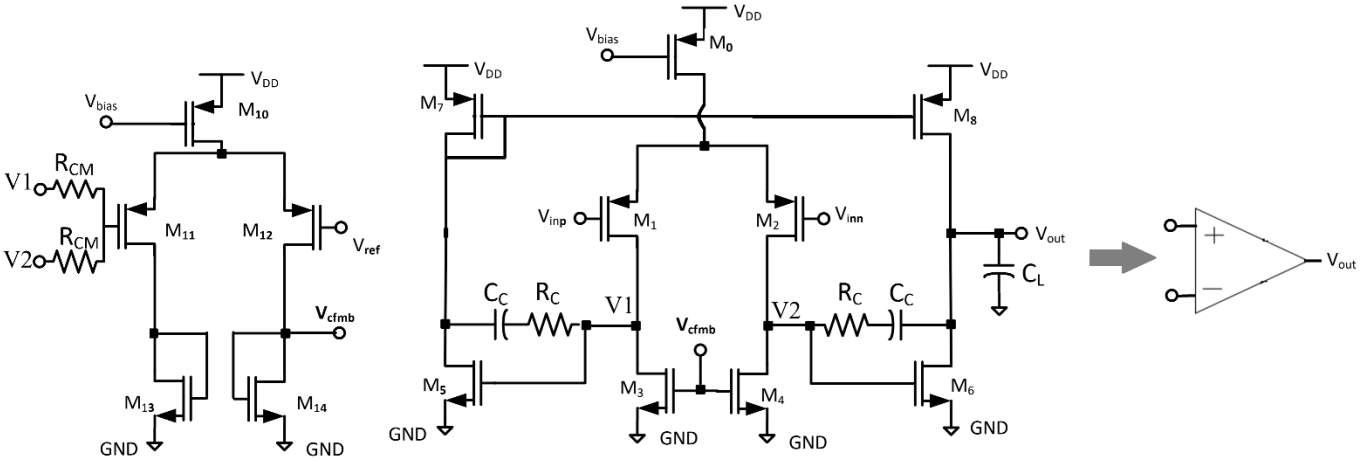
ELEC 401 Analog CMOS Integrated Circuit Design
Design Project: Two-Stage Opamp Design
Due: Monday, December 22nd, 2025, by 11:59 pm

Design and simulate a two-stage differential to single-ended operational amplifier based on the following topology in the 45-nm CMOS process (the PDK is available through ssh-soc.ece.ubc.ca server and instruction on how to access it can be found on our Canvas web page).



The Design specifications are summarized in the following table:

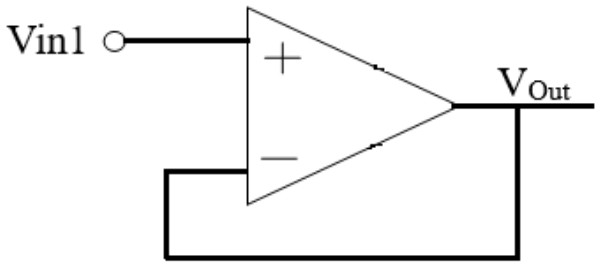
V_{DD}	1.0 V
GND	0 V
C_L	2 pF
Nominal input common-mode (input DC level)	$V_{DD}/2$
Nominal output common-mode (output DC level)	$V_{DD}/2$
two-stage power consumption	$\leq$ 0.4 mW
CMFB circuit power	$\leq$ 40 µW
Differential output Swing	$\geq$ 0.75 V
Low-frequency differential gain	$\geq$ 46 dB
Small-signal unity gain frequency	$\geq$ 600 MHz
Phase Margin	$\geq 60° \& \leq 90°$
Slew rate	$\geq$ 20 V/µs
Maximum length of transistors (L_{min}=45 nm)	$5\times L_{min}$
Maximum width per Multiplier	4 µm
Maximum Multiplier of transistors	50

Note that you may or may not need R_C for the compensation. The output common-mode of first stage has to be set using the simple common-mode feedback circuit that is shown in the schematic (with power less than 40uW). R_{CM}=1 MΩ, and assume that other than supply voltage, V_{DD} = 1 V, you have access to two other voltage sources, namely, V_{ref} between 0 to V_{DD} (this is used as a reference voltage for the common-mode feedback system circuit and can vary based on your design) and V_{bias} of any fixed value between 0 to V_{DD} which is used for biasing the gate of the M_0, M_7, M_8,and M_{10}. To avoid body effect at the input of the opamp, connect the body of PMOS transistors M_1 and M_2 to their respective source terminal. Similarly, connect the body of PMOS transistors M_{11} and M_{12} to their respective source terminals. The body of all the other PMOS transistors is connected to V_{DD} and the body of all the NMOS transistors is connected to ground (GND).

You may use low-threshold-voltage devices (e.g., nmos1v_LVT and pmos1v_LVT). Note that the gpdk_45 models exhibit incorrect behavior when using fingers. Do not use fingered devices. Instead, keep Fingers = 1 and increase the multiplier M (integer values only) whenever additional effective width is needed to ensure that the device width per multiplier does not exceed 4 µm.

- For your project report, please prepare a document that includes a brief report on how you designed your circuit, a table summarizing the performance results of your opamp (required and achieved), summary of your hand calculations and a brief description of your design approach.
- Required plots: including the bode plot of open-loop transfer function on which achieved phase margin and low-frequency gain are annotated, bode plot of closed-loop system on which the 3-dB frequency of the closed-loop system is indicated, and provide the plots of the step responses, and any comments and conclusions. Please also include the schematic of your design with transistor sizes and component values indicated on the schematic (transistor sizes and component values should be indicated beside each transistor/component, respectively).
- Run a DC simulation, annotate the node voltages and device currents, and include screenshots in the report. This is required to demonstrate that all transistors are operating in the saturation region.
- Apply a 0.1MHz differential sinusoidal input to the open-loop circuit with an appropriately small amplitude to avoid distortion at the output. Increase the amplitude gradually and show the transient waveform corresponding to the maximum undistorted output swing. In the report, clearly state the input amplitude at which this maximum undistorted swing is achieved.
- Also, include any other supporting document(s) or plot(s) that you would like to hand in. Please include these items in one file and submit it through our Canvas web page.

Closed loop :
Use the designed opamp in the unity gain buffer configuration that is shown below. Do not remove the load capacitance C_L of the amplifier.



- Plot the frequency response of this structure as well as the transient response for four different input steps with the common-mode of 0.5 V and peak-to-peak value of 10 mV (V_{in1} a step from 0.495 V to 0.505 V), –10 mV (V_{in1} a step from 0.505 V to 0.495 V), 1 V (0 to 1 V), and –1 V (1 to 0 V). Measure and report the small-signal 10 to 90% settling time (that is, the time required for the output to reach from 10% to 90% of its final value) and the large-signal initial rising/falling slopes of the output (i.e., slew rate).

Bonus:

1) Instead of using V_{bias} and V_{ref} design a supply independent biasing circuit and a simple voltage divider that generate V_{bias} and V_{ref}, respectively. Note that the power consumption of the overall opamp including the biasing circuitry and the voltage divider should be less than 0.5 mW.

2) Design your opamp such that the specifications are met even if the supply voltage varies by ±10%. (show the results for Vdd =1.1V and 0.9V)

How to prepare your report:

Please prepare your report with the following structure. Begin with a brief description of your design objectives, methodology, and overall performance. Then, include a table that presents all required specifications alongside the achieved results. The introduction should provide a clear and technical explanation of your design approach. Please include the power-budget distribution, the rationale behind your bias choices and selected effective voltages, the gain calculation for each stage, finding the dominant poles, and explanation of the CMFB architecture and the compensation scheme.

When presenting results, ensure that your sequence follows a logical flow. Start with the DC operating-point screenshot, properly annotated with node voltages and device currents to confirm that every transistor remains in saturation. After this, present both the open-loop and closed-loop AC simulations, highlighting gain, bandwidth, phase margin, and any other relevant frequency-domain characteristics. The transient results should follow, including the maximum undistorted output swing, settling behavior, and any plots that you may include.

Please keep your report succinct and ensure that, including the figures, it does not exceed 20 pages.

Good luck!