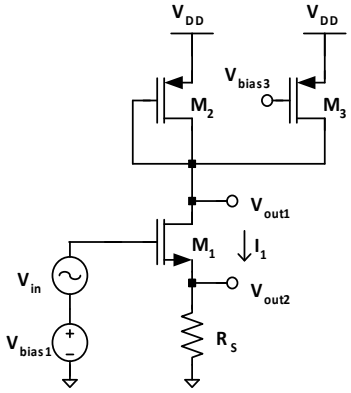
ELEC 401 Analog CMOS Integrated Circuit Design
Assignment 2
Due: Tuesday, October 21, 2025 at 11:59 pm

1. In the following circuit assume that all transistors are operating in the saturation region. Also, assume that $\lambda=\gamma=0$, $V_{DD}=3V$, $V_{bias3}=1.9V$, $V_{TH(NMOS)}=0.5V$, $V_{TH(PMOS)}=-0.6V$, $\mu_nC_{ox}=200\ \mu A/V^2$, $(W/L)_1 = 40$, $\mu_pC_{ox}=100\ \mu A/V^2$, $(W/L)_2 = 40$, $(W/L)_3 = 40$, and $R_S=50\Omega$.



a) Find V_{bias1} such that the bias current of M_1 is I_1=1mA.
b) Calculate the small-signal voltage gain $A_{V1}=V_{out1}/V_{in}$.
c) Calculate the small-signal voltage gain $A_{V2}=V_{out2}/V_{in}$.
d) Calculate the small-signal output impedance seen at the output nodeV_{out1}.
e) Calculate the small-signal output impedance seen at the output nodeV_{out2}.

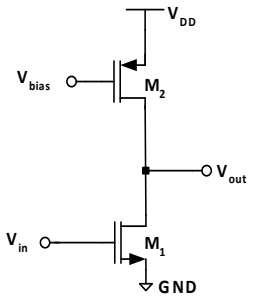
2. Design a common-source amplifier with a current source load based on the topology shown below with the following design specifications:

- V_{DD}=3 V
- Total power consumption of 1.5 mW
- Peak to peak output signal swing of 2.5 V
- Absolute value of gain of 40
- L = 0.4 μm for all the devices

Use the following assumptions for your design

- The nominal dc level of the output node is 1.5 V

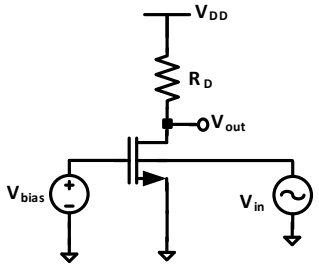
The technology parameters are:
$\lambda_{(NMOS)} = 0.1\ V^{-1}$, $\lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{TH(NMOS)} = 0.5V$ and $V_{TH(PMOS)} = -0.5V$, $\mu_nC_{ox} = 0.2\ mA/V^2$, $\mu_pC_{ox} = 0.1\ mA/V^2$.
Note: Use the parameter λ only for calculating the small-signal output resistance (r_o) of the transistors. Do not use λ in any other calculation including the bias current calculations.



Find V_{bias}, DC level of the input, the transistor widths (i.e., W_1 and W_2), and the gain of the circuit.

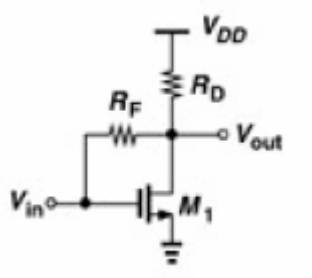
3. It is possible to use the bulk terminal of a transistor as an input of an amplifier. Consider the single-stage NMOS amplifier shown below. For V_{bias}=1.5V:
a) What is the region of operation of the transistor?
b) Calculate the small-signal gain ($A_v=V_{out}/V_{in}$) of the amplifier. **Recall** that $g_{mb}=\eta g_m$.

Assume, $\lambda = 0$, η=0.2, $V_{TH(NMOS)}$= 0.5V, $\mu_n C_{ox}$=100 $\mu A/V^2$, R_D=1kΩ, $(W/L)_{NMOS}$= 20, and V_{DD}=3V.



4. Note: In this problem you do not need to use any numerical value for the process parameters. If needed express your answers in terms of R_D, R_F and/or transistor small-signal parameters g_m and r_o.

In the following circuit, assuming the MOSFET is in active region:



a) Calculate the small-signal voltage gain (assume $\lambda \neq 0$).
b) Find the value of R_F for which the gain of the circuit is +1.
c) Find the value of R_F for which the gain of the circuit is -1.
d) State any condition that may be required so that the R_F calculated in part c is realizable.

Good luck!