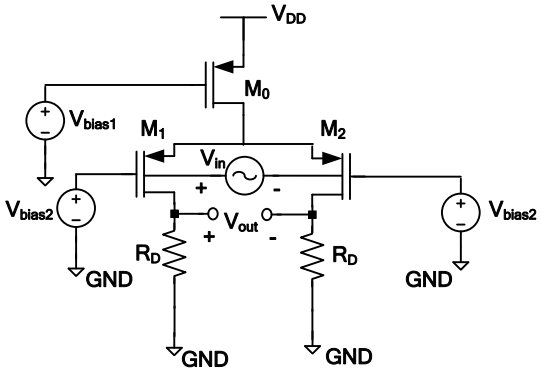
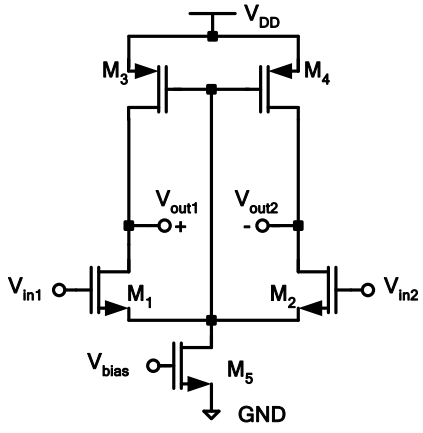
**ELEC401 Analog CMOS Integrated Circuit Design**
**Assignment 3**
**Due: Tuesday, November 4th, 2025 at 11:59 pm**

**1.** Consider the following differential amplifier where the small-signal input is applied to the bulk of $M_1$ and $M_2$. For $V_{bias1}$=1.4V, and assuming that $V_{bias2}$ is properly chosen so that all transistors are operating in their saturation region, calculate the small-signal differential gain of the amplifier.

Recall that $g_{mb}= \eta g_m$.
Assume, $\lambda = 0$, $\eta$=0.2, $|V_{TH(PMOS)}|$= 0.6V (the threshold value is in the presence of body effect), $\mu_p C_{ox}$=100 μA/V$^2$, $R_D$=1kΩ, $(W/L)_0$= 40, $(W/L)_1$=$(W/L)_2$= 20, and $V_{DD}$=3V.




**2.** In the following circuit all transistors have a W/L of 7μm/0.35μm and $M_3$ and $M_4$ are to operate in deep triode region with an on-resistance of 2k Ω. Assume: $I_5 = 40$ μA and $\lambda = \gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = 0.5$ V, $V_{TH(PMOS)} = -0.6$ V, $\mu_n C_{ox}$=200 μA/V$^2$, $\mu_p C_{ox}$=100 μA/V$^2$.



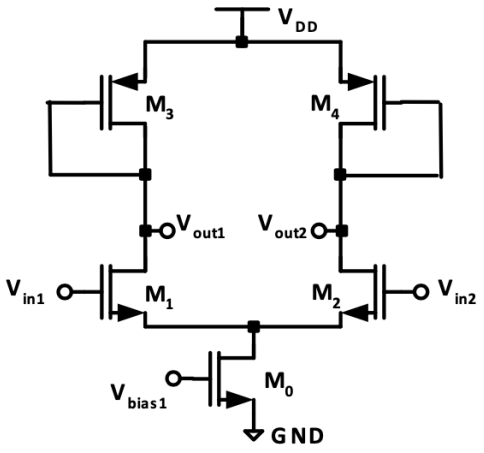

a) Calculate the dc level of the input (input common-mode level) that yields such on-resistance.
b) Calculate the small-signal differential gain, i.e., $(V_{out1}-V_{out2})/(V_{in1}-V_{in2})$, of the circuit when the input common-mode level is equal to value calculated in part a.

**3.** Design a symmetric differential amplifier based on the topology shown below with the following design specifications:

- $V_{DD}$=3.0 V
- Total power consumption of 3.0 mW
- Output DC level of 1.5 V
- Differential gain of 40 V/V
- L=0.4 μm for all devices

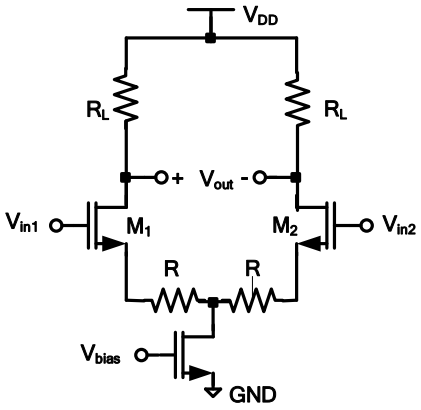
Assume that the minimum required voltage at the drain of $M_0$ to keep it in saturation is 0.2 V.

The technology parameters are:
$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $\gamma=0$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=1mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.




a) Find $V_{bias1}$, and all the transistor widths (i.e., $W_0$,$W_1$, $W_2$, $W_3$, and $W_4$).
b) Find the minimum and maximum allowable input common-mode (input DC) levels.

**4.** Consider the following differential amplifier.




Assume all transistors are operating in saturation region and $\lambda=\gamma=0$, $V_{DD}=3$ V, $V_{TH(NMOS)}=0.5$ V, $\mu_n C_{ox}=1$ mA/V$^2$, R=100 Ω, $(W/L)_1=(W/L)_2=16$ and $(W/L)_0=32$. Also, assume that the $V_{bias}=0.75$ V and the circuit is symmetric.

a) What should the value of $R_L$ be if the magnitude of the differential voltage gain of the circuit is 4 V/V.
b) For the circuit to operate properly (i.e., all transistors operate in their saturation region), what are the minimum and maximum values of the input common-mode voltage (i.e., input DC voltage)

**Good luck.**