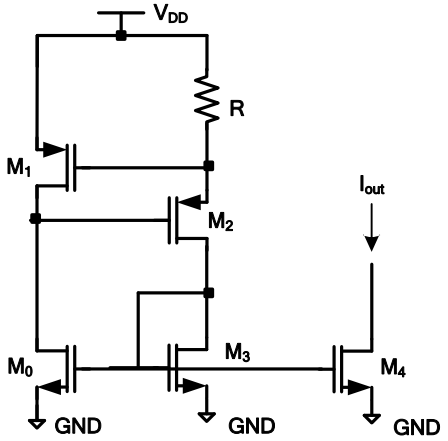
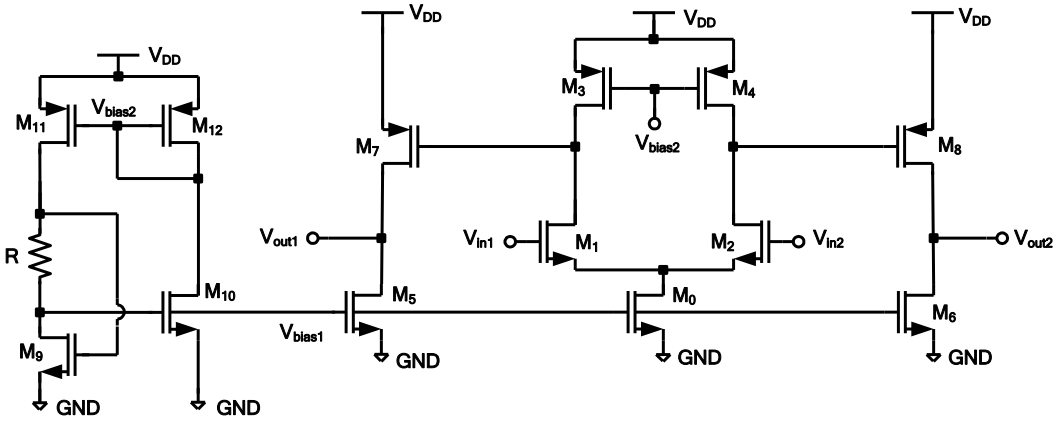
ELEC 401 Analog CMOS Integrated Circuit Design
Assignment 4
Due: Tuesday, December 2nd, 2025 at 11:59pm

1. Consider the following circuit. (This circuit is sometimes referred to as a self-biased current source).



Assume all transistors are operating in saturation region and $\lambda=\gamma=0$, $V_{DD}=3$ V, $V_{TH(NMOS)}=0.5$ V, $V_{TH(PMOS)}=-0.5$ V, $\mu_n C_{ox}=200\ \mu A/V^2$, and $\mu_p C_{ox}=100\ \mu A/V^2$. Also, assume that M_0, M_3 and M_4 have the same aspect ratio.
Given that $I_{out}=50\ \mu A$ and $(W/L)_1=16$**,** find R.

2. Design a two-stage differential amplifier based on the topology shown below:



Use the following design specifications (Note that the gate of M_{12} is also connected to the gate of M_3):

- $V_{DD}=1.8$V
- Total power consumption of 1.98 mW
- Total gain of 4000
- L=0.4 μm for all the devices
- $W_{11}=W_{12}$
- $W_{10}=4W_9$
- R=1 kΩ

Furthermore, assume:

- The op-amp circuit is symmetric
- The bias currents of the first stage and second stage are equal (i.e., $I_0=I_5+I_6$) and I_{11} is 10% of I_0.
- The magnitude of overdrive voltages of M_4, M_6, and M_8 are equal

The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.1V^{-1}$, $\gamma = 0$, $V_{DD}=1.8V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4V$, $\mu_nC_{ox}=1\ mA/V^2$, $\mu_pC_{ox}=0.5\ mA/V^2$.

Note: Use the parameter λ only for calculating the r_o of the transistors. **Do not** use λ in any other calculation including your bias currents.

Find all transistor widths (namely, W_0,W_1, W_2, W_3, W_4, W_5, W_6, W_7, W_8, W_9, W_{10}, W_{11} and W_{12}).

Good luck!