ELEC 401: Analog CMOS Integrated Circuit Design

Introduction

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Marking

Assignments **10%**

4 to 6 assignments.

Midterms **25%**

Two in class midterms: October 23rd and November 13th, 2025.

Project **20%**

Design project will be released in the first half of November.

Final Exam **45%**

References

- Main reference: Lecture notes

- Recommended Textbook:

📖 Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 1st or 2nd edition, 2001 or 2016

- Some other useful references:

📖 T. Chan Carusone, D. Johns and K. Martin, *Analog Integrated Circuit Design*, 2nd Edition, John Wiley, 2011

📖 P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, John Wiley, 2009

📖 D. Holberg and P. Allen, *CMOS Analog Circuit Design*, 3rd Edition, Oxford University Press, 2011

📖 A. Sedra and K.C. Smith (and T. Chan Carusone and V. Gaudet), *Microelectronic Circuits*, 5th, 6th, 7th, or (8th) Edition, Oxford University Press, 2004, 2009, 2014, 2020

📖 Journal and conference articles including *IEEE Journal of Solid-State Circuits* and *International Solid-State Circuits Conference*

Fun to Watch and Check

Razavi Electronics 1 - YouTube (45 Lectures)

Razavi Electronics 2 – YouTube (46 Lectures)

William F. Brinkman, Douglas E. Haggan, and William W. Troutman, "A History of the Invention of the Transistor and Where It Will Lead Us," *IEEE Journal of Solid-State Circuits*, volume 32, no. 12, December 1997, pp. 1858-1865

Over 6 Decades of Continued Transistor Shrinkage, Innovation (intel.com)

Mark Bohr 2014 IDF Session Presentation (intel.com)

Boris Murmann, "Digitally Assisted Analog Circuits," IEEE Micro, vol. 26, no. 2, pp. 38-47, Mar. 2006.

Fun to Read

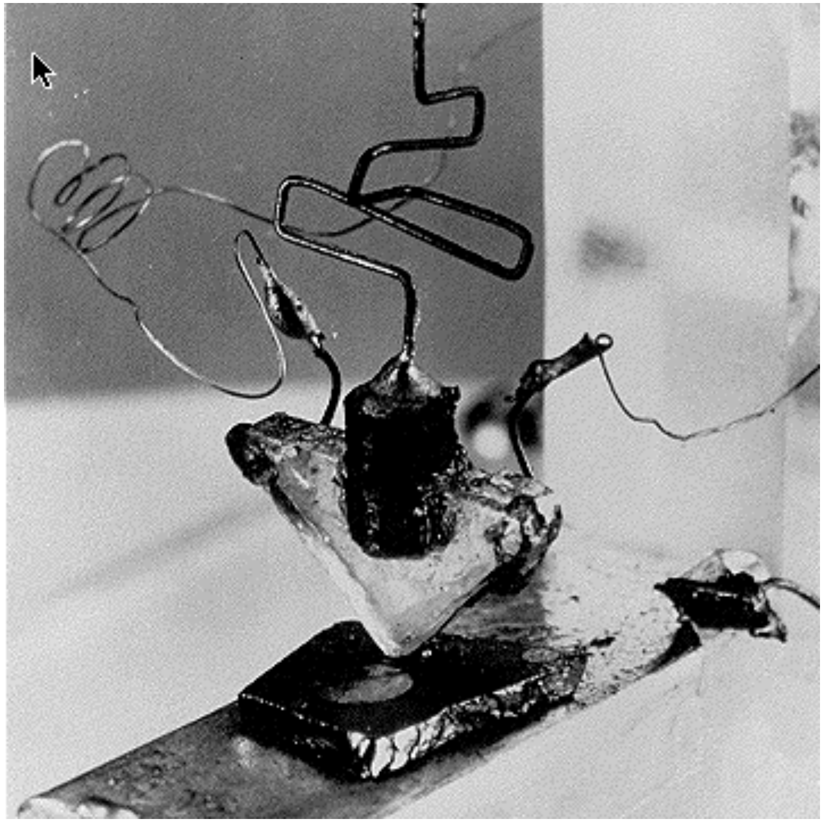
IEEE Solid-State Circuits Magazine, in particular

- Circuit Intuitions A series of articles prepared by Professor Ali Sheikholeslami and published in IEEE Solid-State Circuits Magazine that provide insights and intuitions into circuit design and analysis.

- "The Analog Mind": A recurring technical column published in the IEEE Solid-State Circuits Magazine, authored by Profesosr Behzad Razavi, focusing on the intuitive and creative processes behind analog circuit design.

Transistor Era

First Transistor invented in Bell Labs (1947)

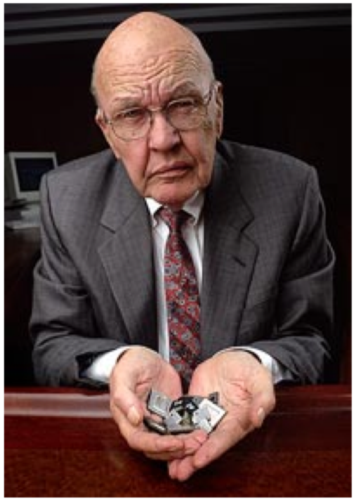


Dr. John Bardeen (left), Dr. Walter Brattain (right), and Dr. William Shockley (center).

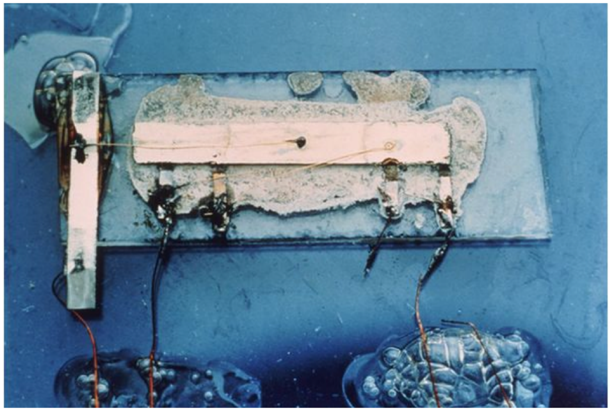
Awarded Nobel Prize in Physics in 1956

First Integrated Circuit

- **Credit for the first integrated circuit is given to Jack S. Kilby (together with Robert Noyce) while working for Texas Instrument (1958)**
- **Kilby won the Nobel Prize in Physics in 2000 for his contributions to the invention of integrated circuits.**

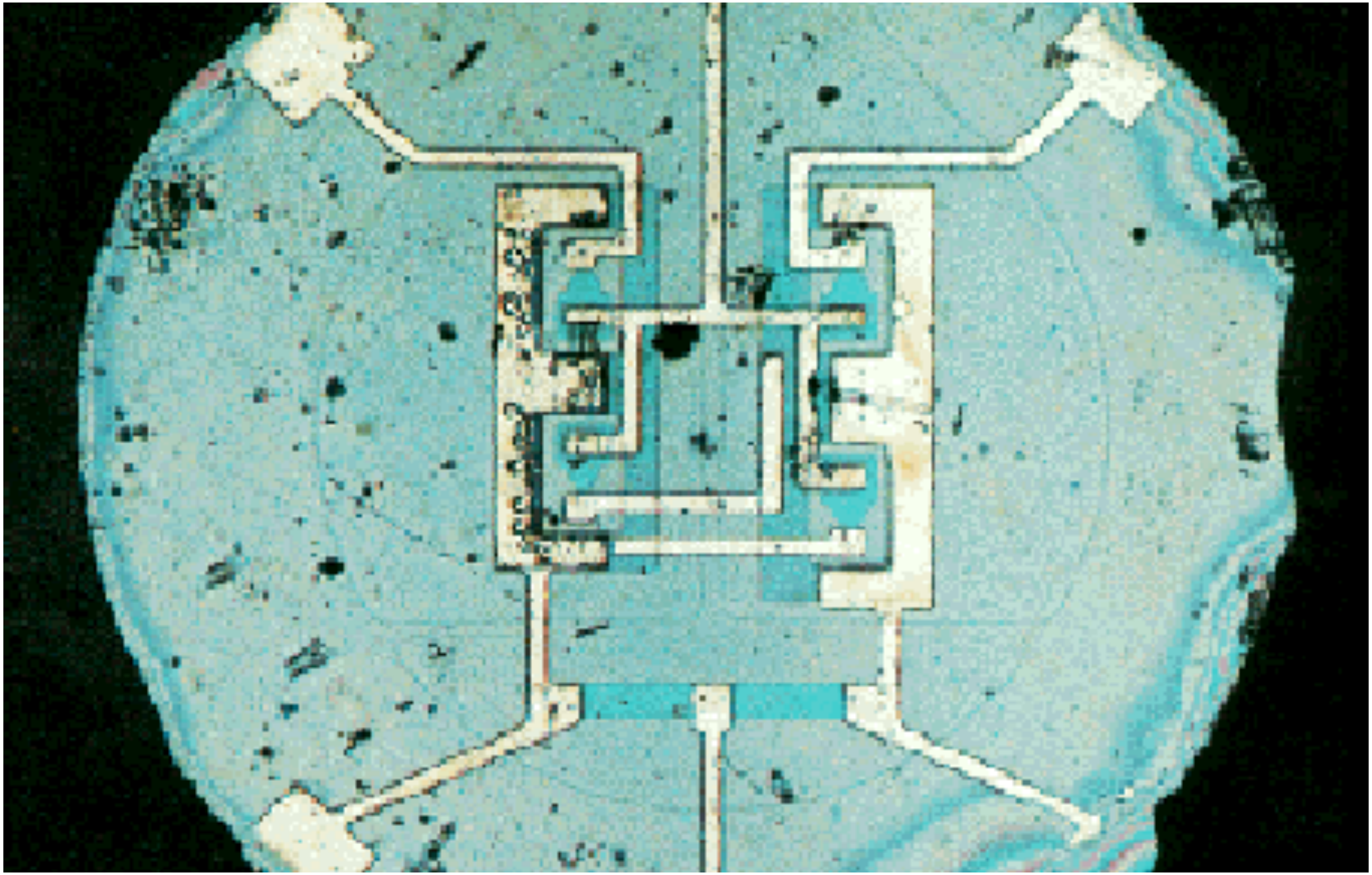


Jack Kilby

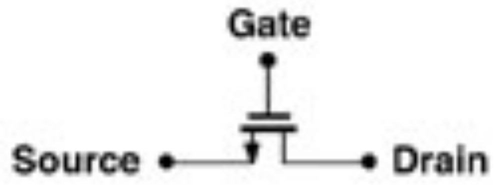


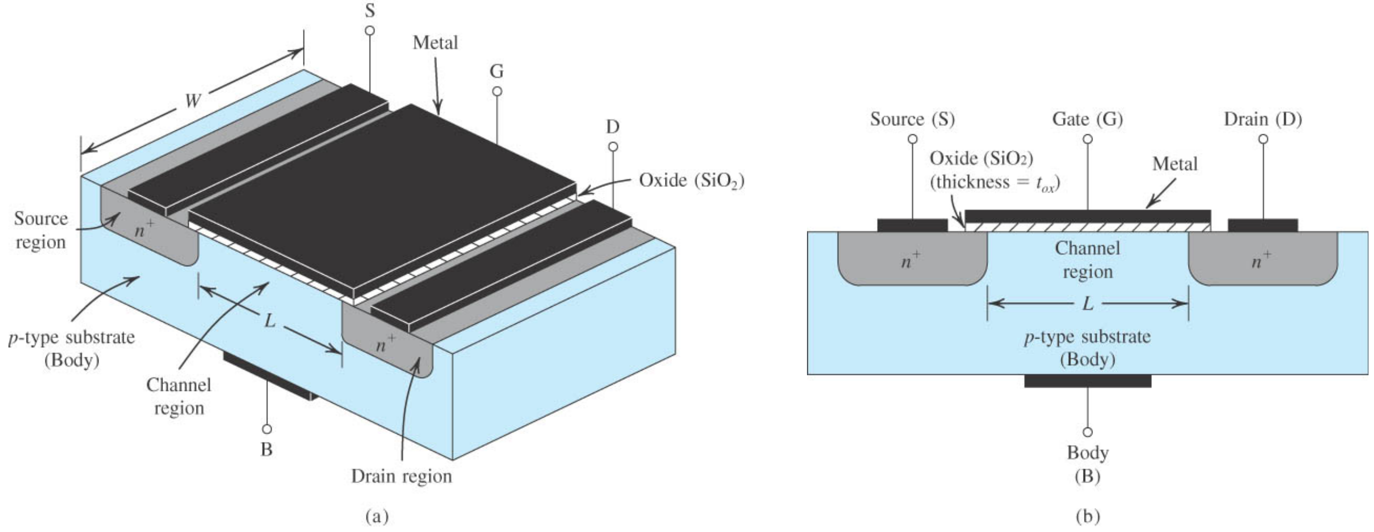
Robert Noyce

First Planar Integrated Circuit (1961)



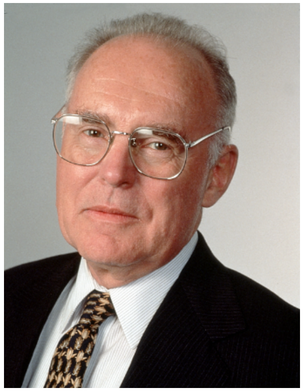
Sneak Preview of a MOS Transistor





Moore's Law

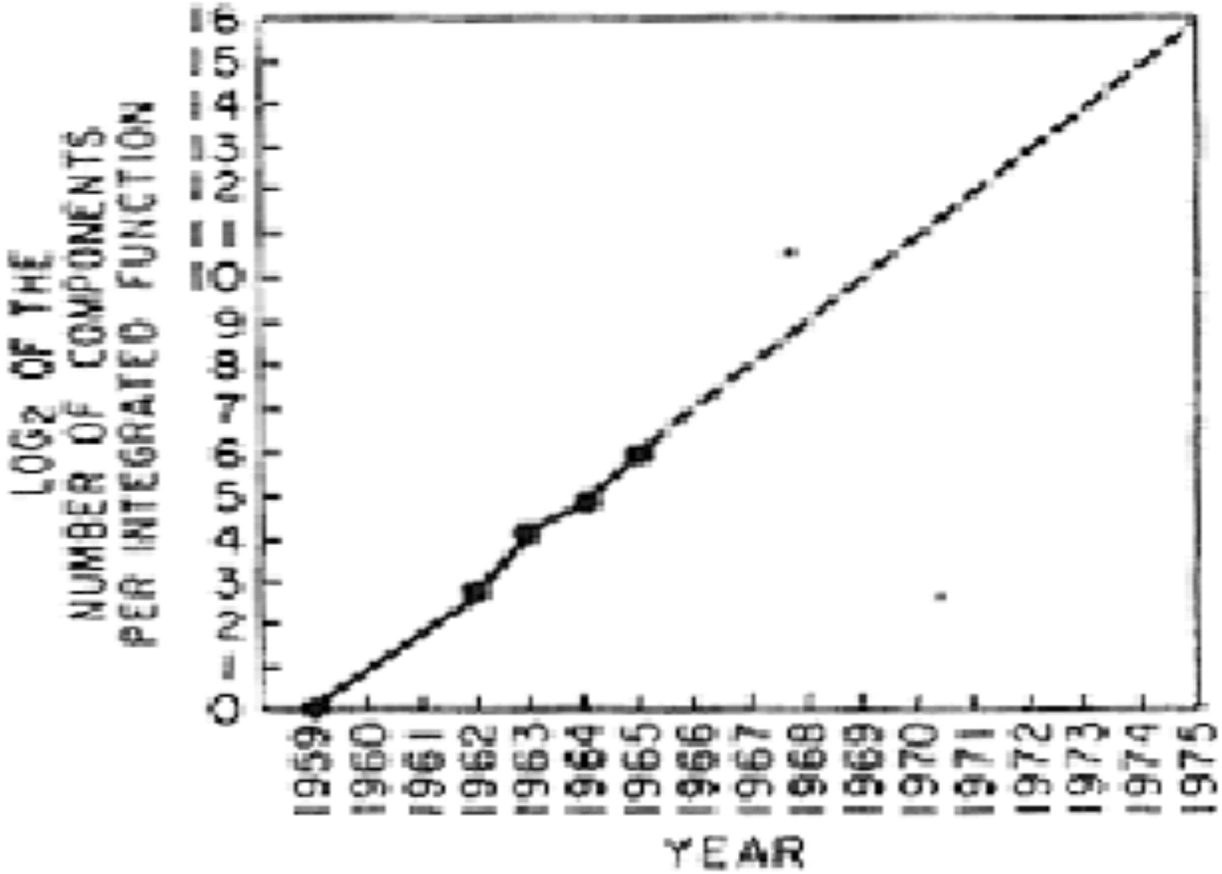
- Named after observation of Gordon Moore (born in 1929), co-founder of Intel



- Around 60 years ago, Moore observed that the number of transistors that could be placed on a chip is doubled every 1.5 to 2 years.

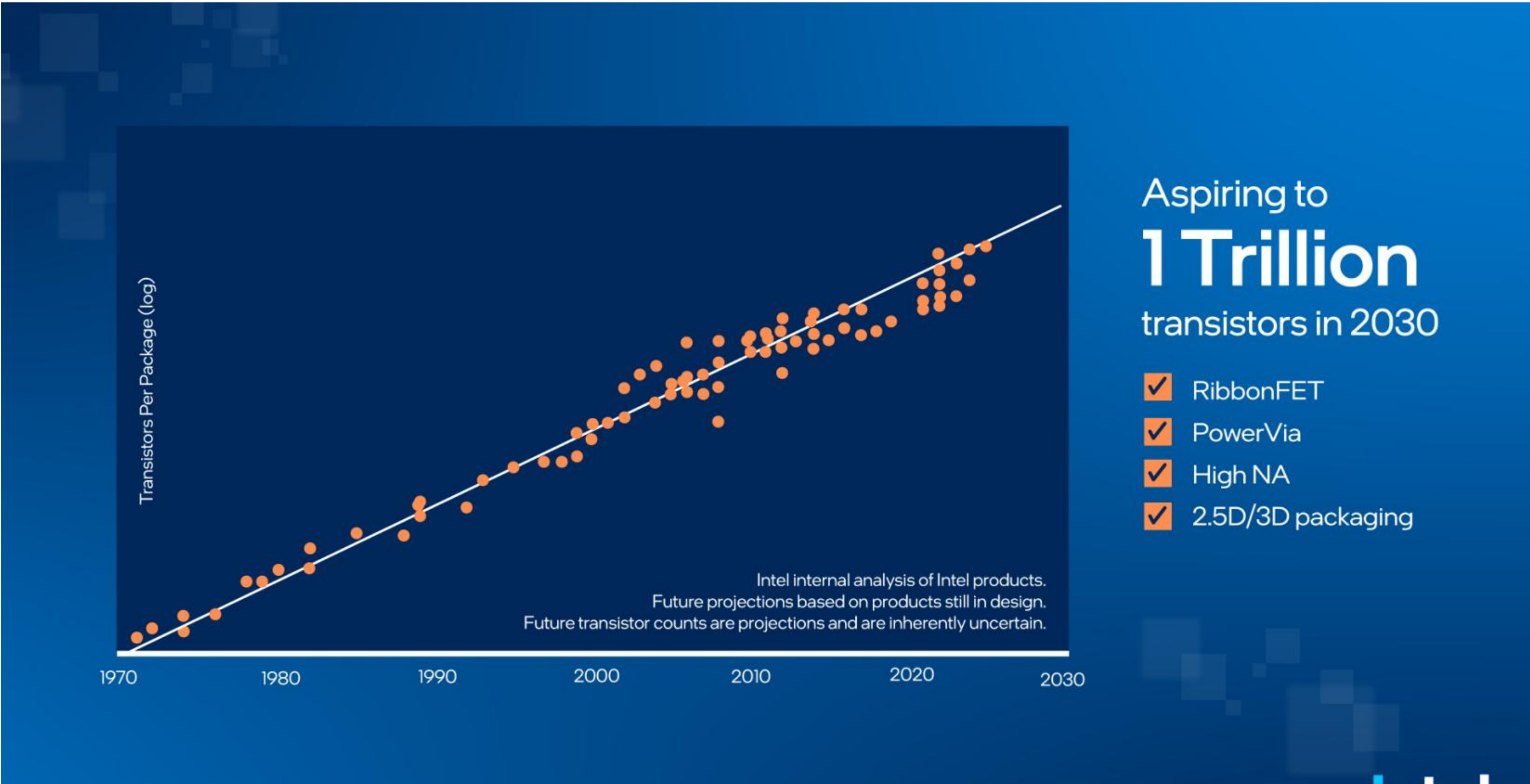
- He predicted that this growth trend will continue and indeed it has been continued to the present.

Moore's Law



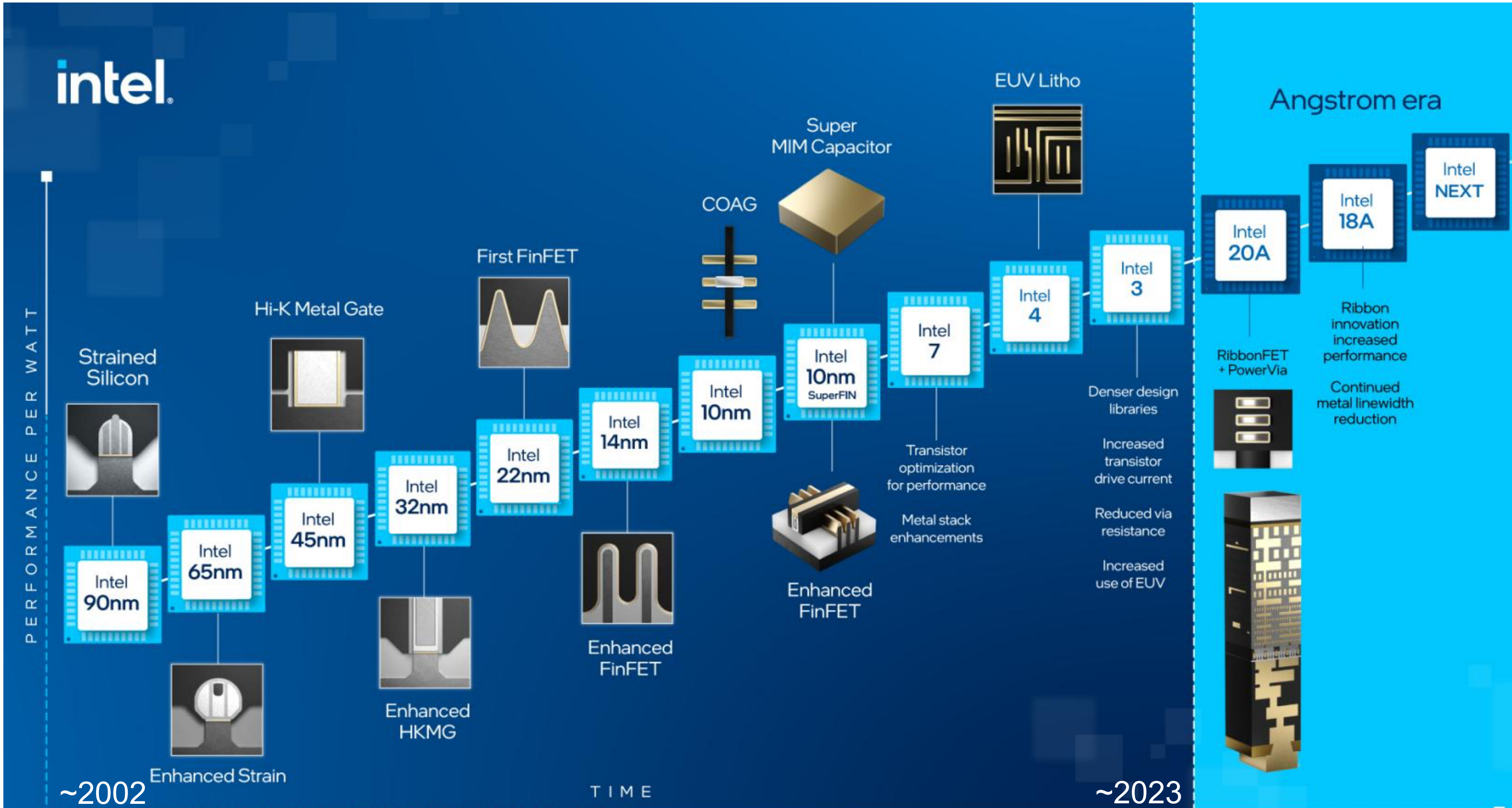
Source: Electronics, Volume 38, Number 8, April 19, 1965

Moore's Law



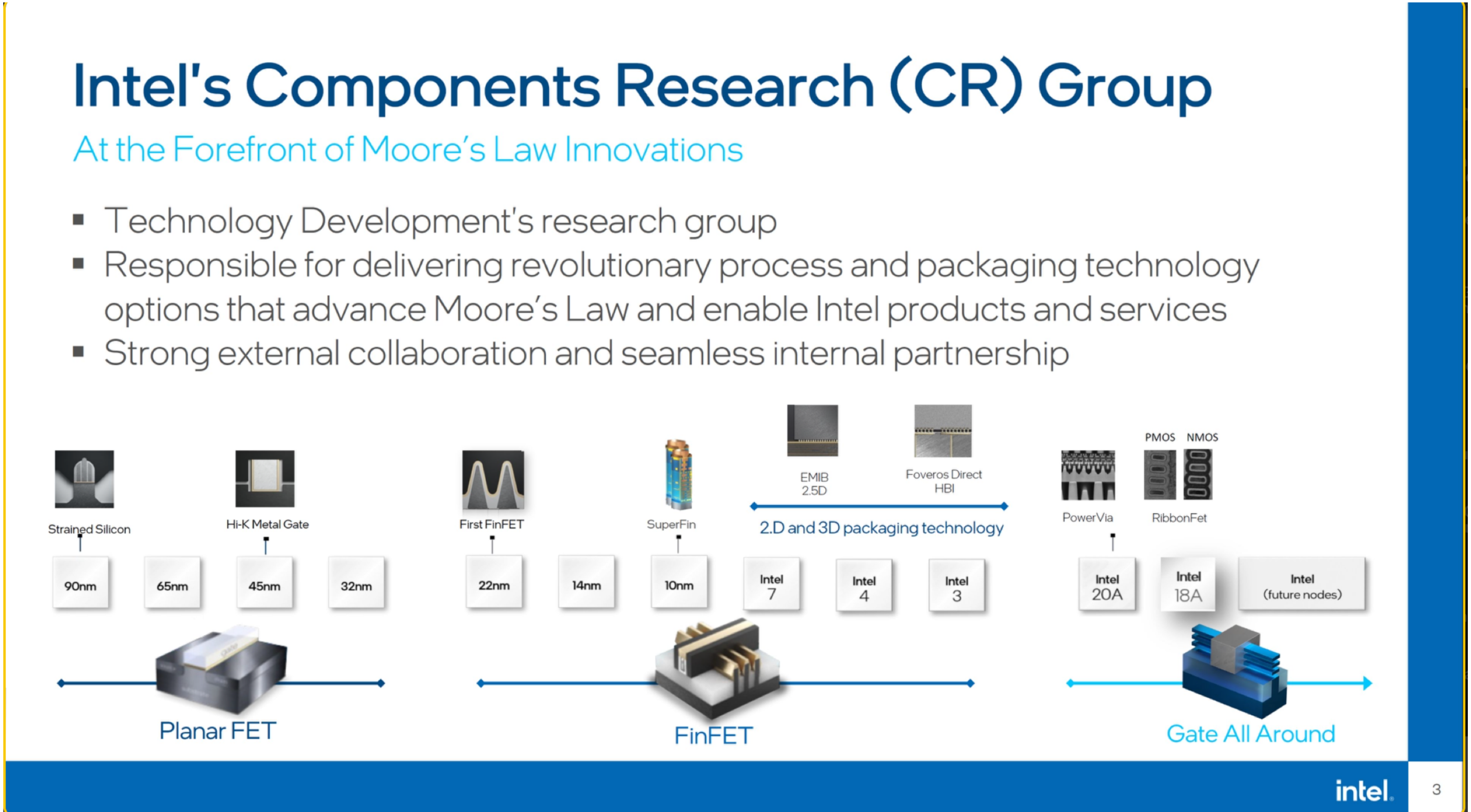
Source: "Moore's Law – Now and in the Future," www.intel.com

Moore's Law



Source: "Moore's Law – Now and in the Future," www.intel.com

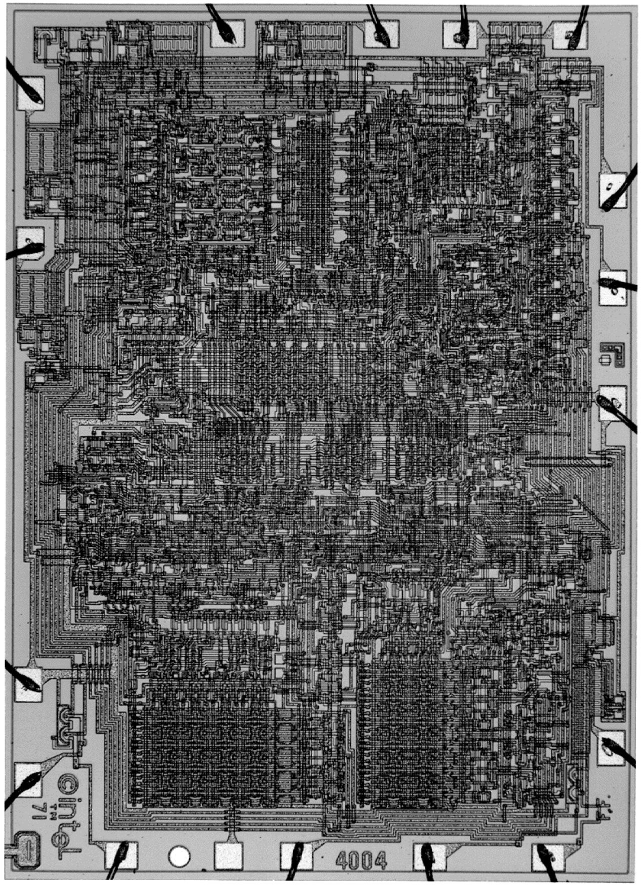
Moore's Law



Intel's Components Research (CR) Group
At the Forefront of Moore's Law Innovations
▪ Technology Development's research group
▪ Responsible for delivering revolutionary process and packaging technology options that advance Moore's Law and enable Intel products and services
▪ Strong external collaboration and seamless internal partnership
Strained Silicon
Hi-K Metal Gate
First FinFET
SuperFin
EMIB 2.5D
Foveros Direct HBI
2.D and 3D packaging technology
PowerVia
PMOS
NMOS
RibbonFet
90nm
65nm
45nm
32nm
22nm
14nm
10nm
Intel 7
Intel 4
Intel 3
Intel 20A
Intel 18A
Intel (future nodes)
Planar FET
FinFET
Gate All Around
intel.
3

First Microprocessor

Intel's 4004 (1971) with 2250 transistors in a 12mm^2 area (10-μm)



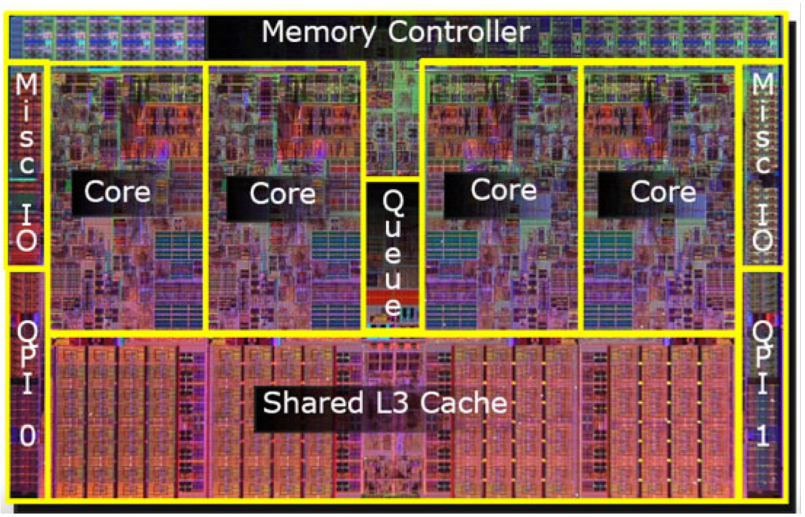
Pentium 4

42,000,000 transistors in a ~170mm^2 area

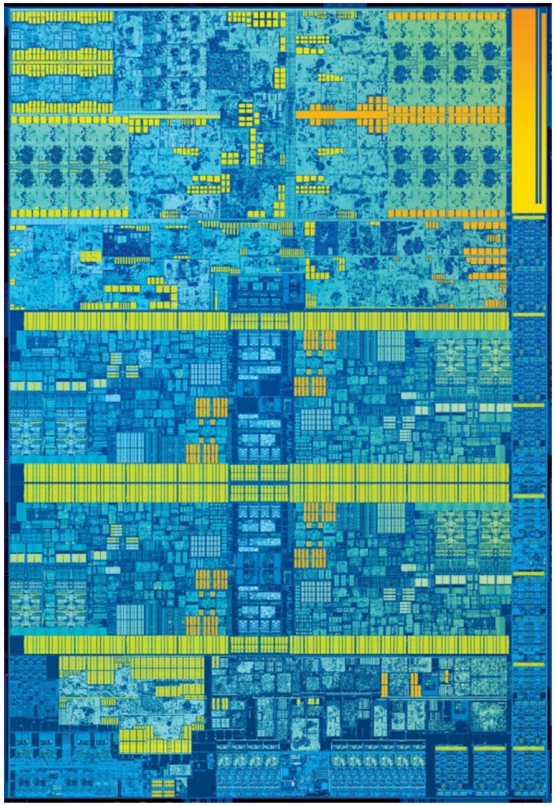
0.18-μm Technology (1999)

0.13-μm Technology (2001)

Intel Core i7



2010

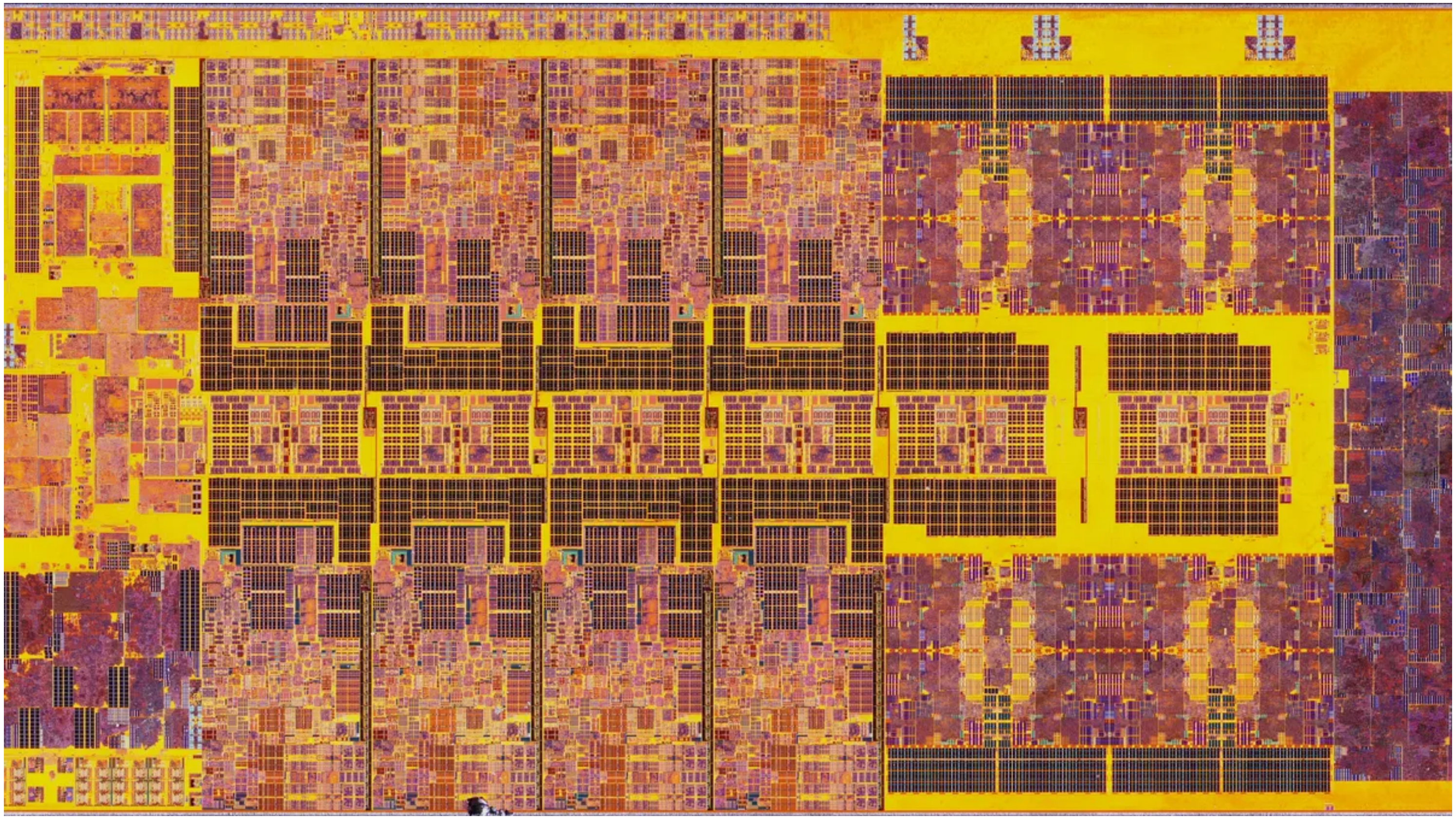


2015

14 nm CMOS, 1,700,000,000 transistors

Intel Core i9

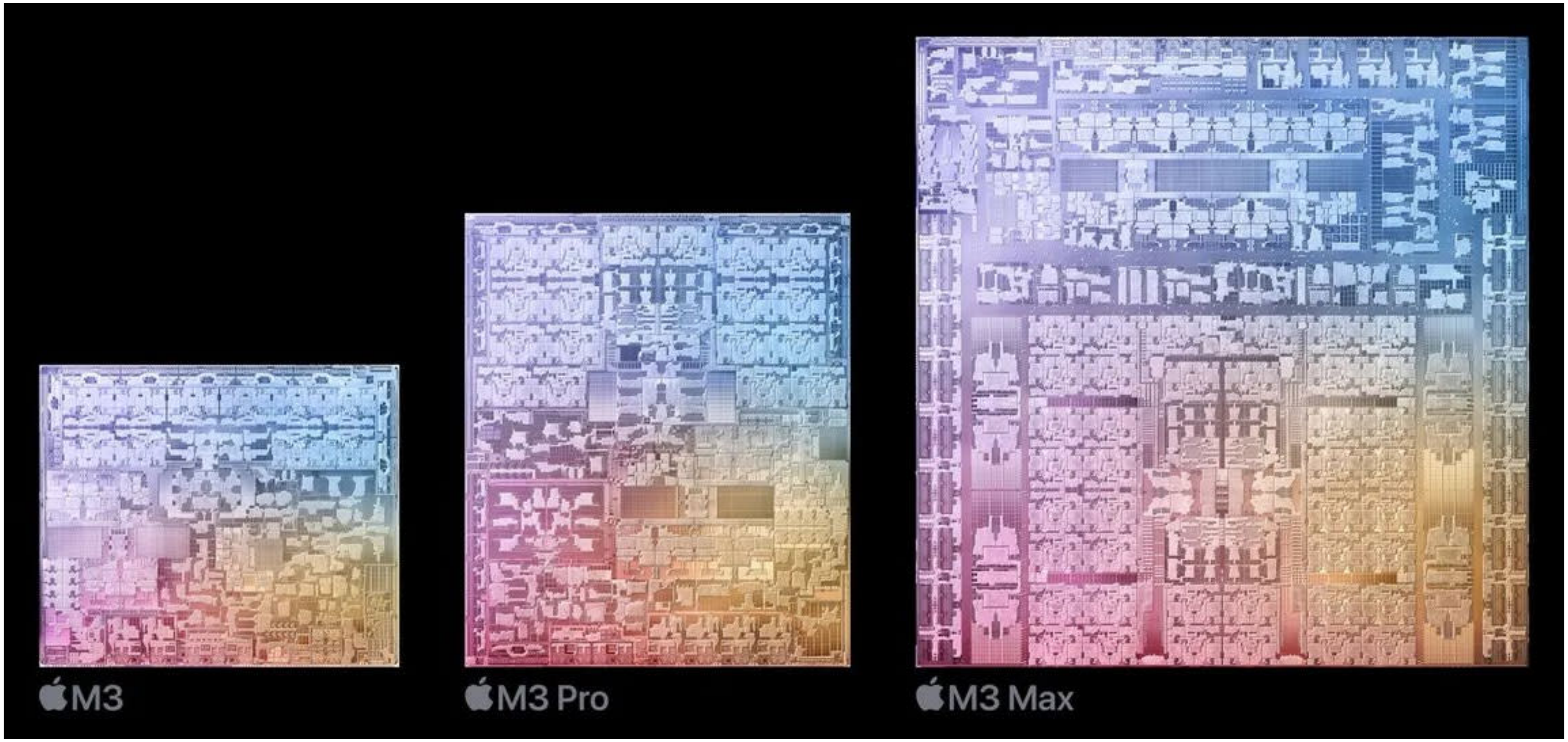
Intel Core i9-13900K (10 nm CMOS, ~252 mm^2, ~25.9 billion transistors)



2022

(Image credit: Fritzchens Fritz)

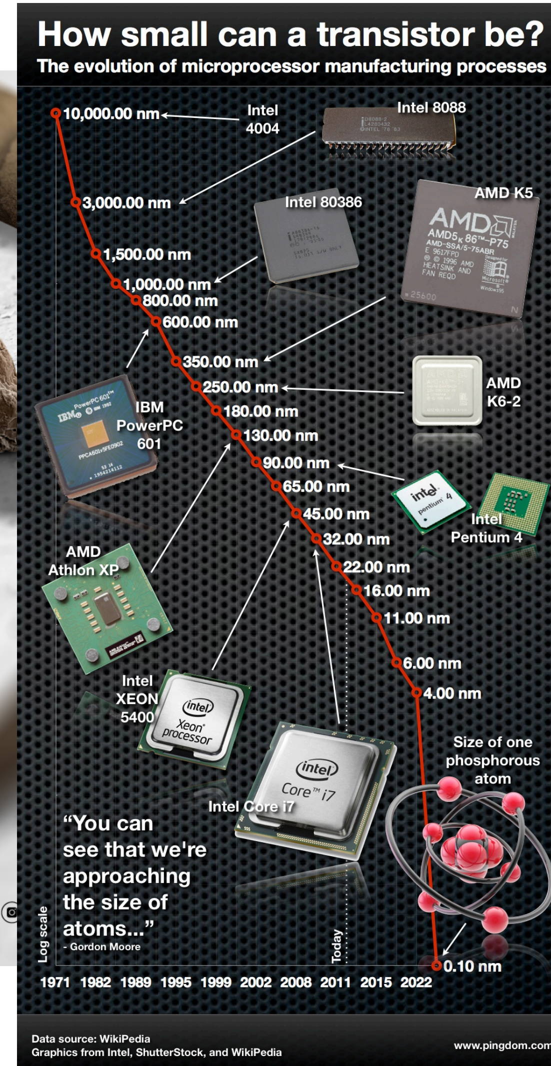
Apple M3 in 3-nm CMOS



25 billion transistors (2023). 37 billion transistors (2023). 92 billion transistors (2023)

M3 Ultra (2025) has 184 billion transistors,.

THE RELATIVE SIZE
OF PARTICLES
From the COVID-19 pandemic to the U.S. West Coast wildfires, some of the biggest threats now are also the most microscopic.
A particle needs to be 10 microns (µm) or less before it can be inhaled into your respiratory tract. But just how small are these specks?
Here's a look at the relative sizes of some familiar particles
HUMAN HAIR 50-180µm
FOR SCALE
FINE BEACH SAND 90µm
GRAIN OF SALT 60µm
WHITE BLOOD CELL 25µm
GRAIN OF POLLEN 15µm
DUST PARTICLE (PM10) <10µm
RED BLOOD CELL 7-8µm
RESPIRATORY DROPLETS 5-10µm
DUST PARTICLE (PM2.5) 2.5µm
BACTERIUM 1-3µm
WILDFIRE SMOKE 0.4-0.7µm
CORONAVIRUS 0.1-0.5µm
T4 BACTERIOPHAGE 0.225µm
ZIKA VIRUS 0.045µm
Pollen can trigger allergic reactions and hay fever—which 1 in 5 Americans experience every year.
Source: Harvard Health
The visibility limits for what the naked eye can see hovers around 10-40µm.
Respiratory droplets have the potential to carry smaller particles within them, such as dust or coronavirus.
Wildfire smoke can persist in the air for several days, and even months.
VISUAL CAPITALIST
/visualcapitalist

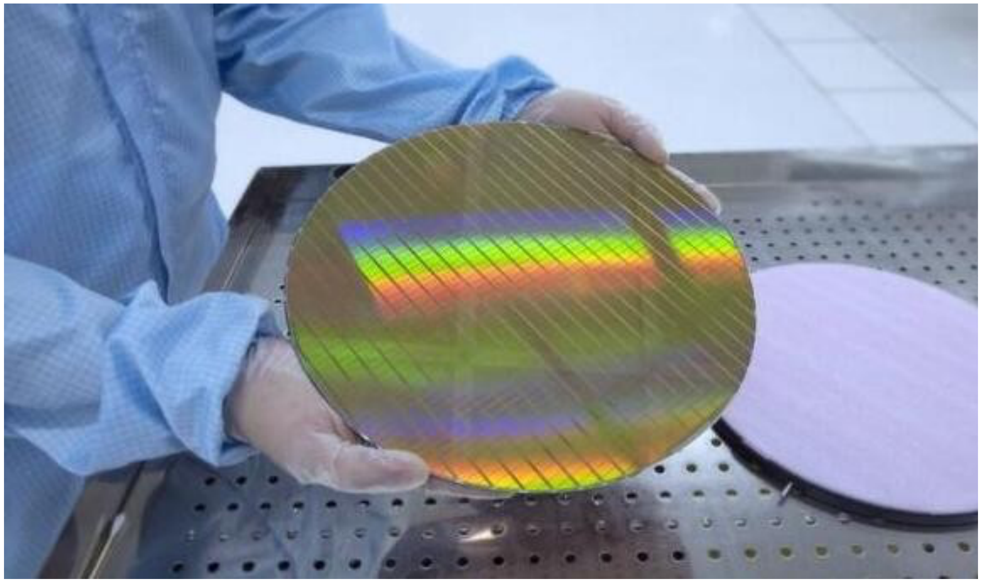


How small can a transistor be?
The evolution of microprocessor manufacturing processes
10,000.00 nm
3,000.00 nm
1,500.00 nm
1,000.00 nm
800.00 nm
600.00 nm
350.00 nm
250.00 nm
180.00 nm
130.00 nm
90.00 nm
65.00 nm
45.00 nm
32.00 nm
22.00 nm
16.00 nm
11.00 nm
6.00 nm
4.00 nm
0.10 nm
Intel 4004
Intel 8088
Intel 80386
AMD K5
IBM PowerPC 601
AMD K6-2
Intel Pentium 4
AMD Athlon XP
Intel XEON 5400
Intel Core i7
Size of one phosphorous atom
"You can see that we're approaching the size of atoms..."
- Gordon Moore
Log scale
Today
1971 1982 1989 1995 1999 2002 2008 2011 2015 2022
Data source: WikiPedia
Graphics from Intel, ShutterStock, and WikiPedia
www.pingdom.com

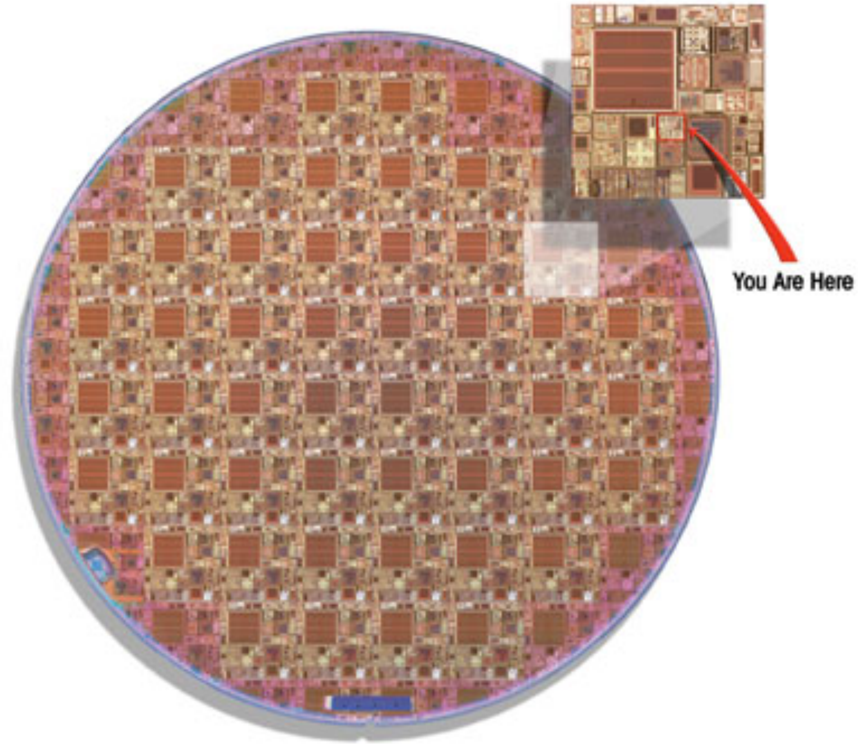
Technology Scaling and Roadmap (Intel)

Source: "Moore's Law – Now and in the Future," www.intel.com

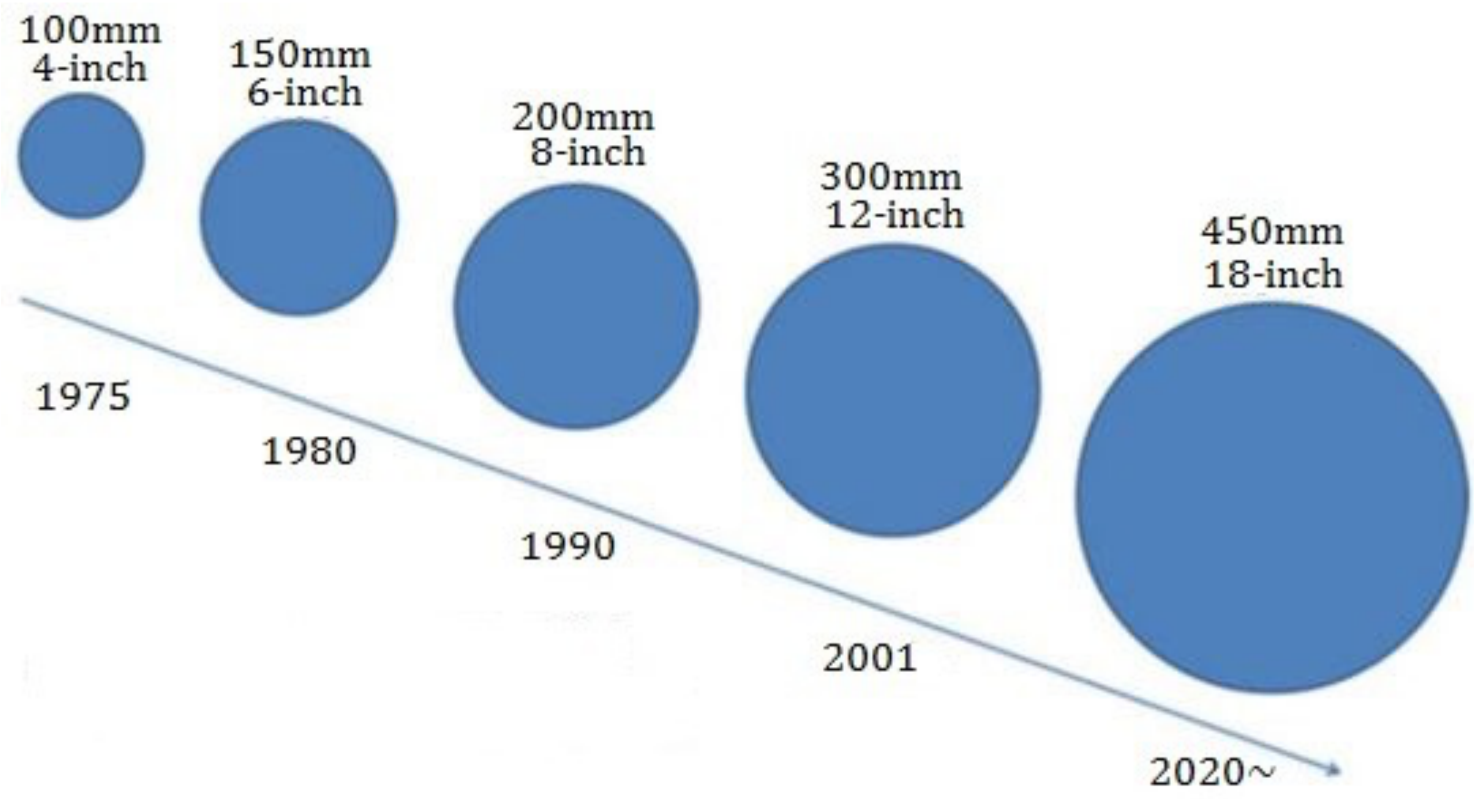
CMOS Wafer



(Image credit Kuke Electronics Limited)



A typical multiproject wafer from Mosis accommodates the needs of integrated device manufacturers and fabless semiconductor companies.

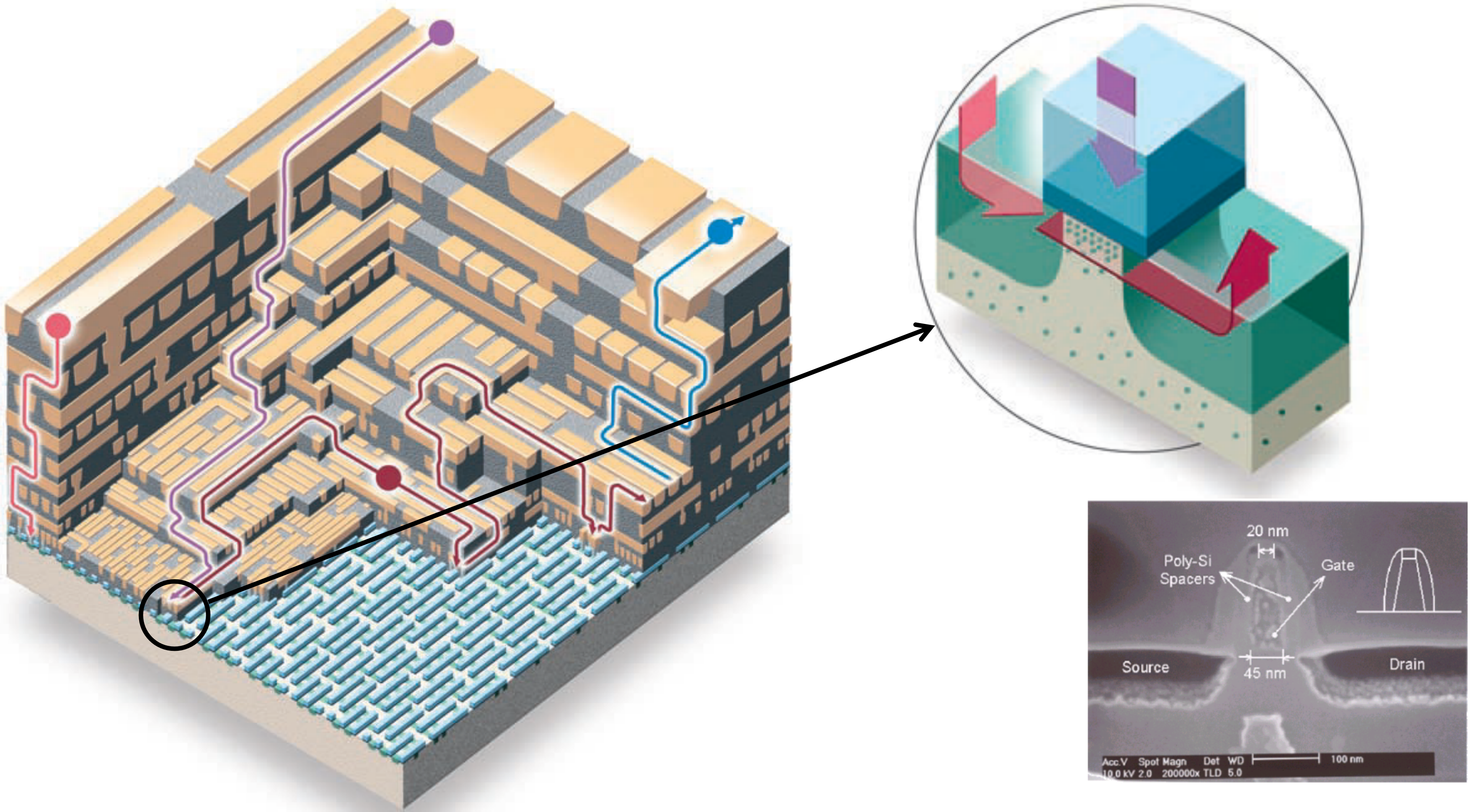


Source: Kuke Electronics Limited

CMOS Wafer

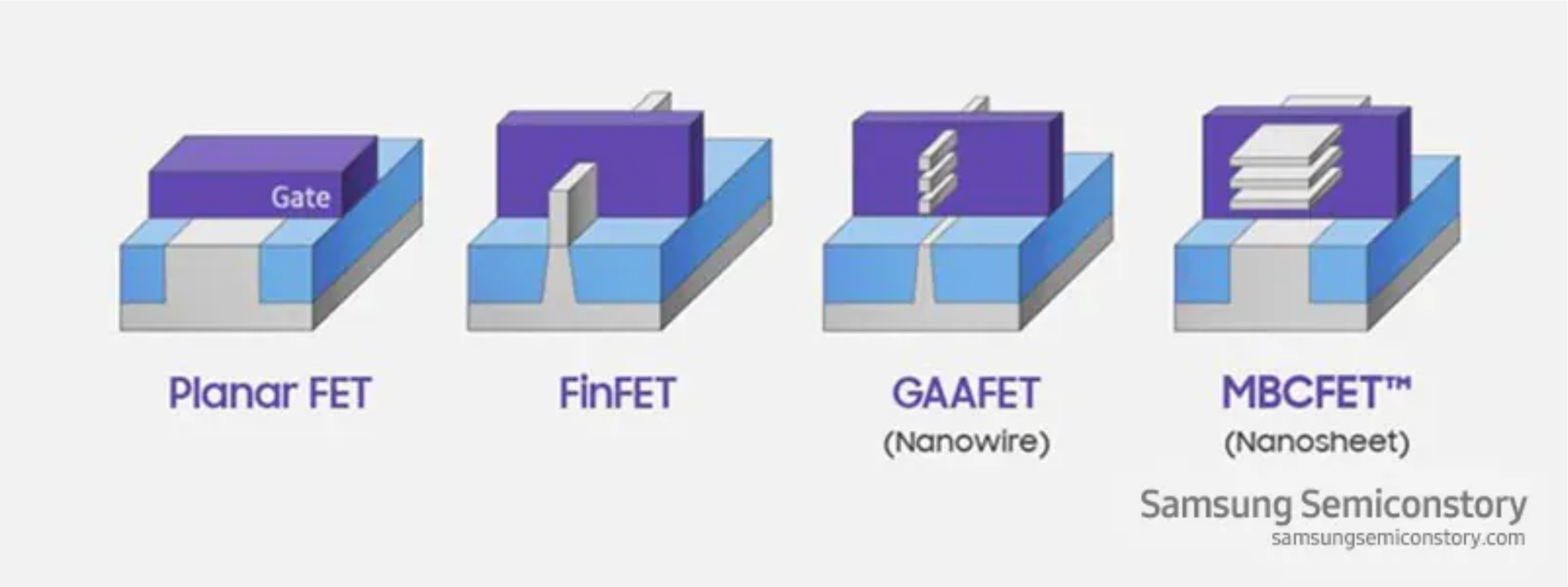
Source: https://ece.vt.edu/news/article/life-beyond-silicon

Intel 45 nm Process



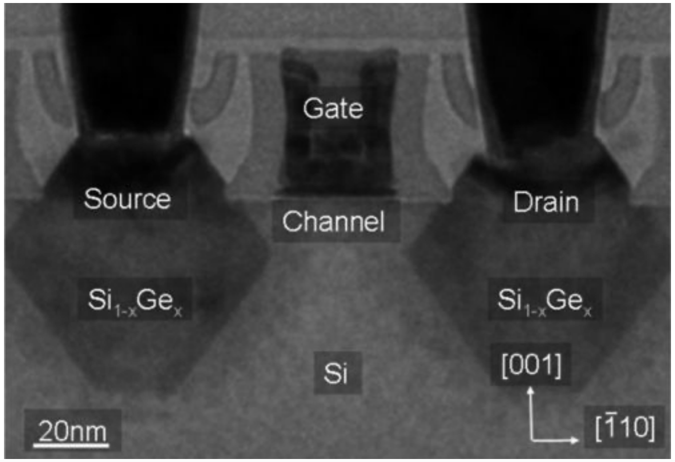
http://blog.oregonlive.com/siliconforest/2007/11/intel11.pdf

Planar to 3D Structures

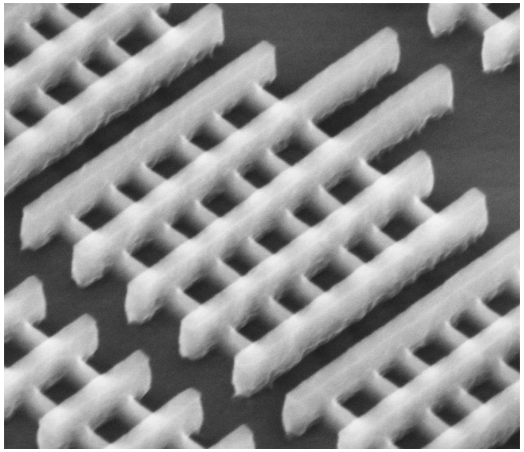


https://semiconductor.samsung.com/

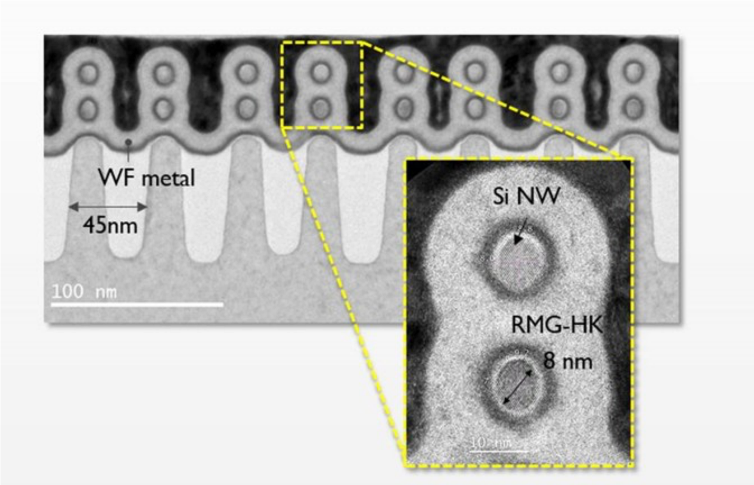
FinFET



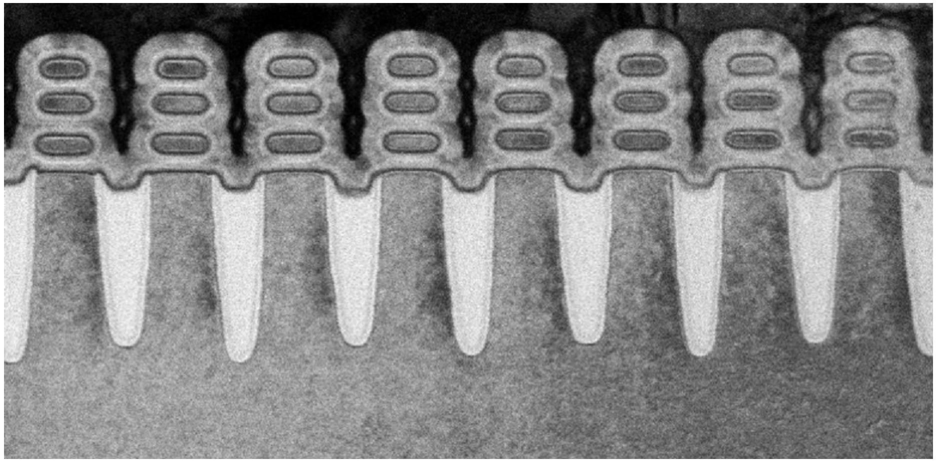
Source: Wiley, Analytical Science



Source: Intel



Source: Imec

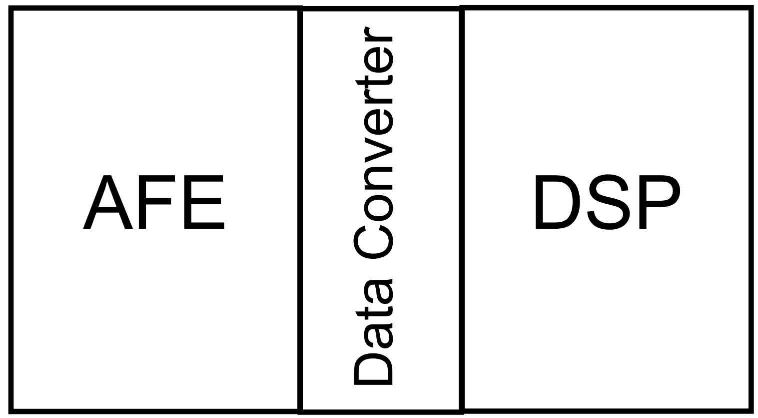


Source: IBM

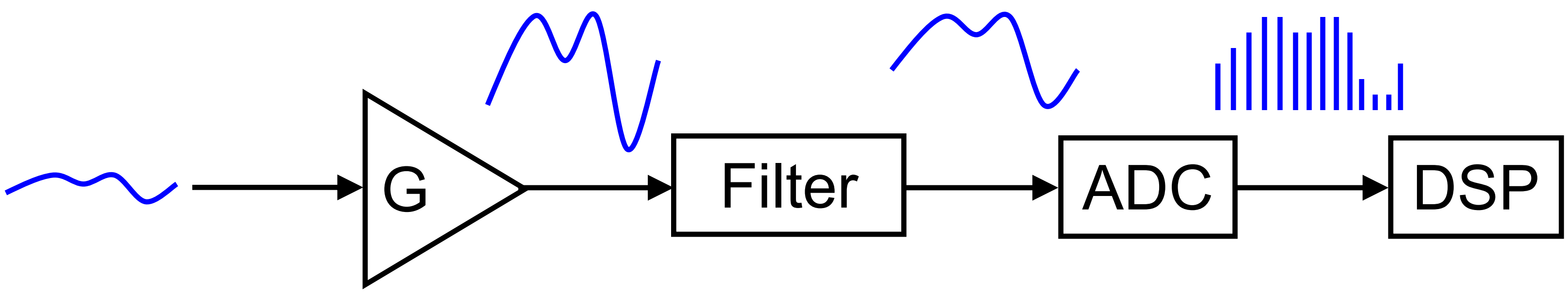
Why Analog?

- Most of the physical signals are analog in nature!
  - Sound (listening to music)
  - Electromagnetic waves (mobile phones)
  - Biosignals (ECG)
  - …
- Although digital is great we need an analog interface to convert these physical signals from analog to digital
- In many applications after processing the signals in digital domain, we need to convert them back to analog.
- Thus analog and mixed-signal (combination of analog and digital) circuits are typically the performance bottlenecks.
- Therefore, analog and mixed-signal designers are still and hopefully will be in demand for the foreseeable future.

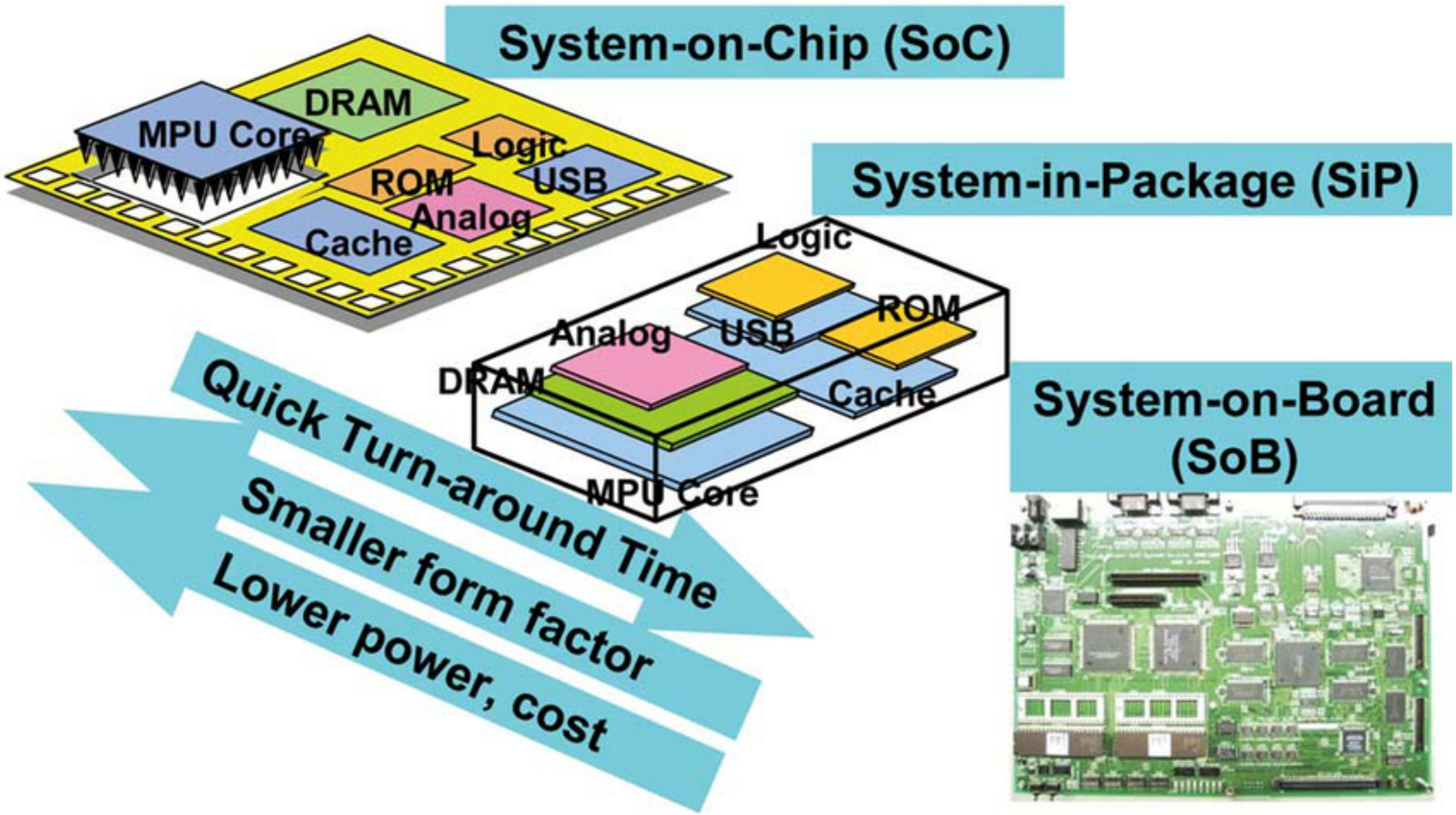
Typical Real World System



- Example:

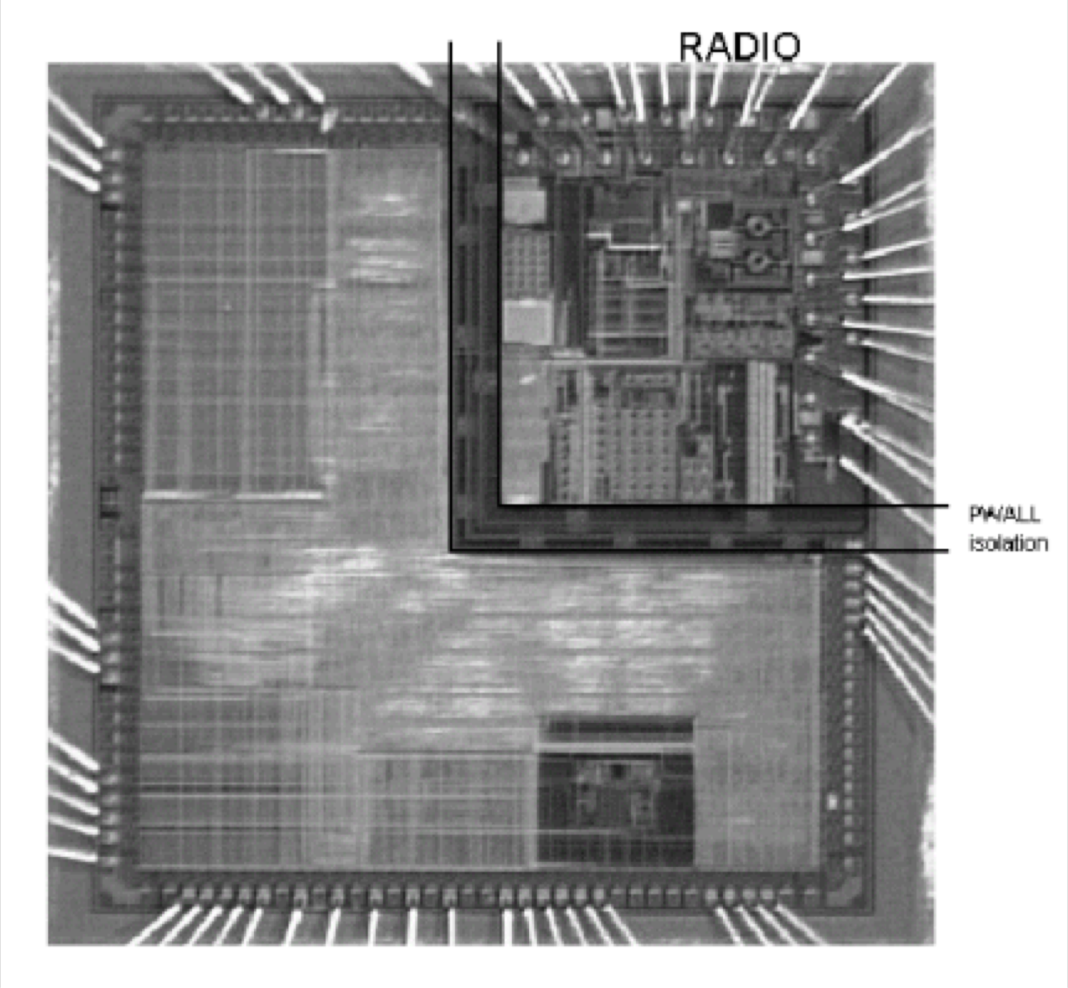


System



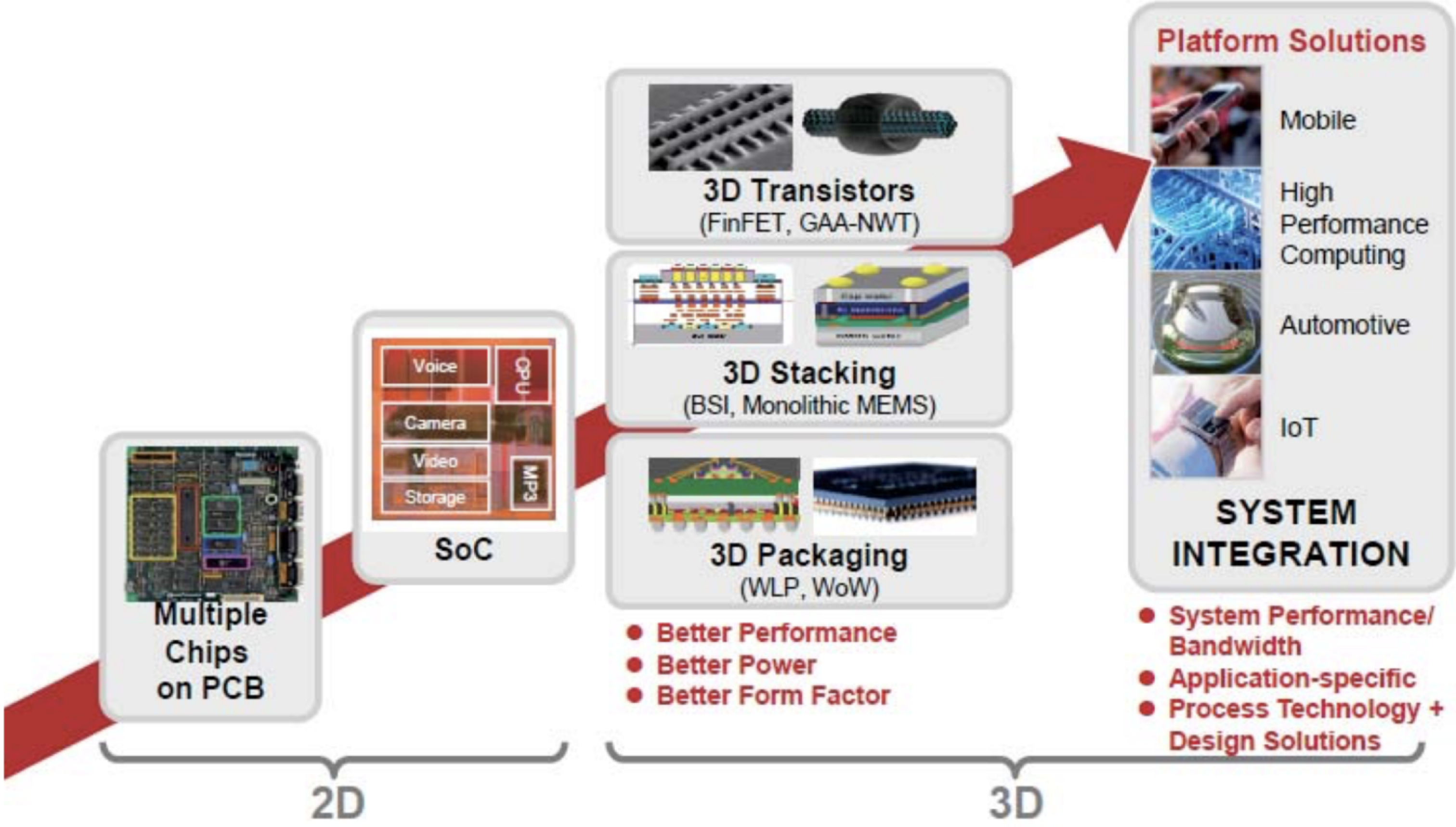
Source: R. Saleh *et al.*, "System-on-Chip: Reuse and Integration," *Proceedings of the IEEE*, vol. 94, no. 6, pp. 1050-1069, June 2006, doi: 10.1109/JPROC.2006.873611.

System on Chip



ISSCC 2002

Chip and System Integration



Source: Cliff Hou (TSMC), ISSCC 2017 (Plenary)