ELEC 401: Analog CMOS Integrated Circuit Design

Set 6

Opamp Design

References: "Analog Integrated Circuit Design" by D. Johns and K. Martin and "Design of Analog CMOS Integrated Circuits" by B. Razavi

All figures in this set of slides are taken from the above books

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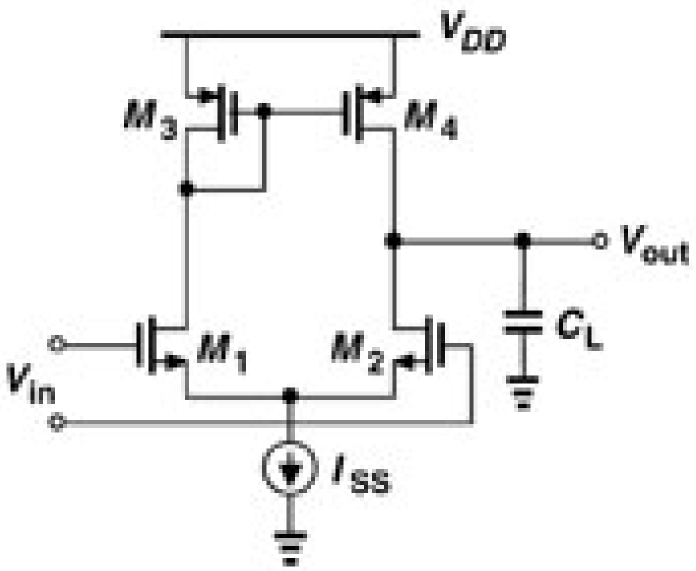
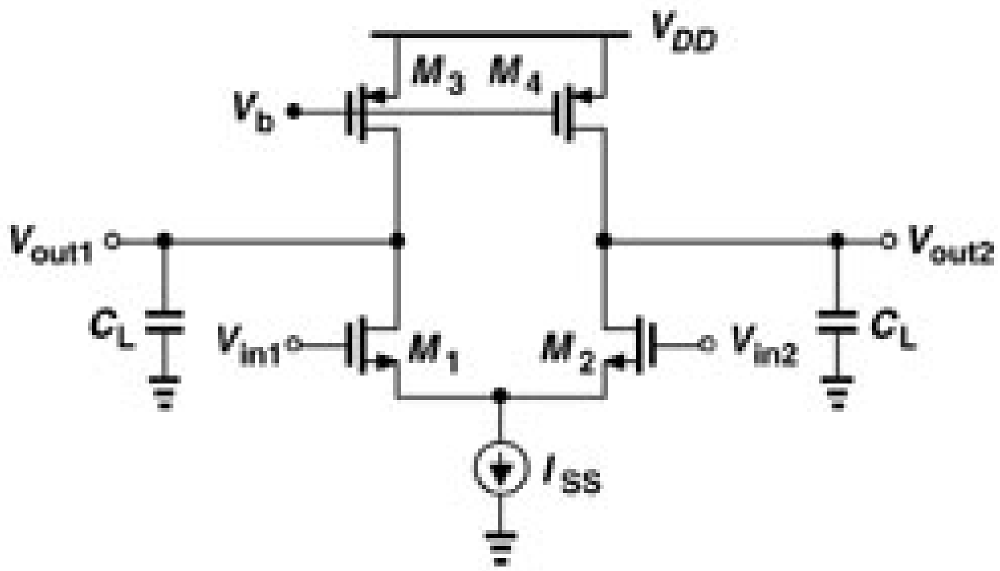
General Considerations

- Gain
- Small-signal bandwidth
- Large-signal performance
- Output swing
- Input common-mode range
- Linearity
- Noise/offset
- Supply rejection

One-Stage Op Amps

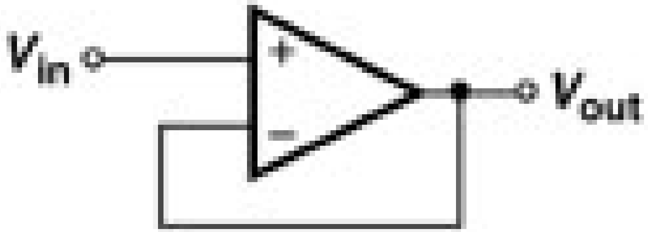


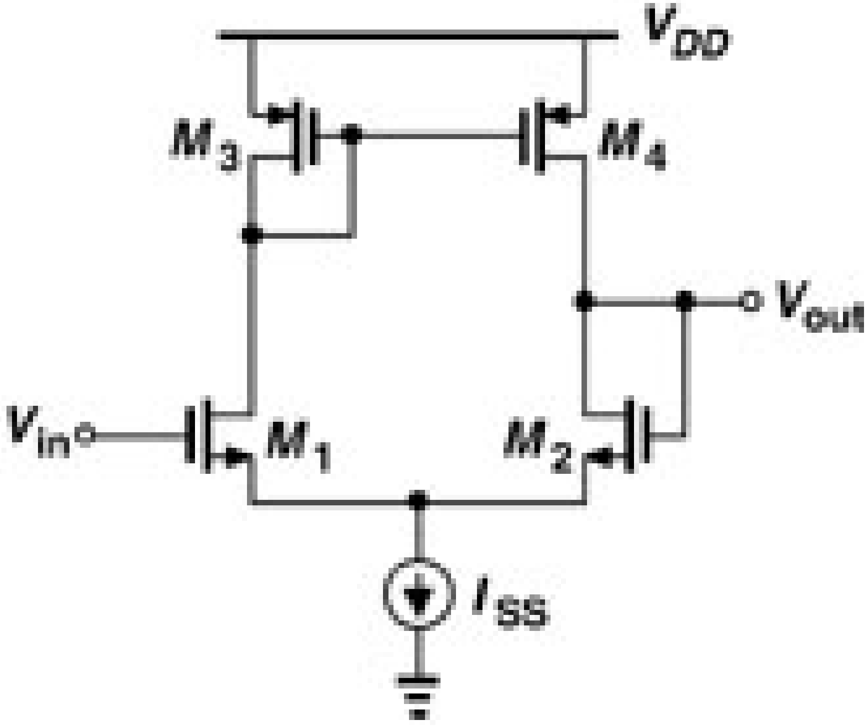
(a)



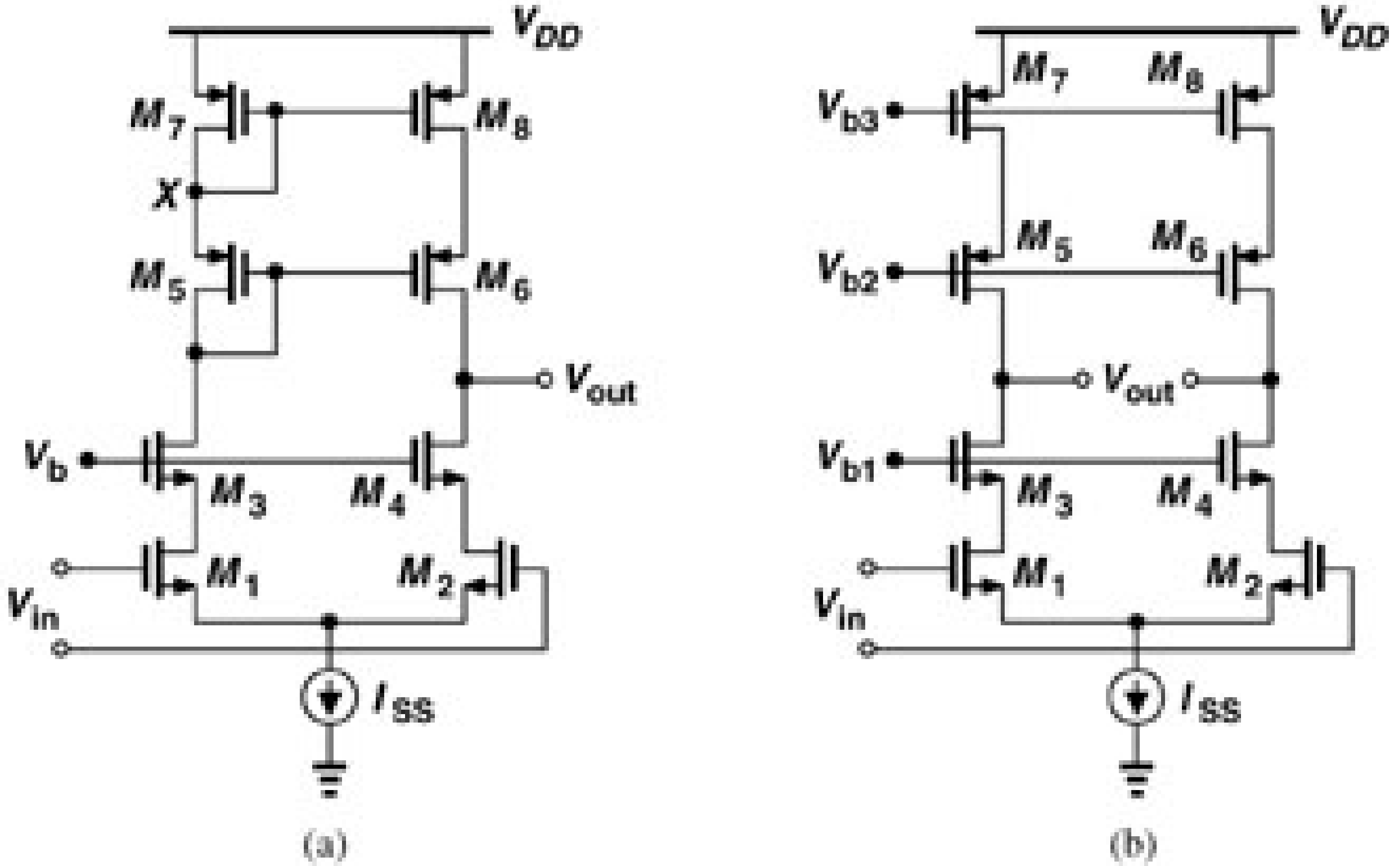
(b)

One-Stage Op Amp in Unity Gain Configuration

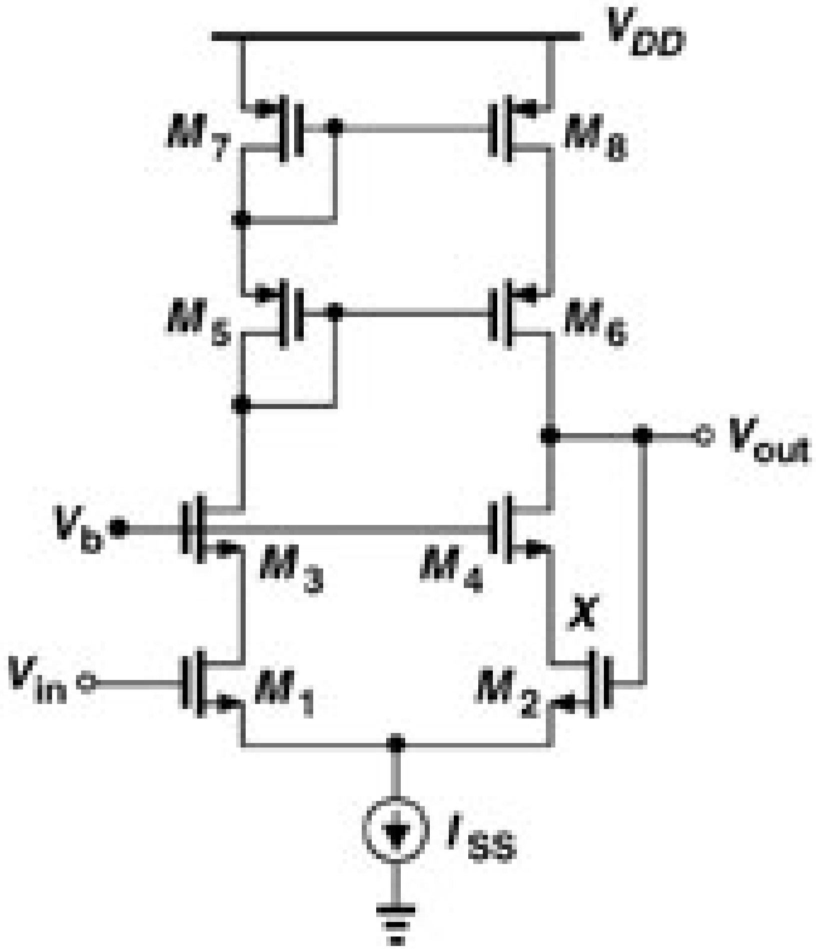


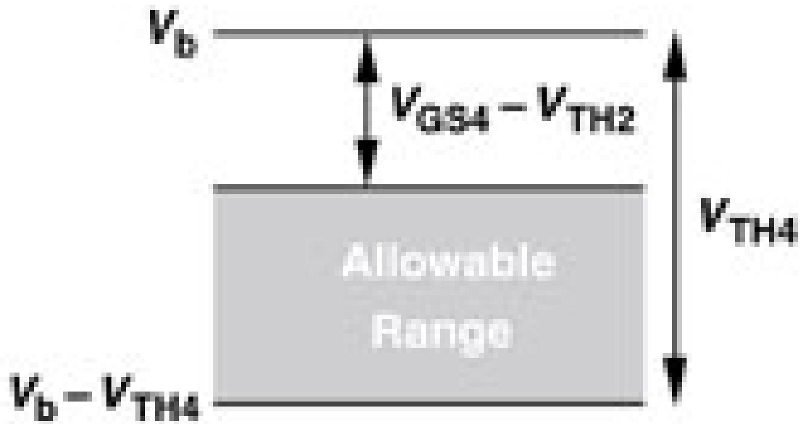


Cascode Op Amps

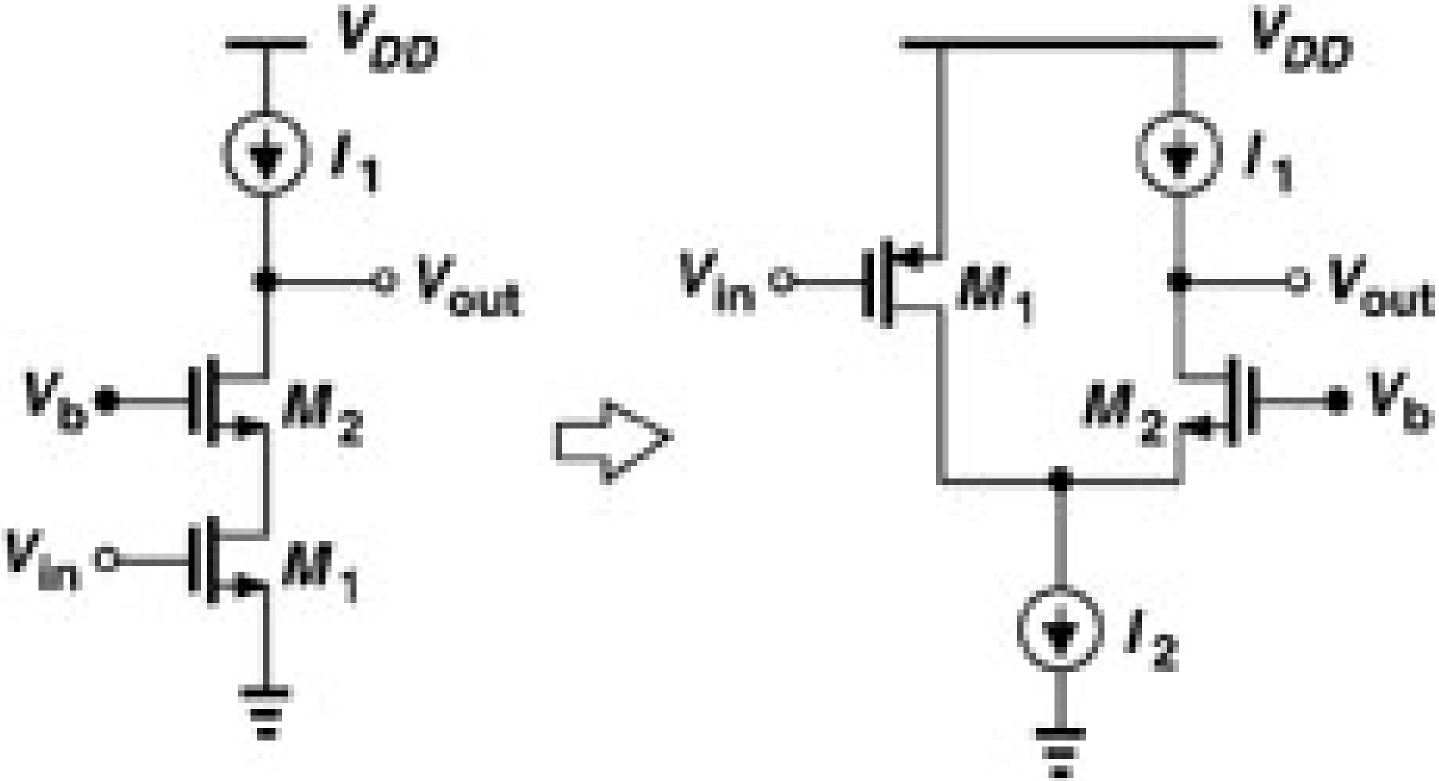


Unity Gain One Stage Cascode

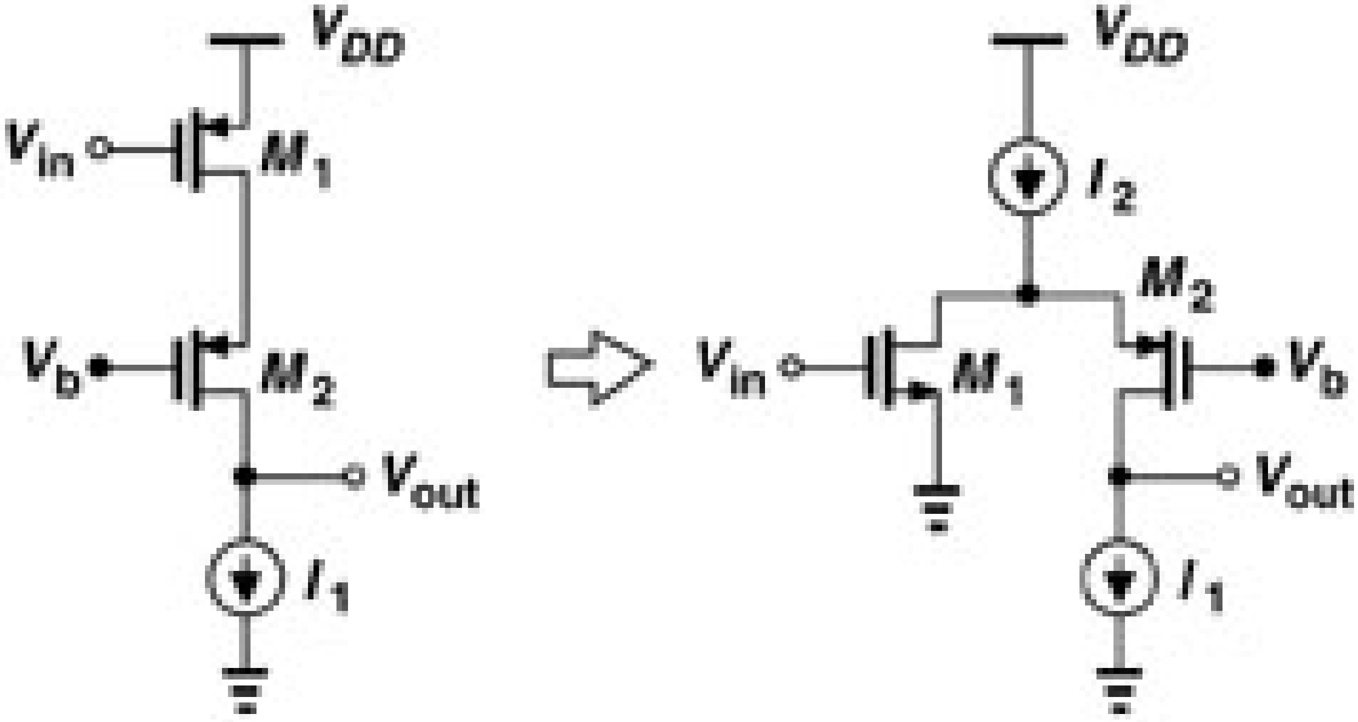




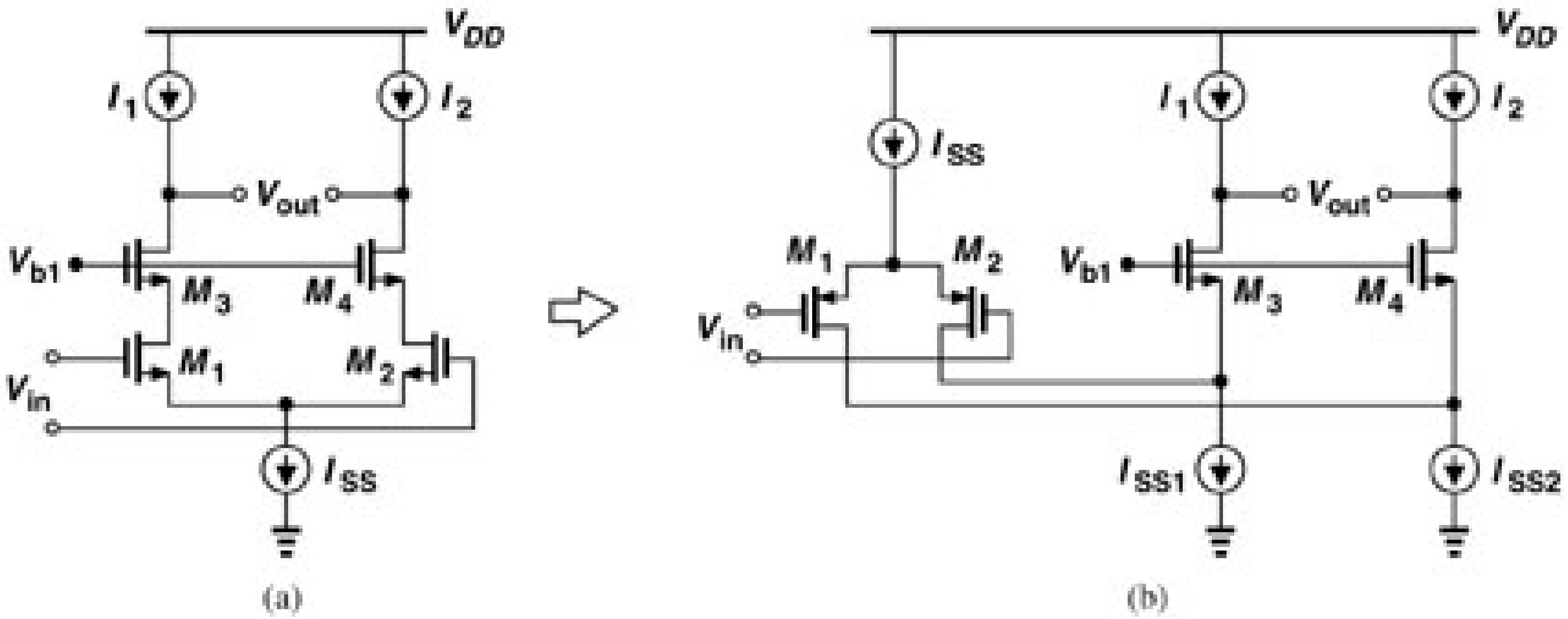
Folded Cascode Op Amps



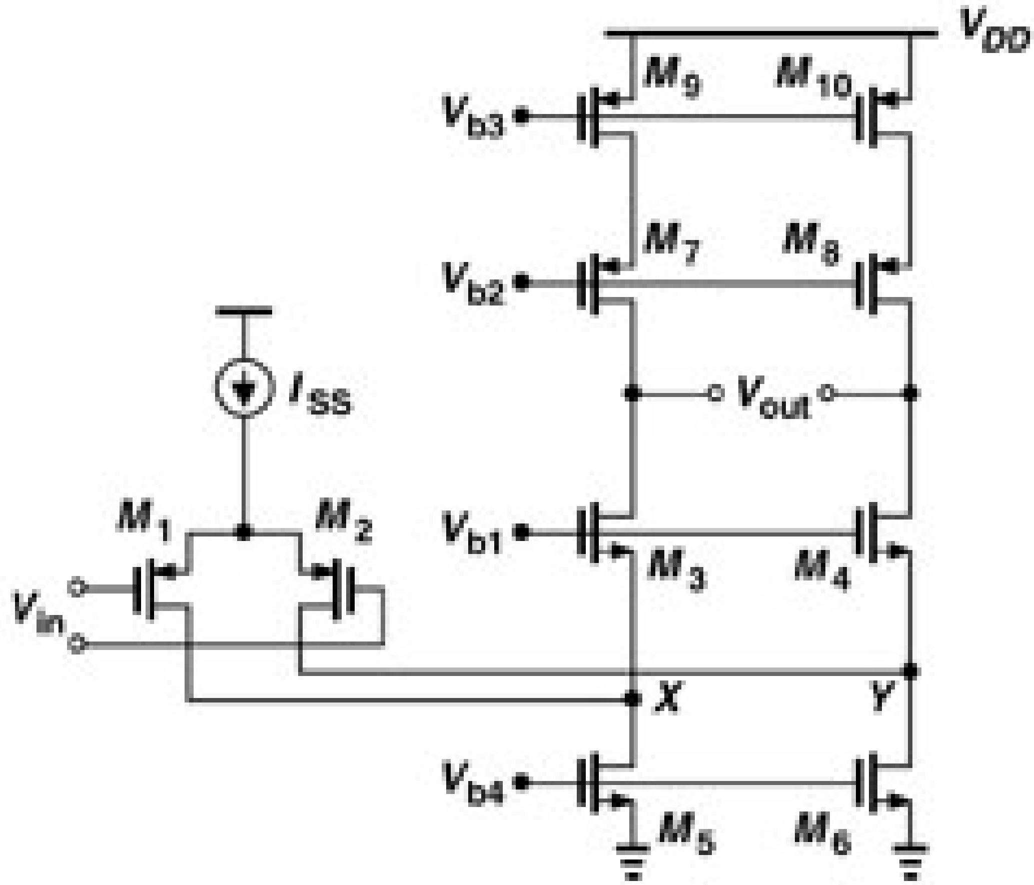
Folded Cascode Stages



Folded Cascode (cont.)

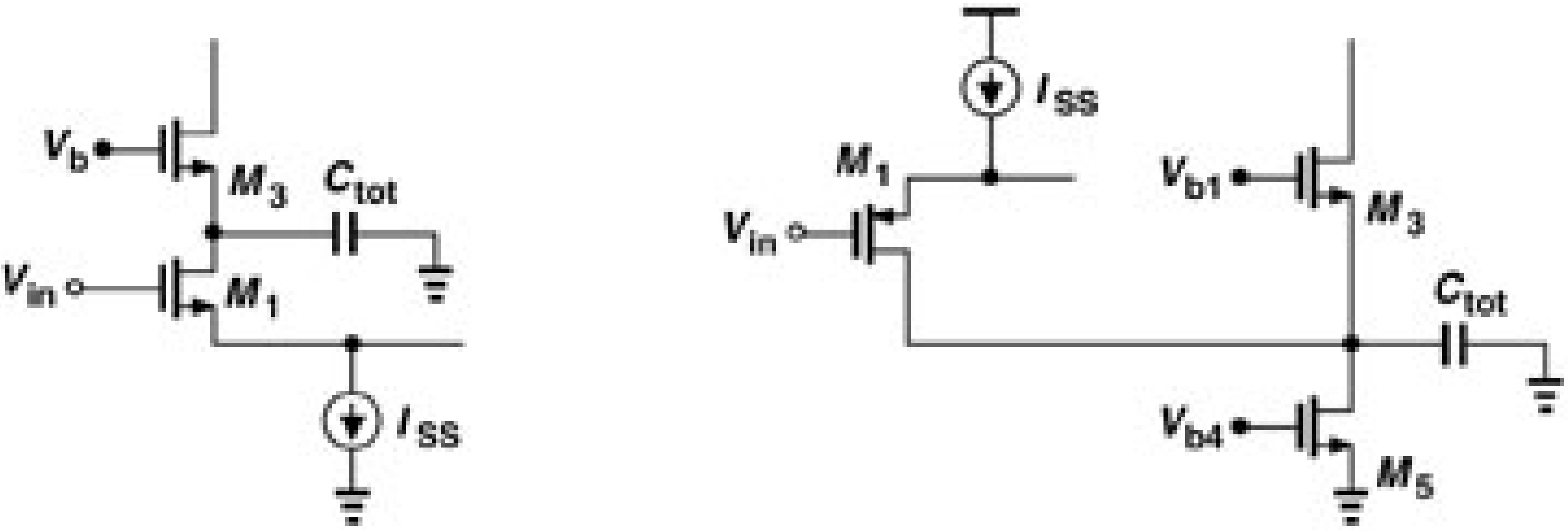


Folded Cascode (cont.)



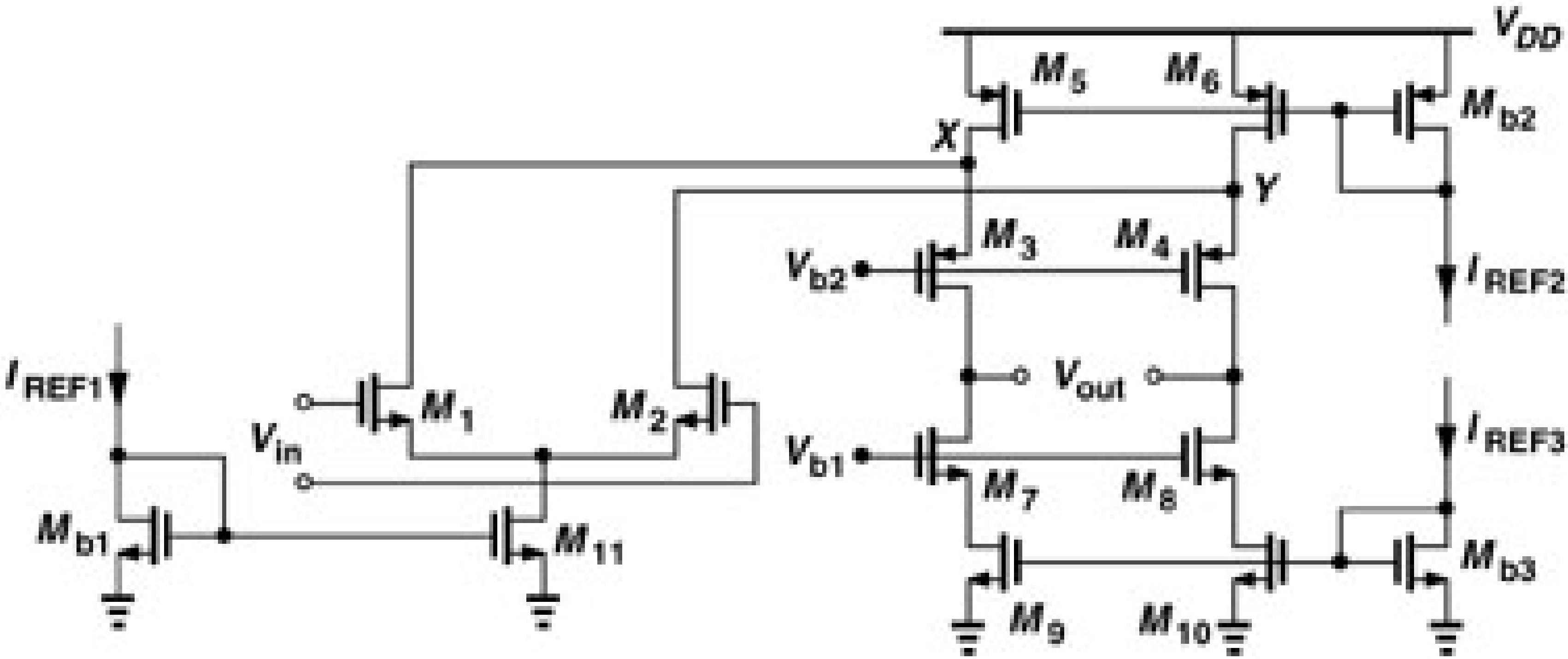
$$|A_v| \approx g_{m1}\{[(g_{m3}+g_{mb3})r_{o3}(r_{o1}\parallel r_{o5})]\parallel[(g_{m7}+g_{mb7})r_{o7}r_{o9}]\}$$

Telescopic versus Folded Cascode

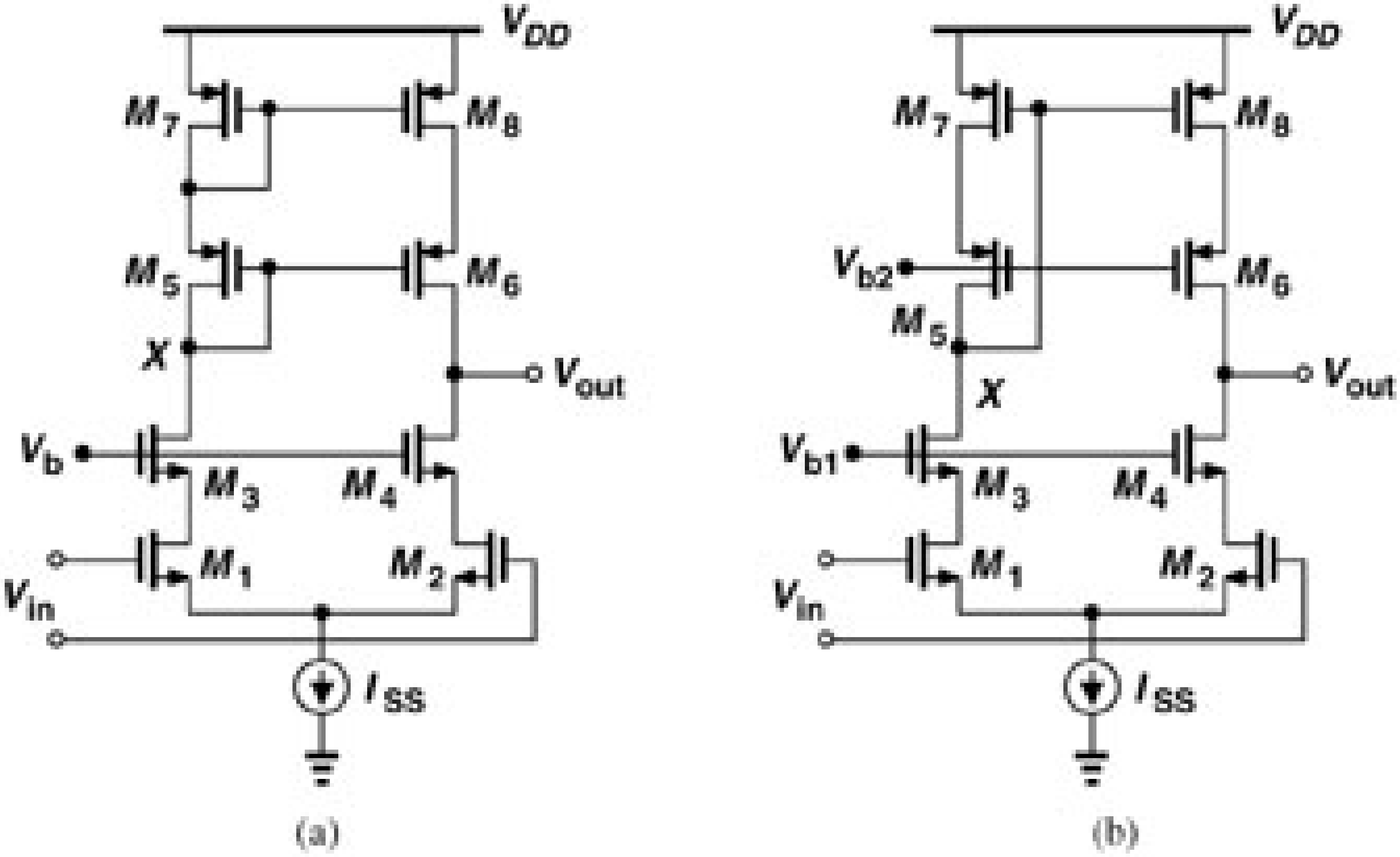


(a) (b)

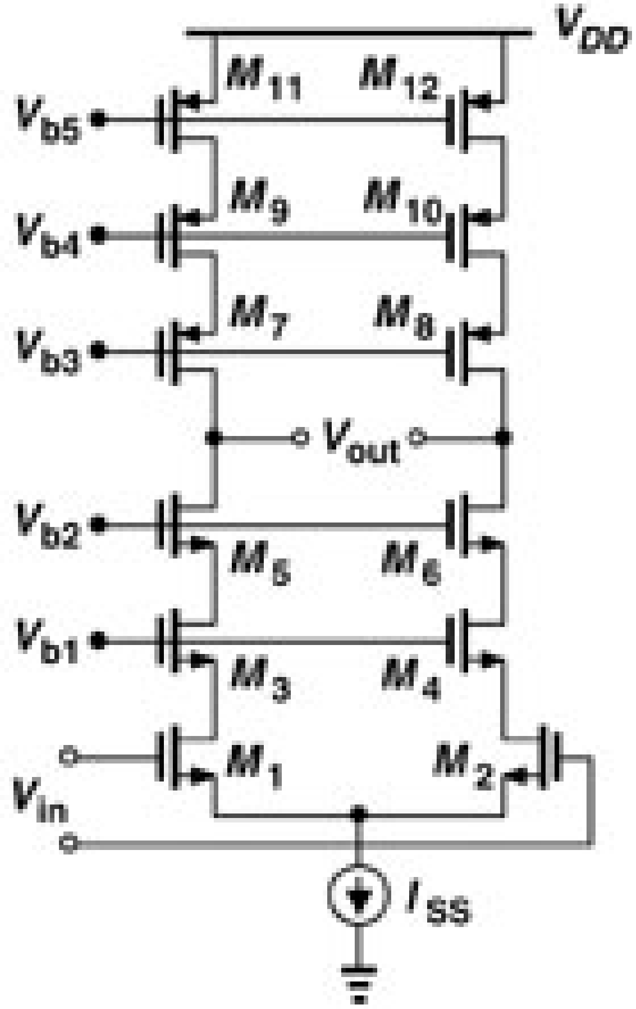
Example Folded-Cascode Op Amp



Single-Ended Output Cascode Op Amps



Triple Cascode

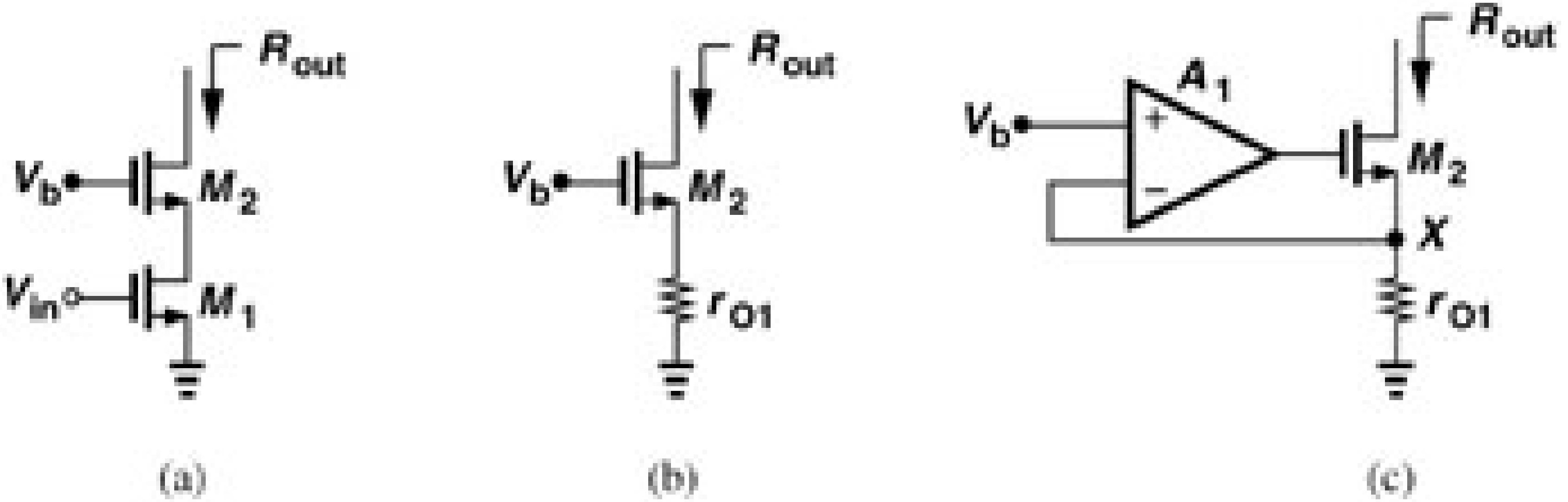


A_v app. $(g_m r_o)^3/2$

Limited Output Swing

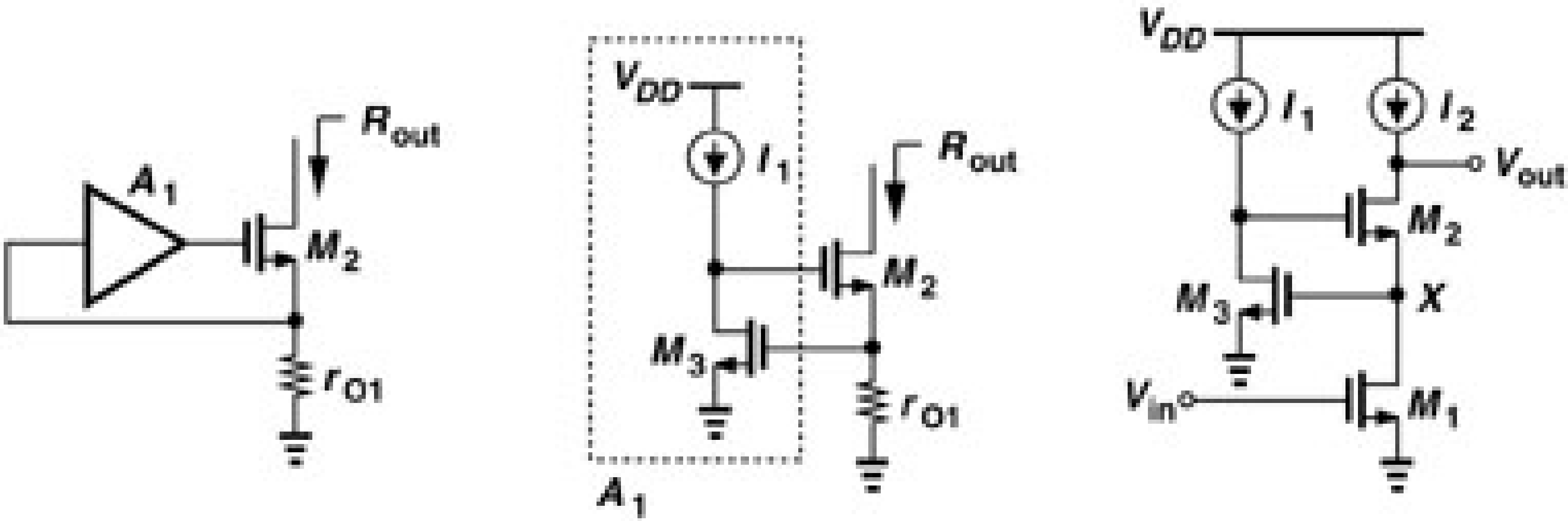
Complex biasing

Output Impedance Enhancement



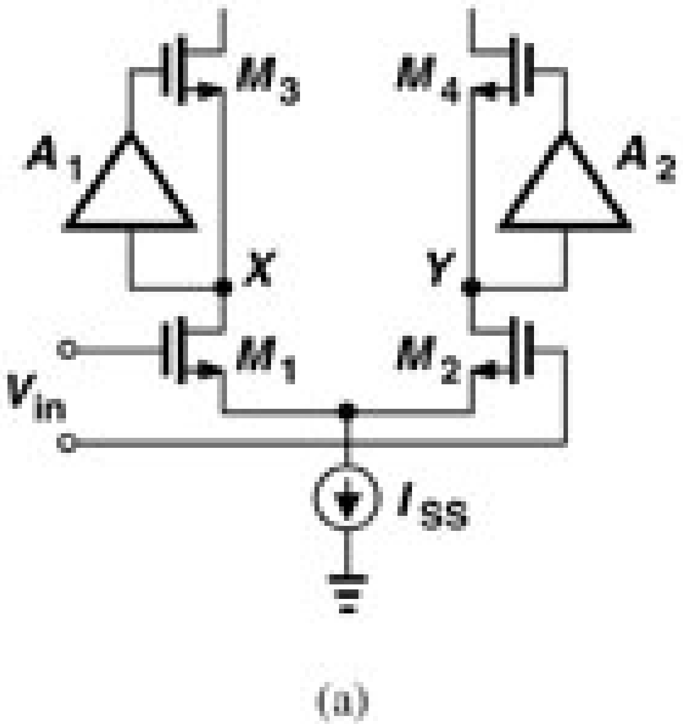
$$R_{out} = A_1 g_{m2} r_{o2} r_{o1}$$

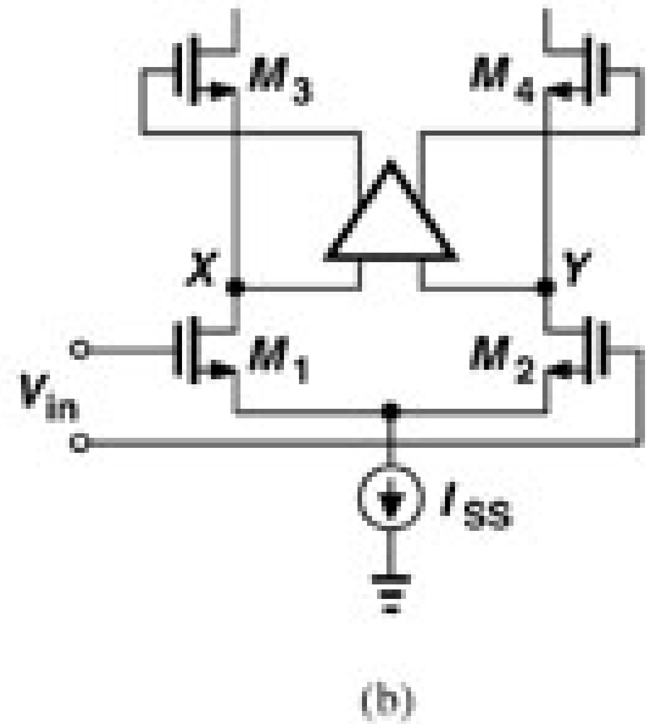
Gain Boosting in Cascode Stage



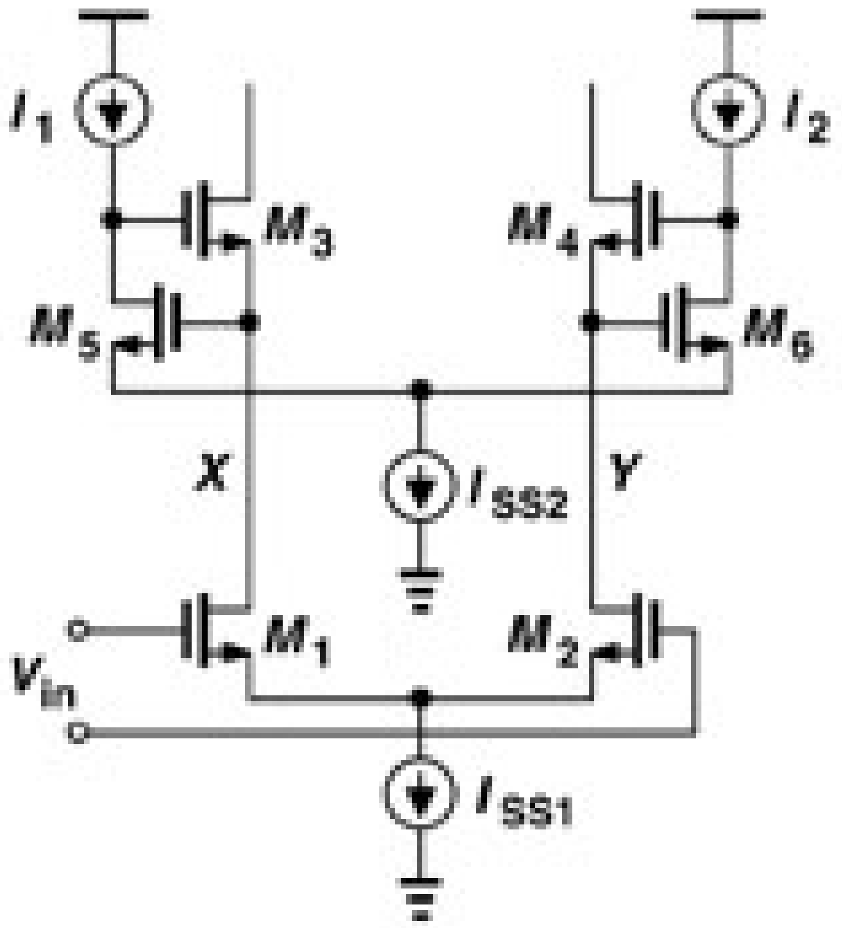
(a) (b) (c)

Differential Gain Boosting

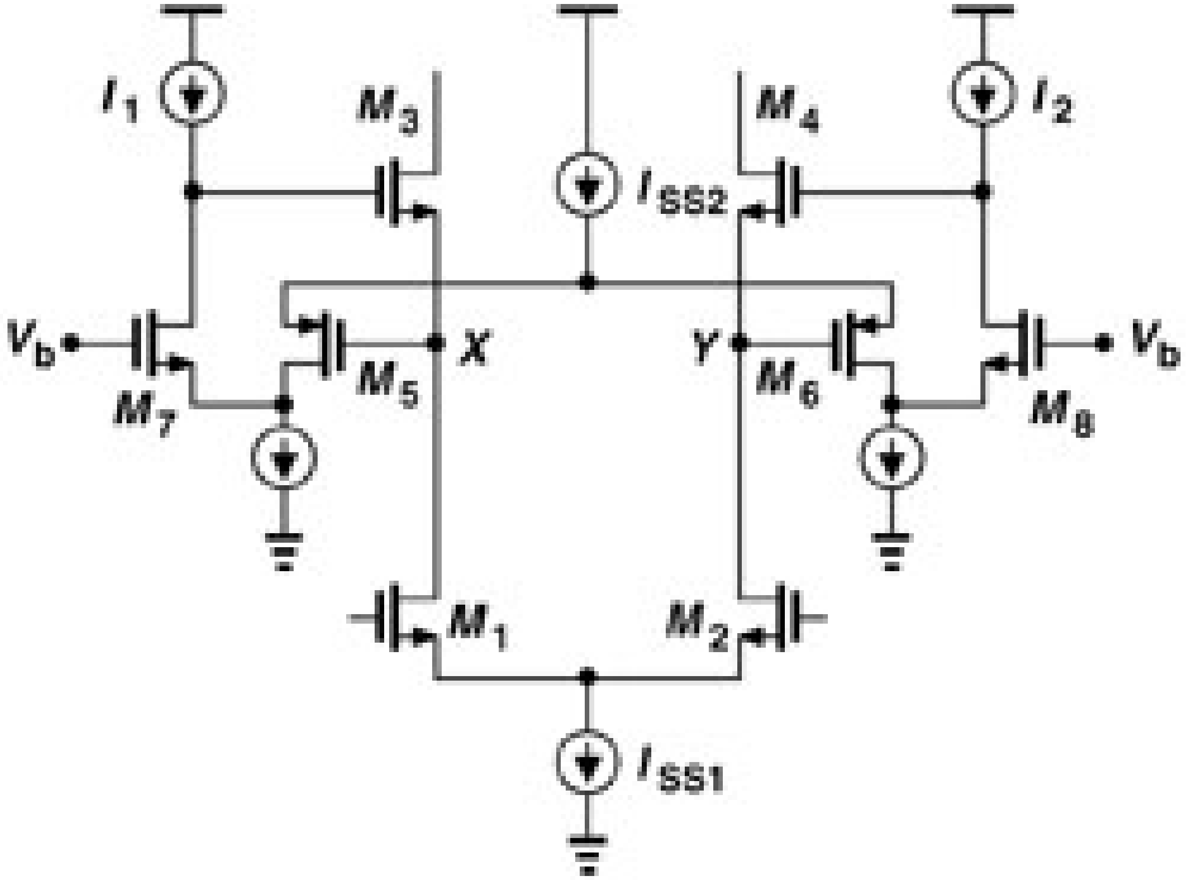




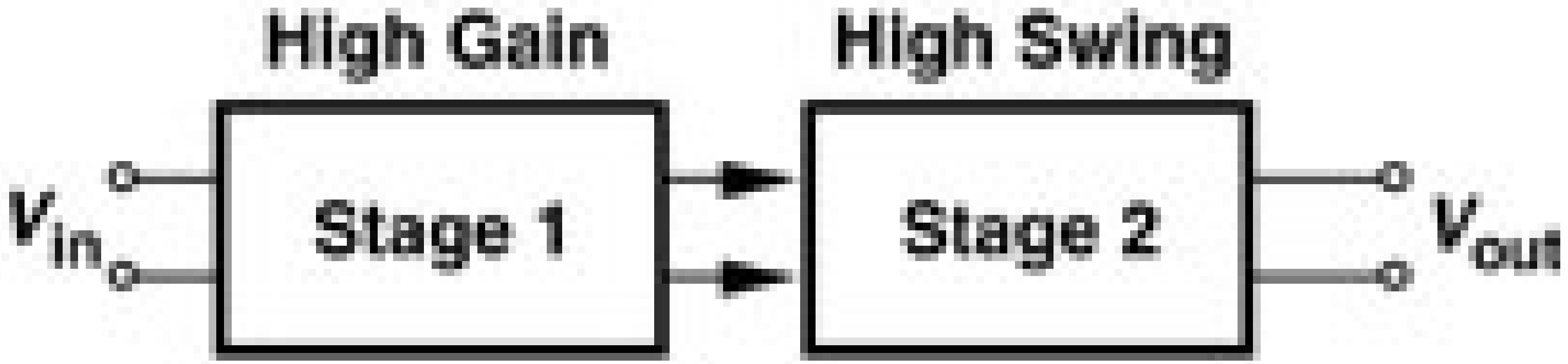
Differential Gain Boosting



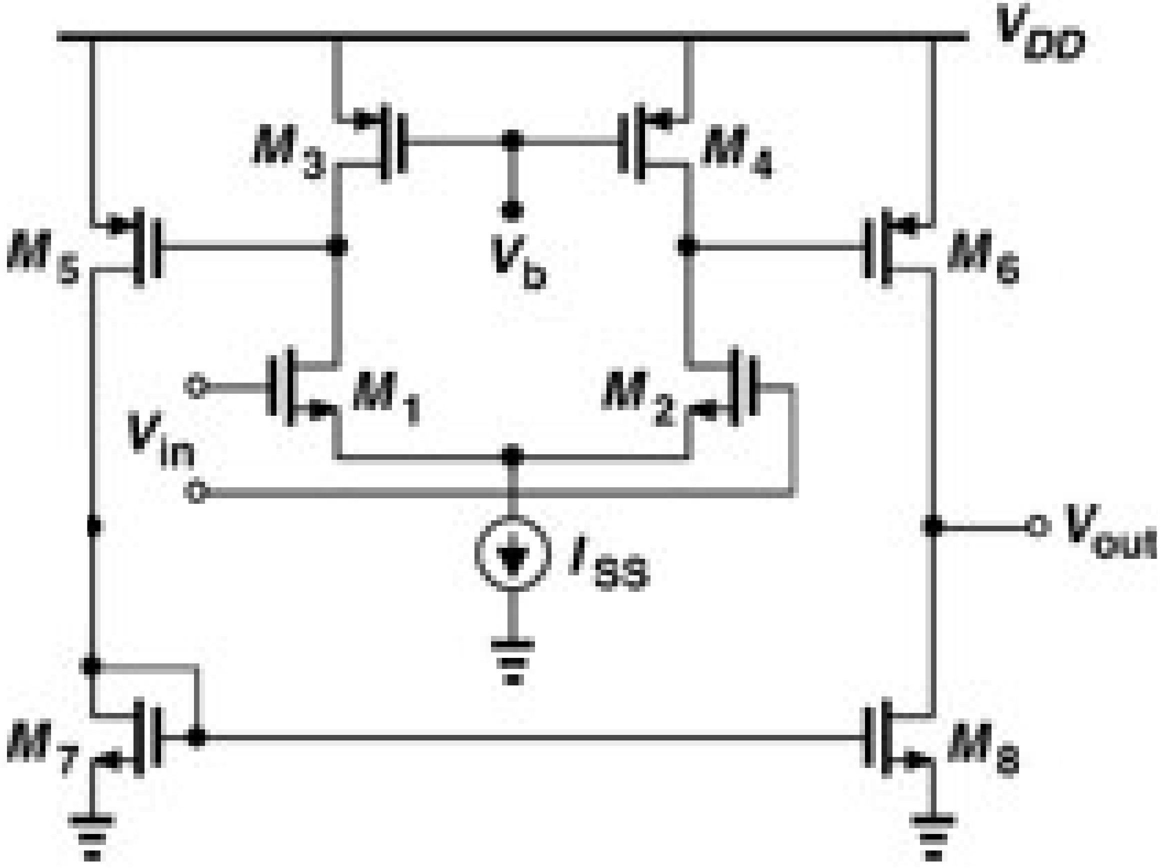
Differential Gain Boosting



Two-Stage Op Amps

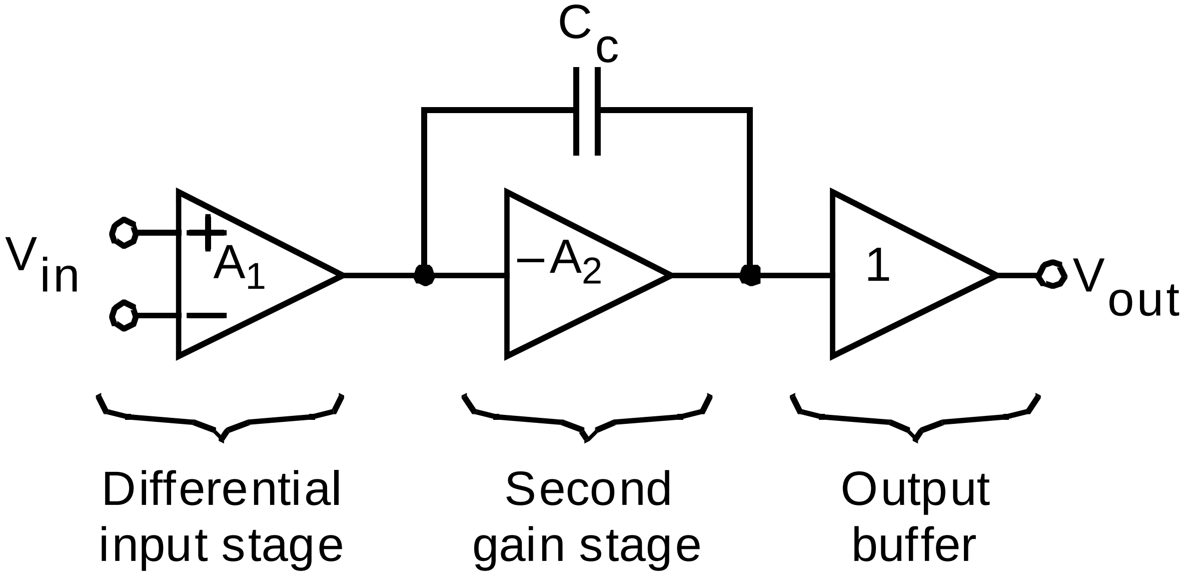


Single-Ended Output Two-Stage Op Amp

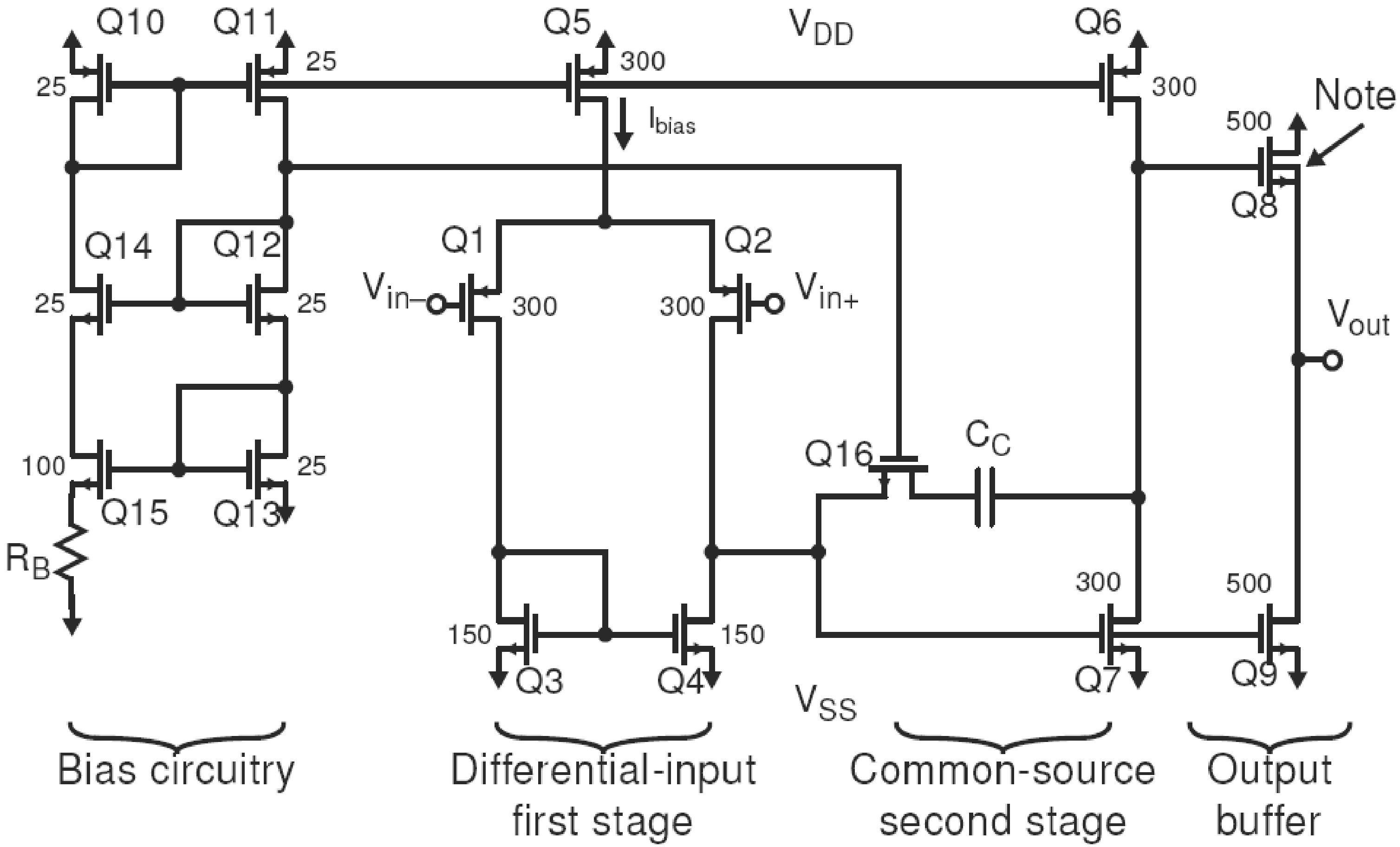


Two-Stage CMOS Opamp

- Popular opamp design approach
- A good example to review many important design concepts
- Output buffer is typically used to drive resistive loads
- For capacitive loads (typical case in CMOS) buffer is not required.



Two-Stage CMOS Opamp Example



all transistor lengths = 1.6 μm (1 μm technology was used!)

Gain of the Opamp

- First Stage

  Differential to single-ended

$$A_{v1} = g_{m1}(r_{O2} \| r_{O4})$$

$$g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \frac{I_{bias}}{2}}$$

- Second Stage

  Common-source stage

$$A_{v2} = -g_{m7}(r_{O6} \| r_{O7})$$

- Output buffer is not required when driving capacitive loads

Gain of the Opamp

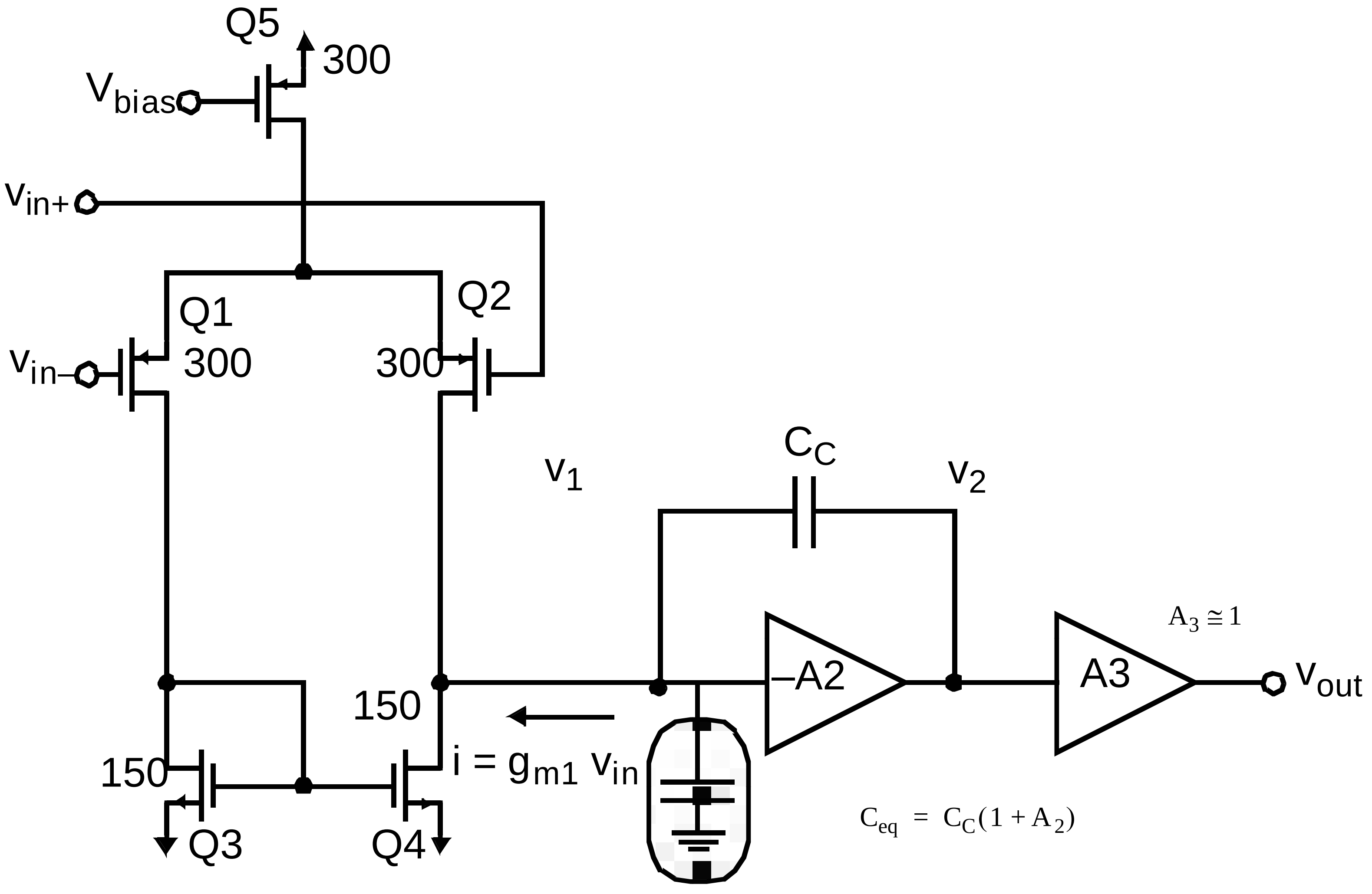
Third Stage

- Source follower

$$A_{v3} \cong \frac{g_{m8}}{g_{m8} + G_L + g_{mb8} + g_{O8} + g_{O9}}$$

- Typical gain: between 0.7 to1
- Note: $g_o = 1/r_o$ and $G_L = 1/R_L$
- g_{mb} is body-effect conductance (is zero if source can be tied to substrate)

Frequency Response



Frequency Response

Simplifying assumptions:

- C_C dominates
- Ignore Q_{16} for the time being (it is used for lead compensation)

Miller effect results in

$$C_{eq} = C_C(1 + A_2) \cong C_C A_2$$

- At midband frequencies

$$Z_{eq} = r_{O2} \| r_{O4} \| 1/sC_{eq} \cong 1/(sC_C A_2)$$

$$A_1 = g_{m1} Z_{eq} = g_{m1}/(sC_C A_2)$$

Frequency Response

- Overall gain (assuming $A_3 \approx 1$)

$$A_v(s) = A_2 A_1 = g_{m1}/(sC_C)$$

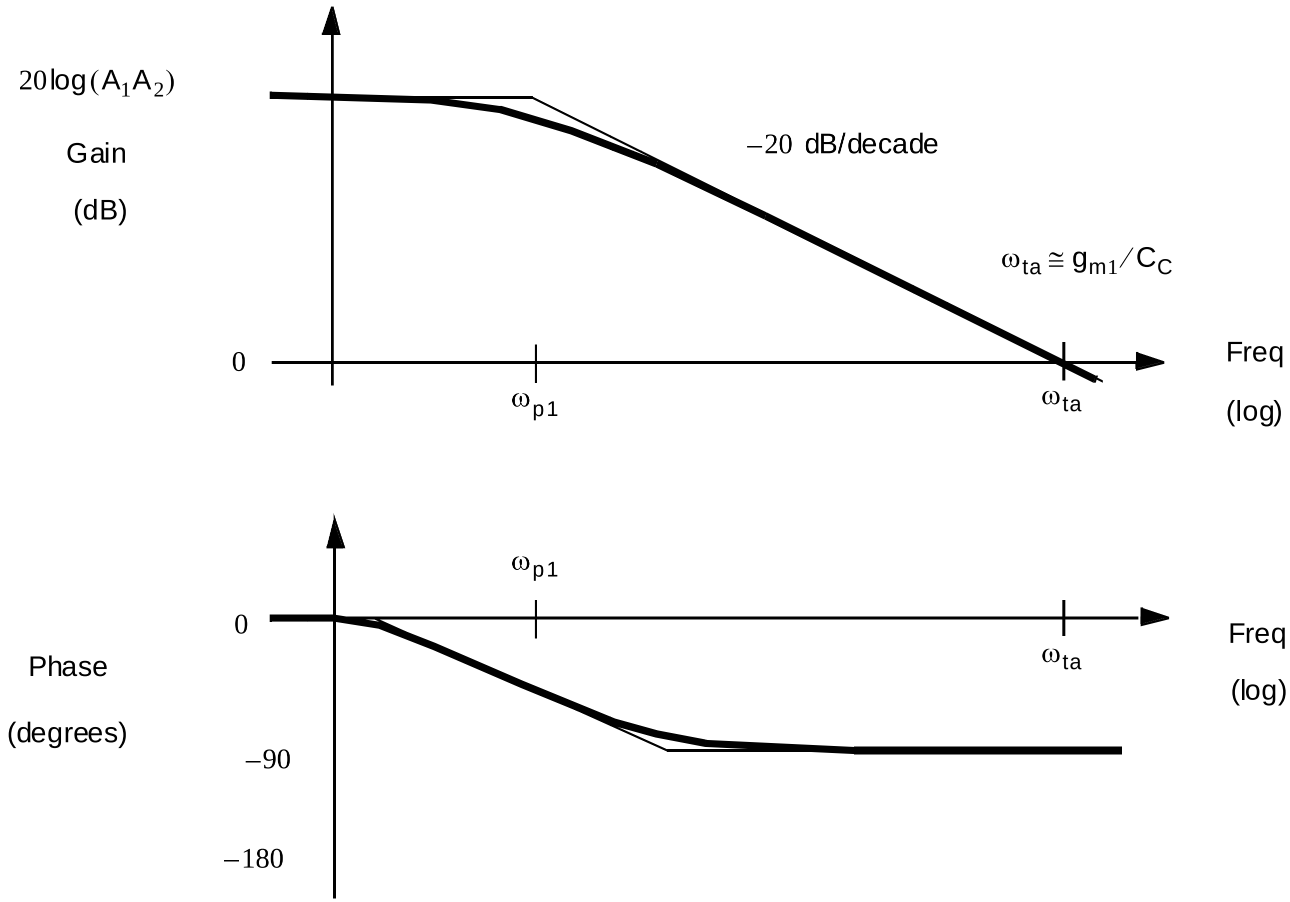
which results in a unity-gain frequency of

$$\omega_{ta} = g_{m1}/C_C$$

- Note: ω_{ta} is directly proportional to g_{m1} and inversely proportional to C_C.

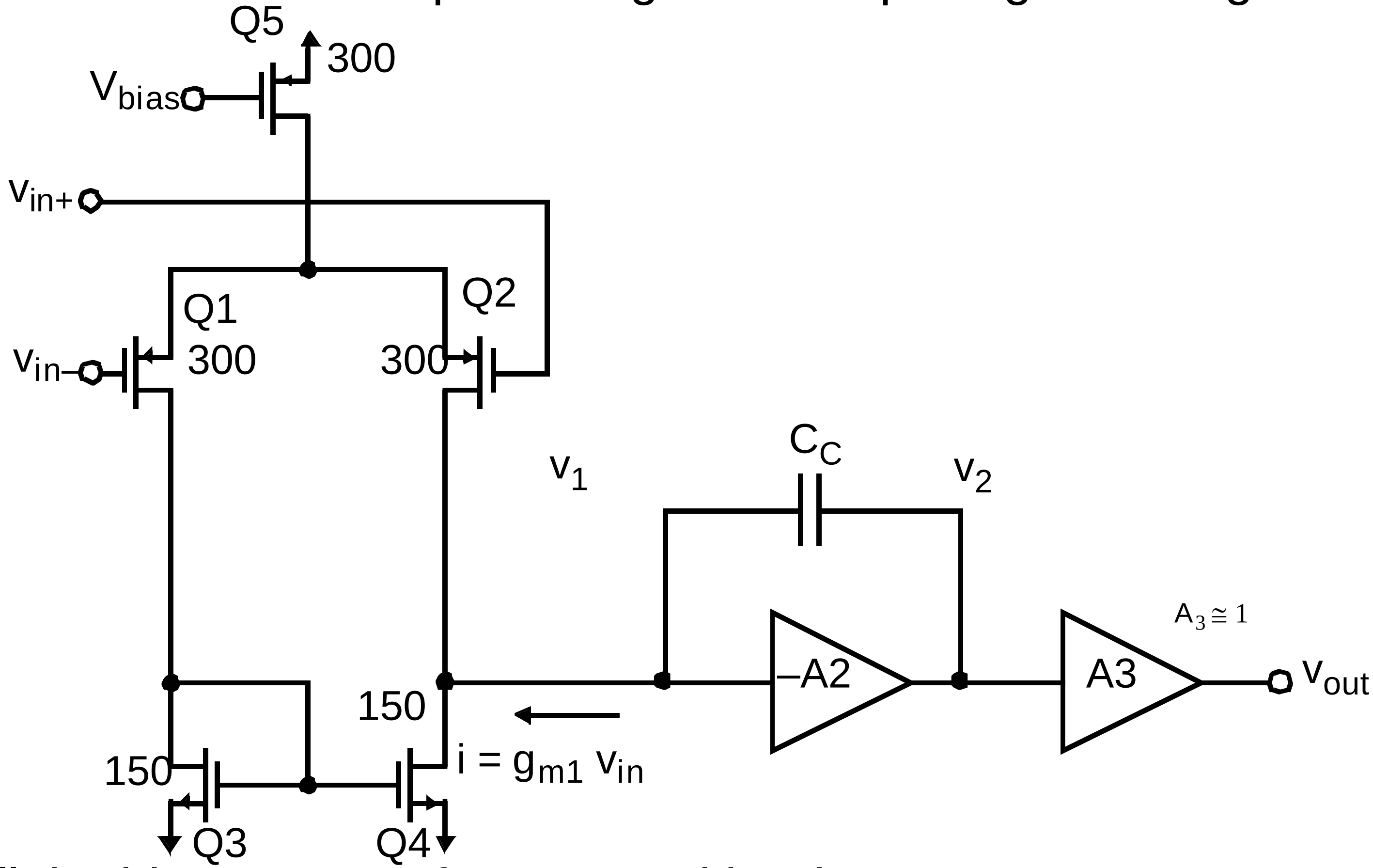
Frequency Response

- First-order model



Slew Rate

- Maximum rate of output change when input signal is large.



- All the bias current of Q5 goes either into Q1 or Q2.

Slew Rate

- Thus

$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{max} = \frac{I_{C_C}|_{max}}{C_C} = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C}$$

I_{D1} is nominal bias current of input transistors

- Using $C_C = g_{m1}/\omega_{ta}$ and $g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}}$

$$SR = \frac{2I_{D1}}{\sqrt{2\mu_p C_{ox}(W/L)_1 I_{D1}}}\omega_{ta} = V_{eff1}\omega_{ta}$$

where $V_{eff1} = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_1}}$

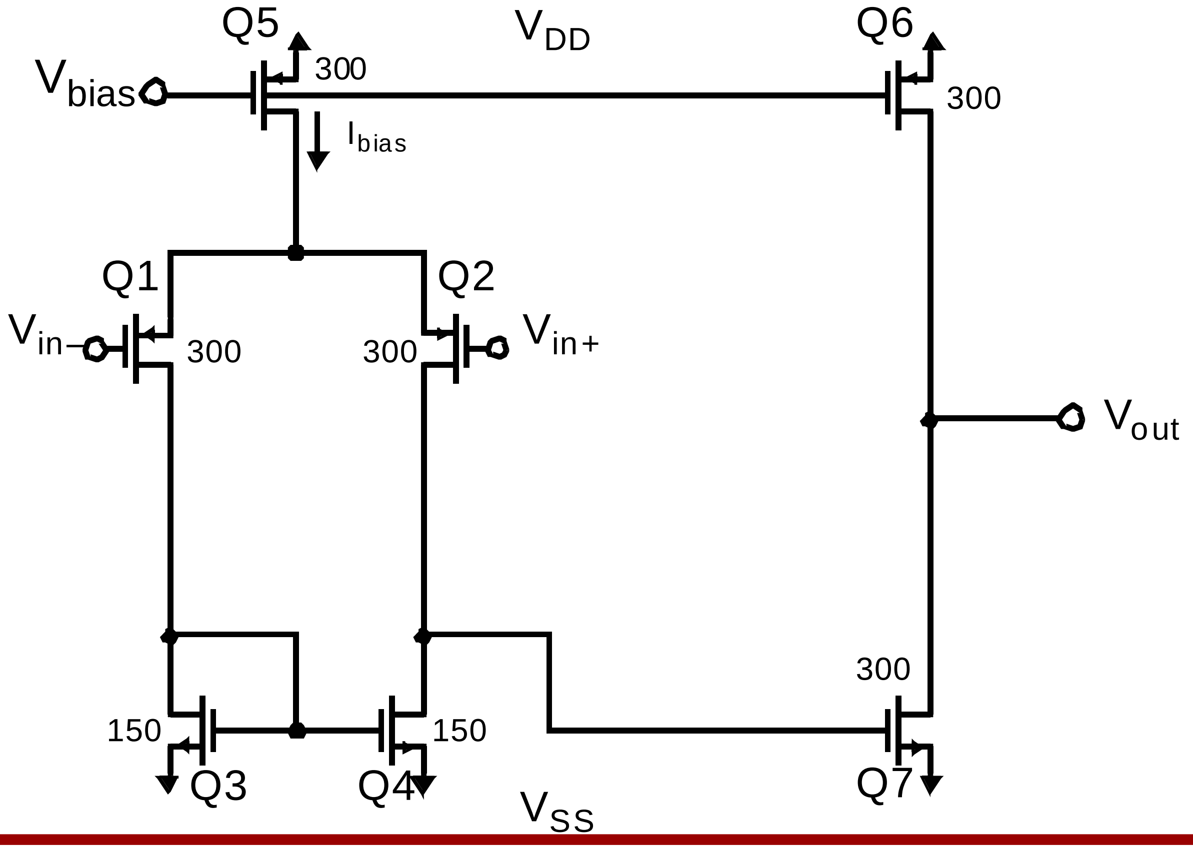
Slew Rate

$$SR = V_{eff1}\omega_{ta}$$

- Normally, the designer has not much control over ω_{ta}
- Slew-rate can be increased by increasing V_{eff1}
- This is one of the reasons for using p-channel input stage: higher slew-rate

Systematic Offset Voltage

- To ensure inherent (systematic) offset voltage does not exist, nominal current through Q7 should equal to that of Q6 when the differential input is zero.



Systematic Offset Voltage

- Avoid systematic offset by choosing:

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5}$$

- Found by noting

$$I_{D5} = 2I_{D3} = 2I_{D4}$$

and

$$V_{GS7} = V_{DS3} = V_{GS4}$$

then setting $I_{D7} = I_{D6}$

N-Channel versus P-Channel Input Stage

- Complimentary opamp can be designed with an n-channel input differential pair and p-channel second-stage
- Overall gain would be roughly the same in both designs

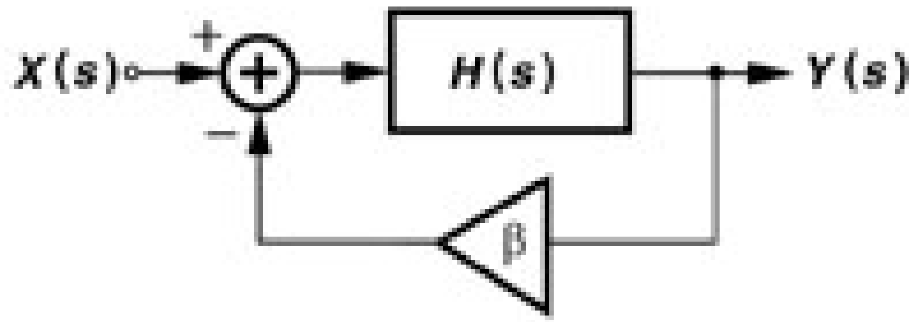
P-channel Advantages

- Higher slew-rate: for fixed bias current, V_{eff} is larger (assuming similar widths used for maximum gain)
- Higher frequency of operation: higher transconductance of second stage which results in higher unity-gain frequency
- Lower 1/f noise: holes less likely to be trapped; p-channel transistors have lower 1/f noise
- N-channel source follower is preferable (less voltage drop and higher g_m)

N-channel Advantage

- Lower thermal noise — thermal noise is lowered by high transconductance of first stage

Feedback and Opamp Compensation



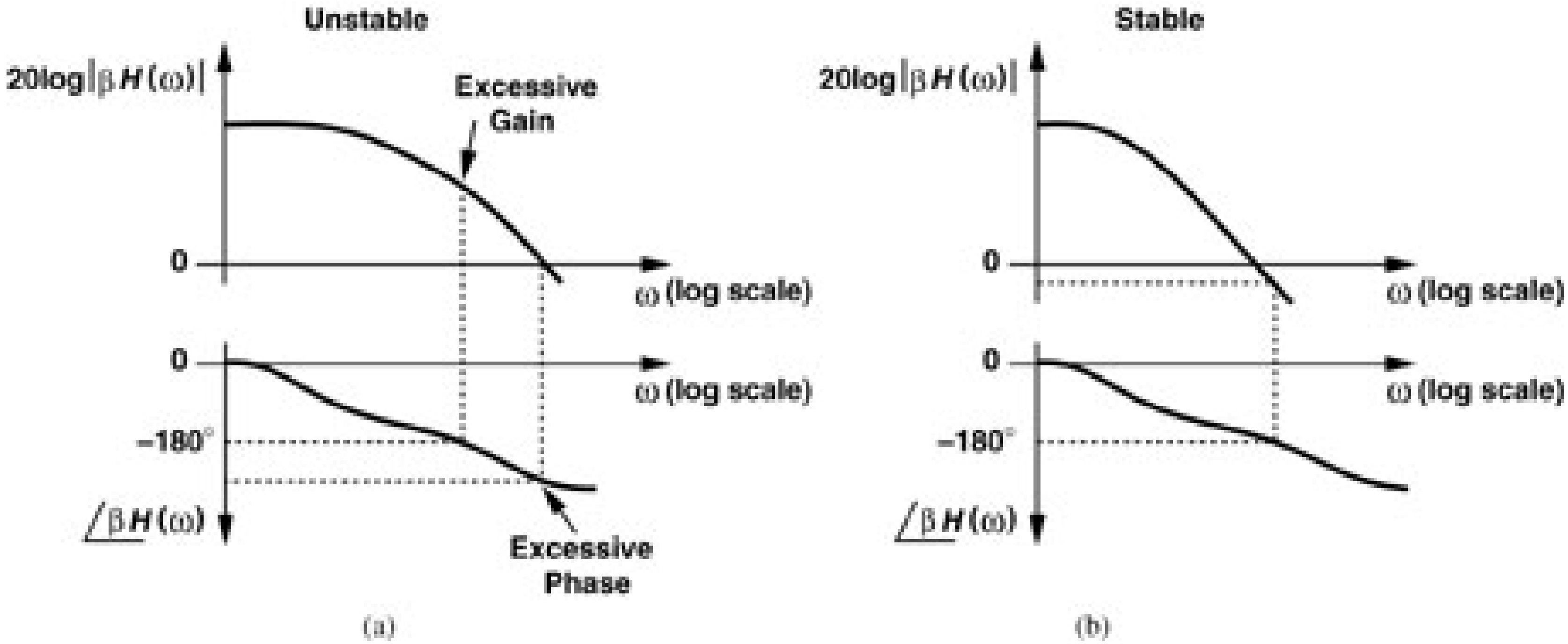
$$\frac{Y}{X}(s) = \frac{H(s)}{1+\beta H(s)}$$

- Feedback systems may oscillate
- The following two are the oscillation conditions:

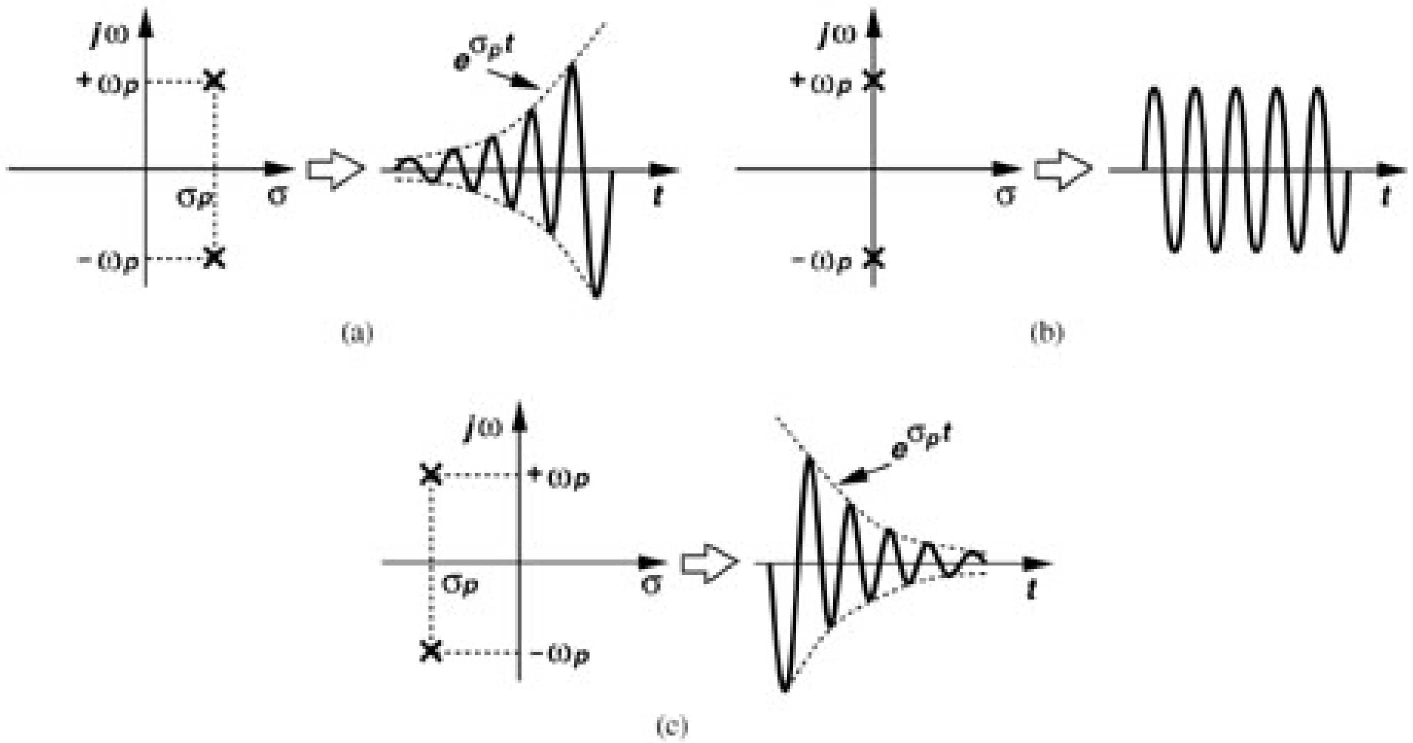
$$|\beta H(j\omega)| = 1$$

$$\angle \beta H(j\omega) = -180$$

Stable and Unstable Systems



Time-domain response of a feedback system

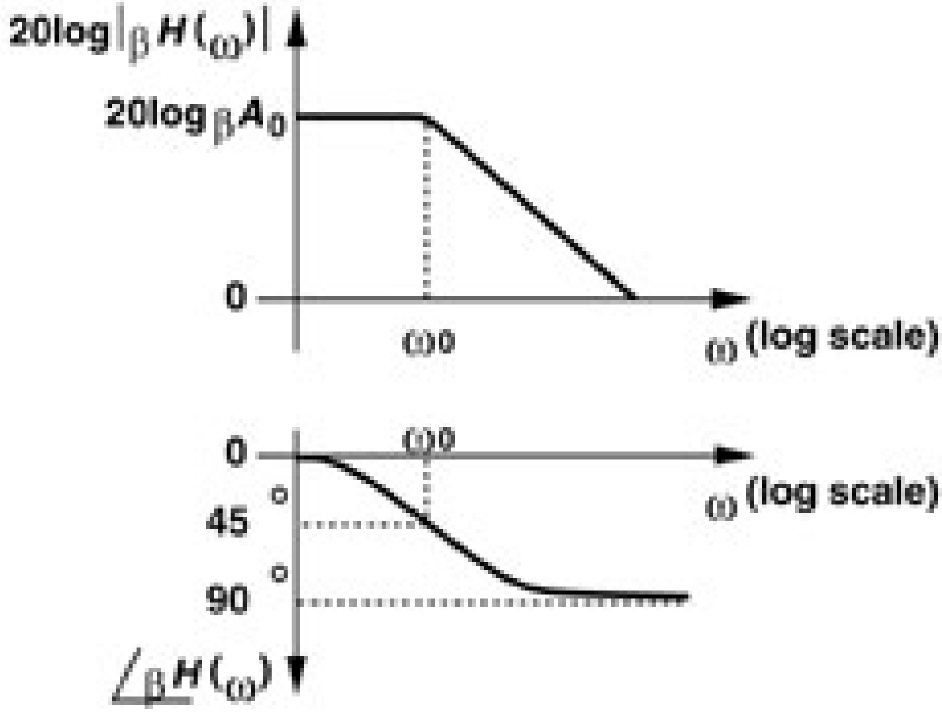


One-pole system

$$H(s) = \frac{A_0}{1 + s/\omega_0}$$

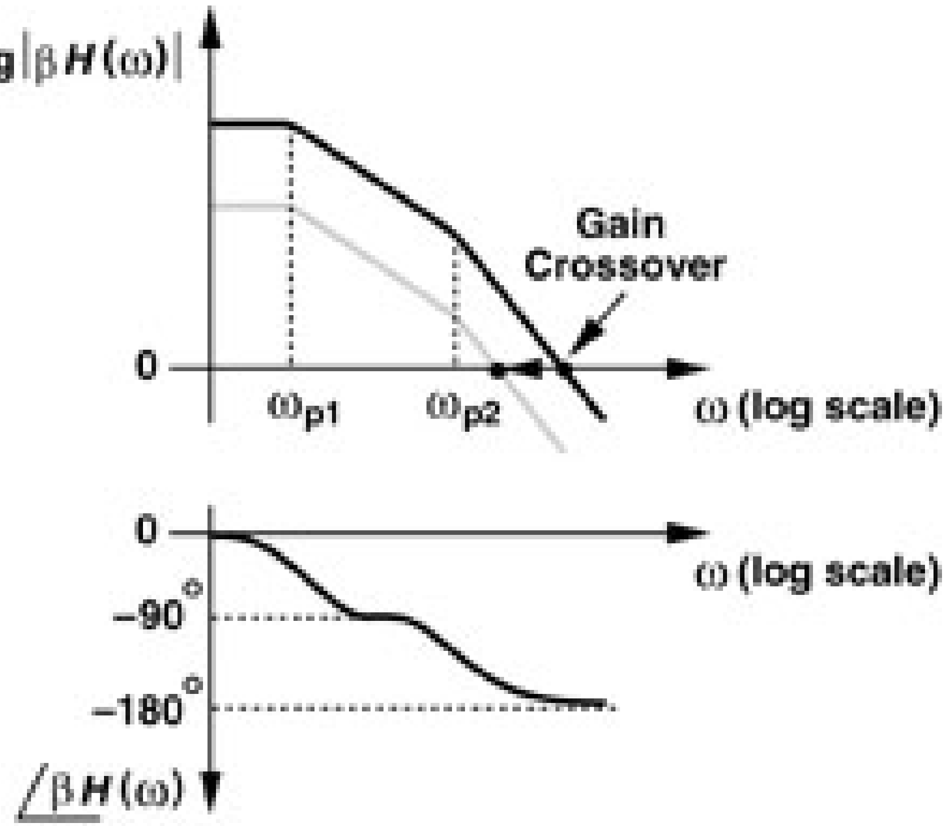
$$\frac{Y}{X}(s) = \frac{\dfrac{A_0}{1+\beta A_0}}{1 + \dfrac{s}{\omega_0(1+\beta A_0)}}$$

$$S_p = -\omega_0(1+\beta A_0)$$



Bode plot of the Loop gain

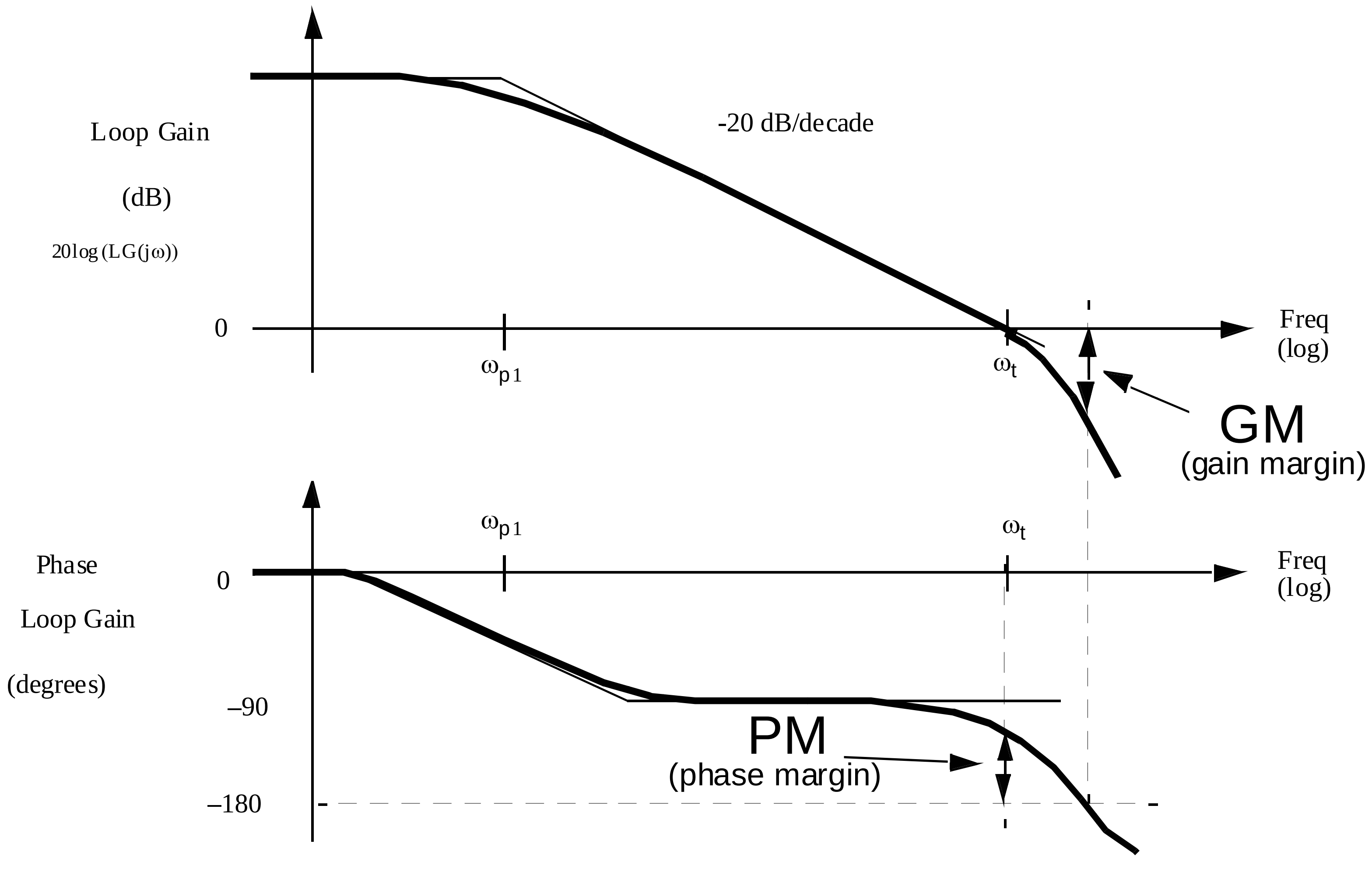
Multi-pole system



$$0.1\omega_{p2} > 10\omega_{p1}$$

Bode plot of the Loop gain

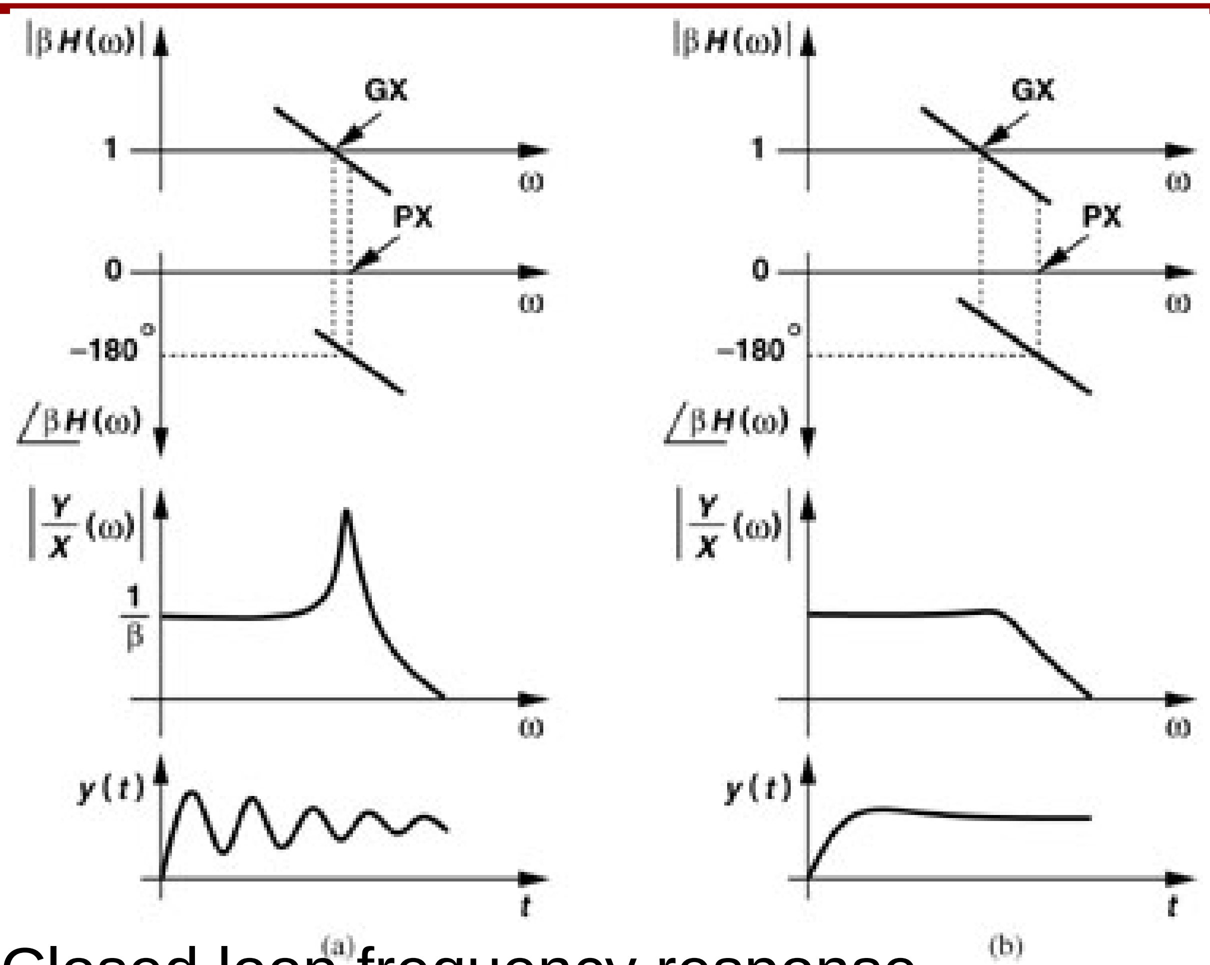
Phase Margin



Phase Margin

$$\beta H(\omega_1) = 1 \times e^{-j175}$$

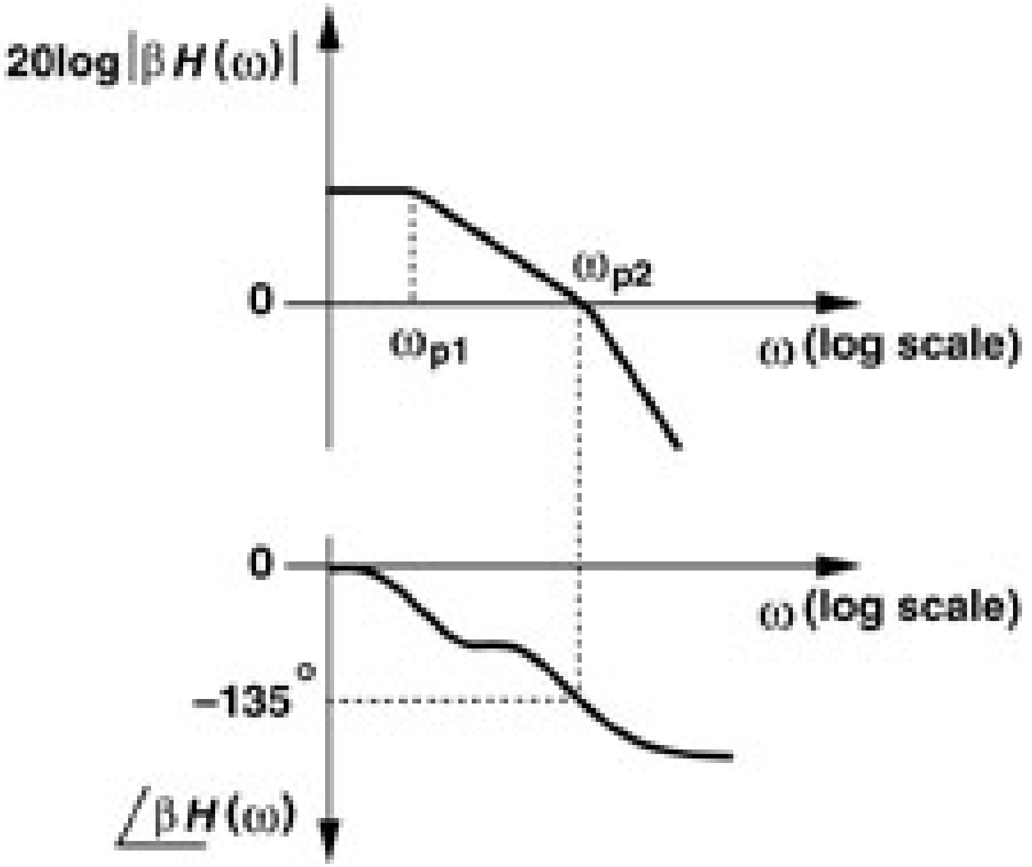
$$\left|\frac{Y}{X}(s)\right| = \frac{11.5}{\beta}$$



Closed loop frequency response

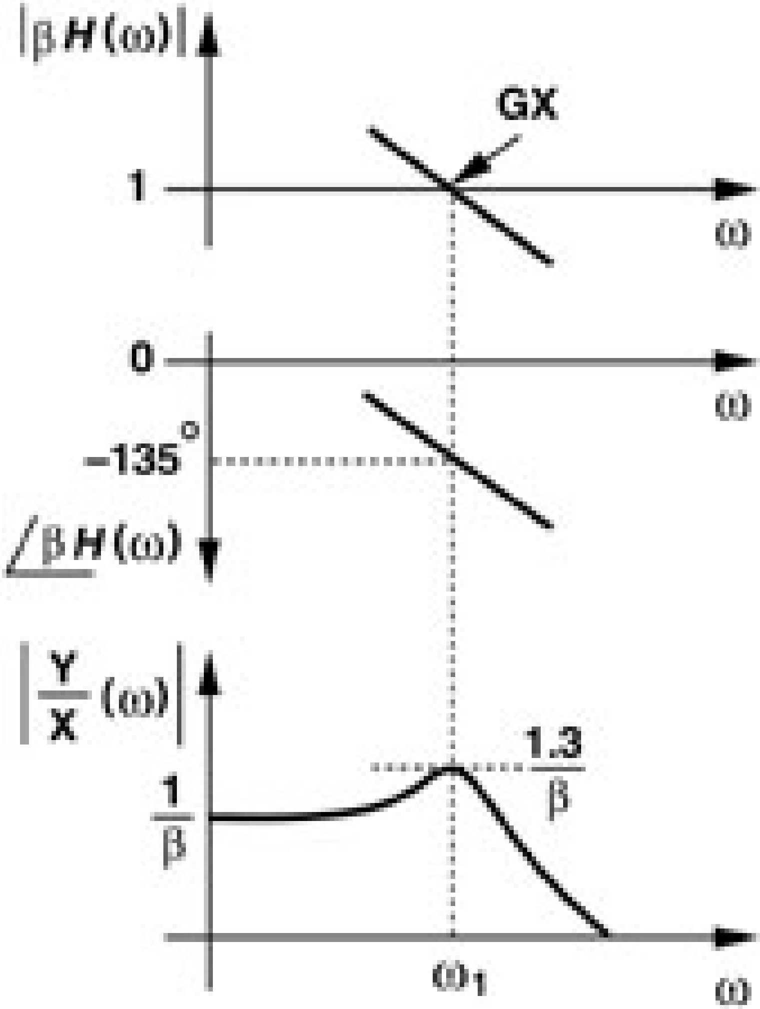
Phase Margin (Cont.)

$$PM = 180 + \angle \beta H(\omega_{GX})$$



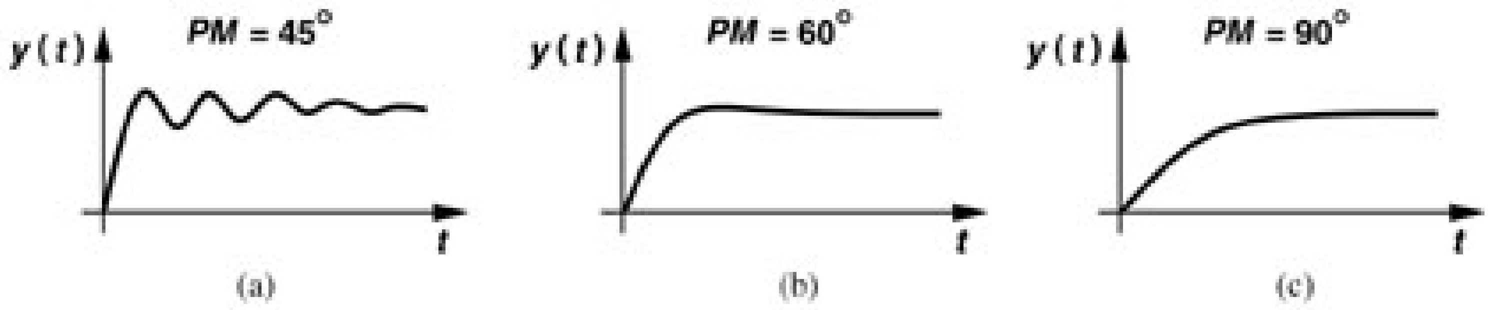
Phase Margin = 45°

Phase Margin (Cont.)



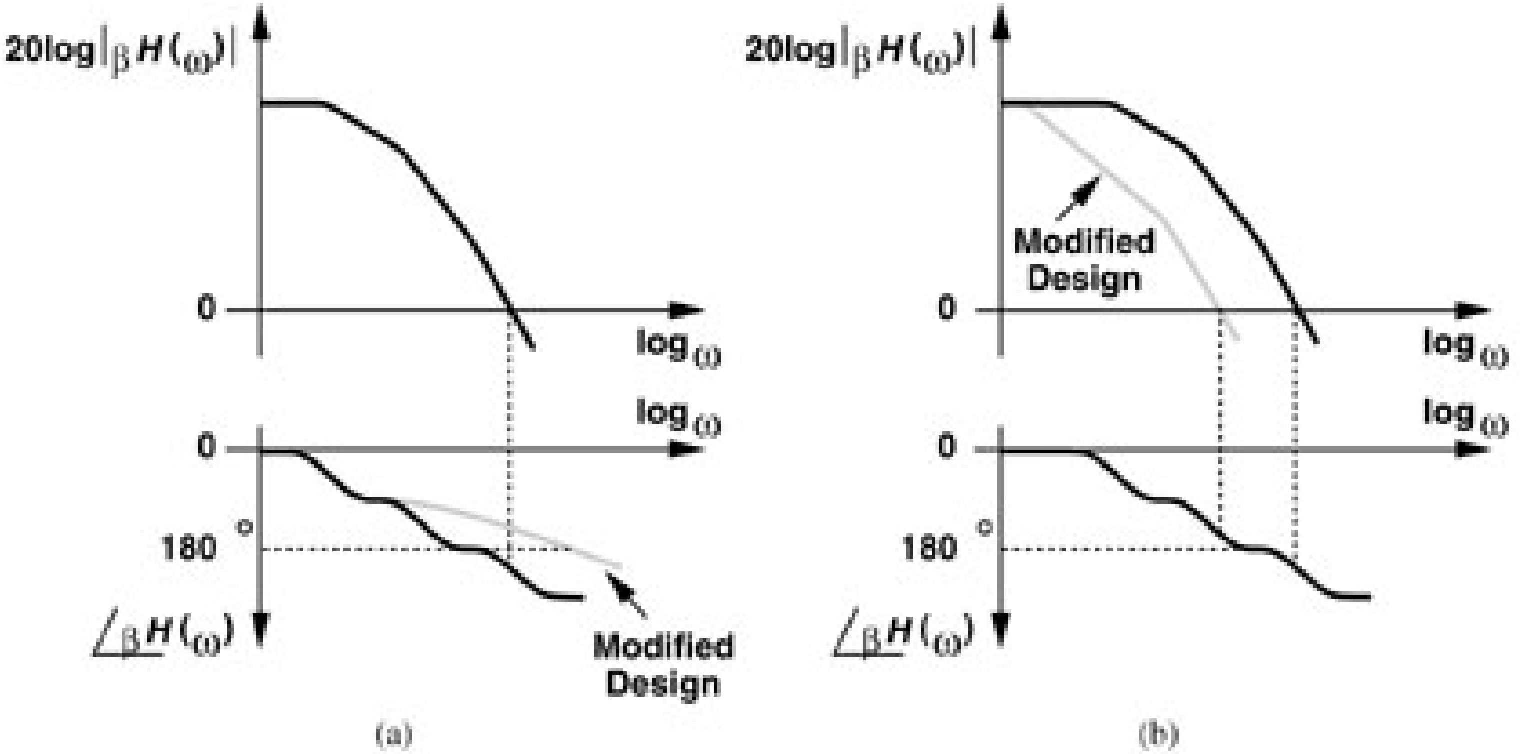
$$\text{Phase Margin} = 45°$$

Phase Margin (Cont.)



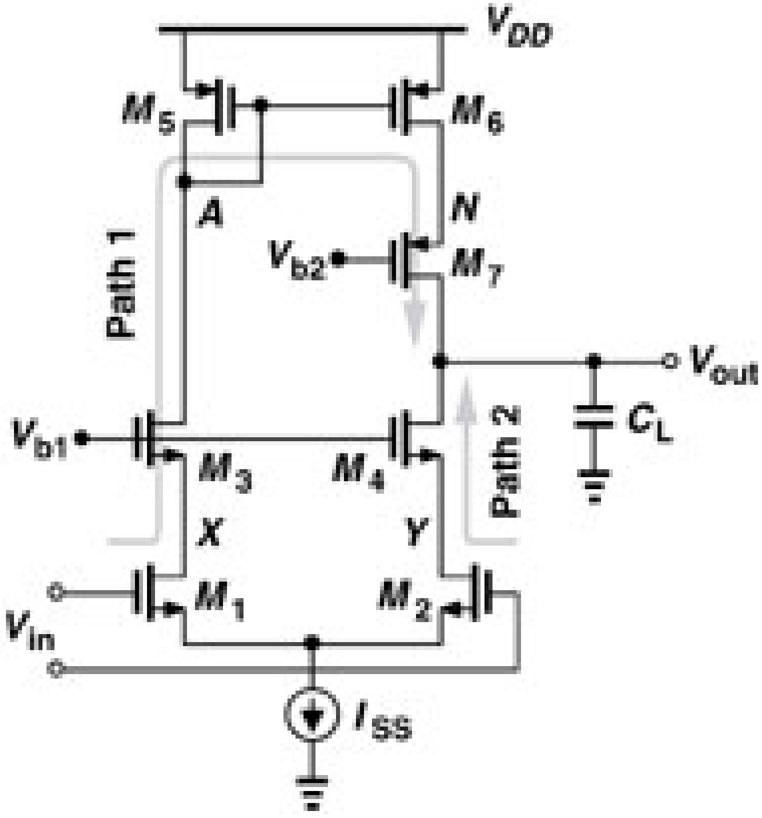
- At PM = 60º results in a small overshoot in the step response.
- If we increase PM, the system will be more stable but the time response slows down.

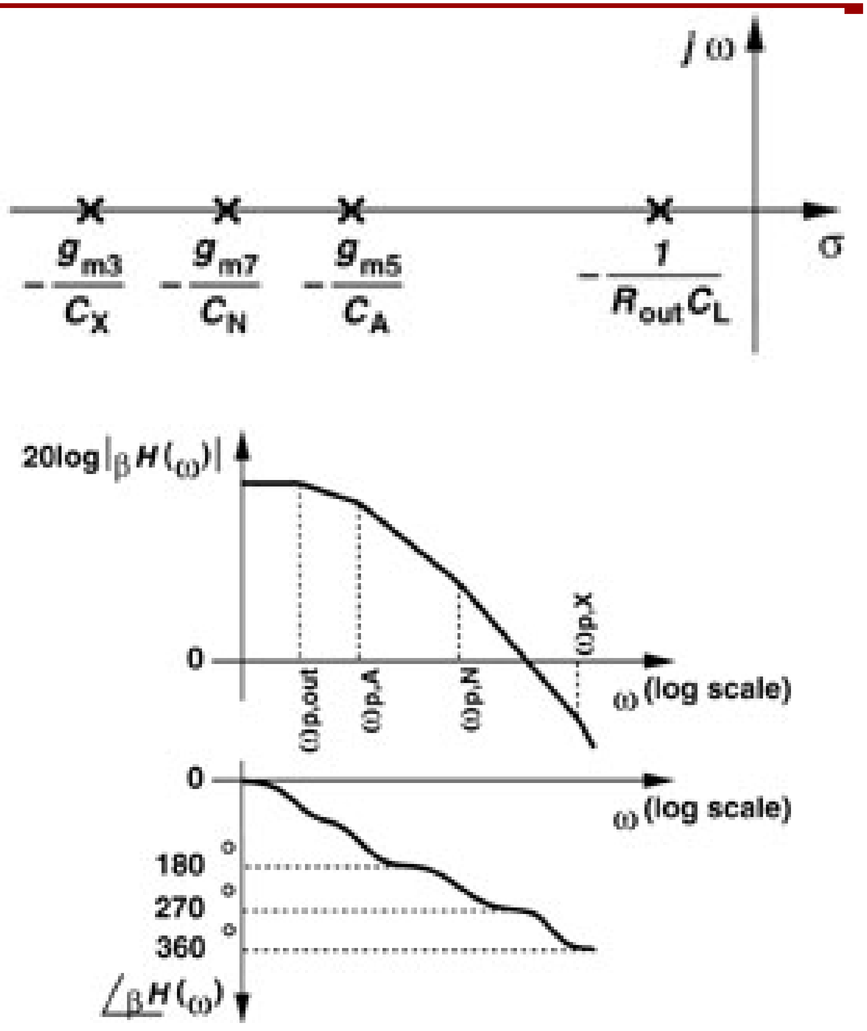
Frequency Compensation



- Push phase crossing point out
- Push gain crossing point in

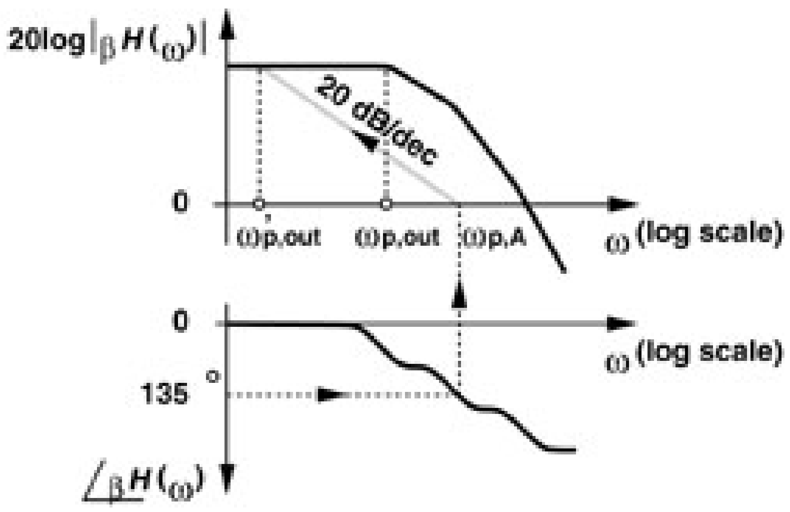
Telescopic Opamp (single-ended) -example

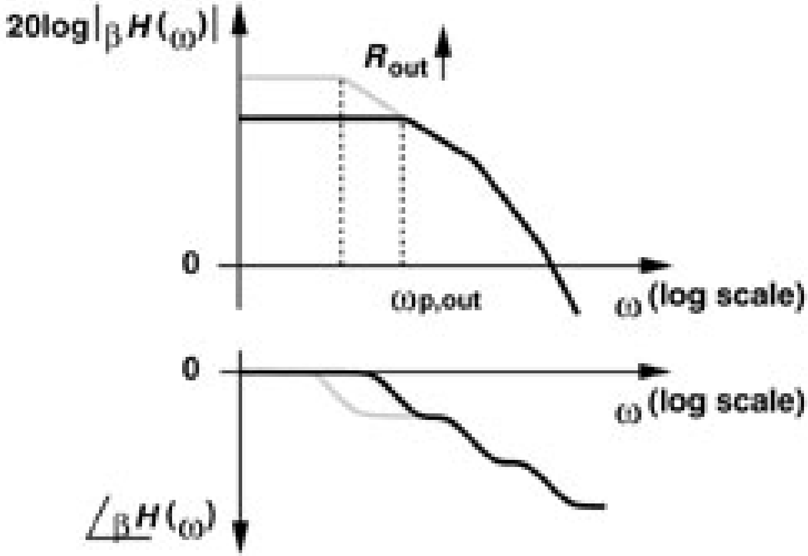




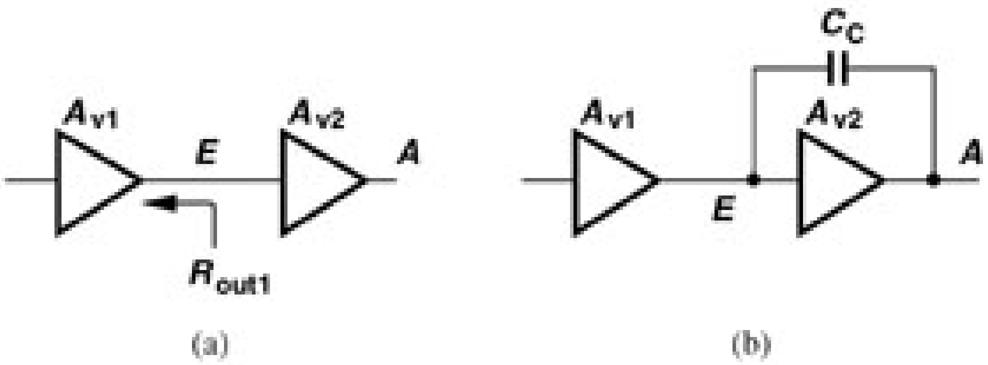
Compensation (Cont.)

• **Assume we need a phase margin of 45º (usually inadequate) and other non-dominant poles are at high frequency.**





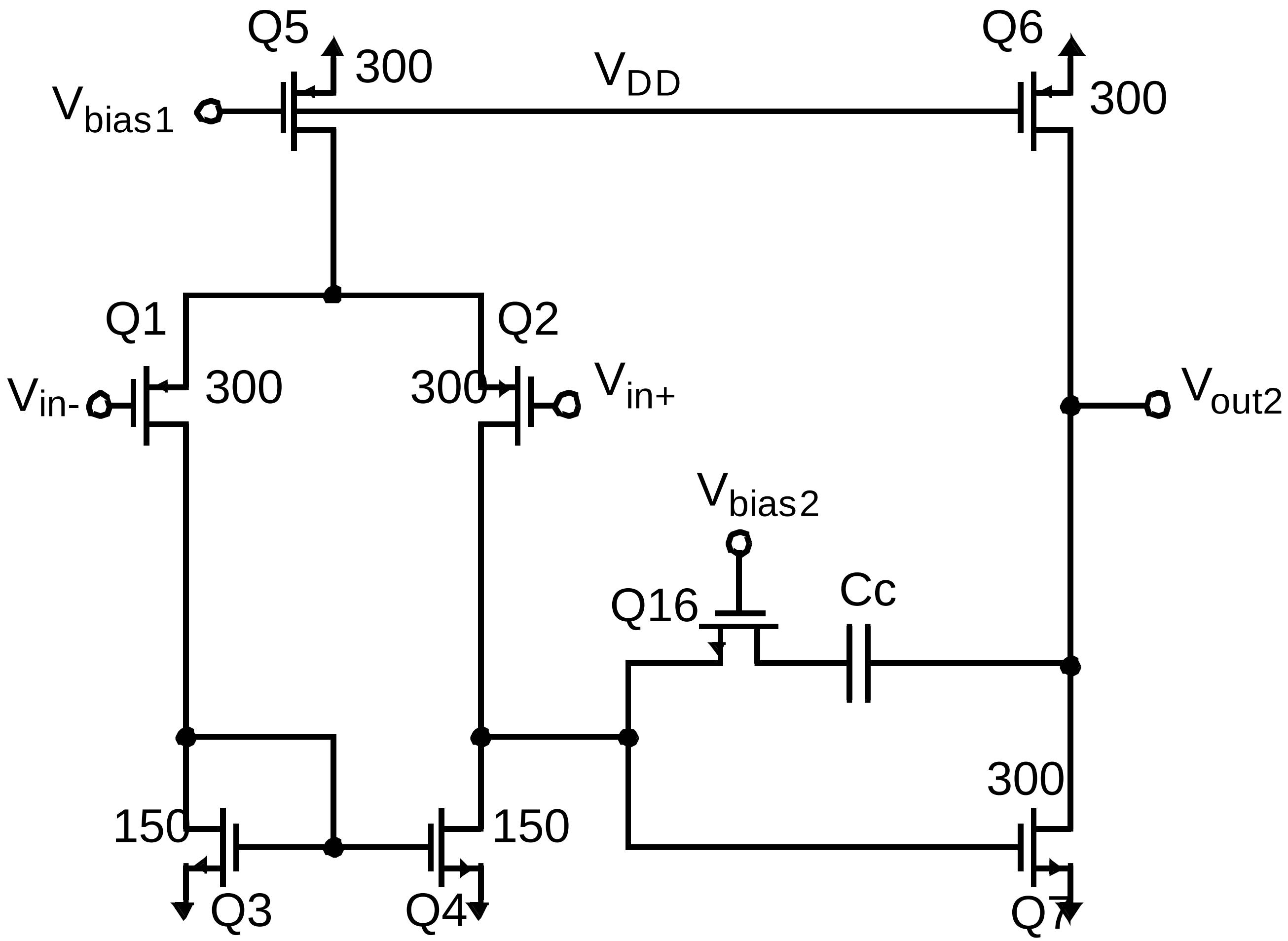
Compensation of a two-stage opamp



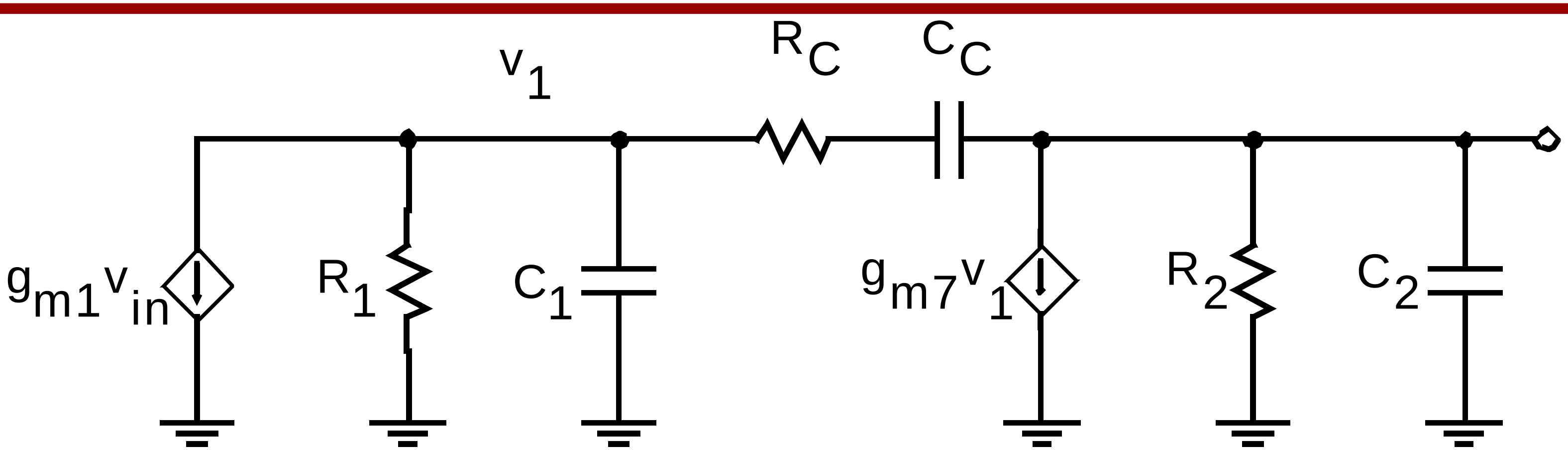
$$Miller \quad Effect \qquad C_{eq} = C_E + (1 + A_{v2})C_C$$

$$f_{pE} = \frac{1}{2\pi R_{out}[C_E + (1 + A_{v2})C_C]}$$

Compensating Two-Stage Opamps



Compensating Two-Stage Opamps



- Q16 has $V_{DS16} = 0$ therefore it is hard in the triode region.

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{16} V_{eff16}}$$

- Small signal analysis: without R_C, a right-half plane zero occurs and worsens the phase-margin.

Compensating Two-Stage Opamps

- Using R_C (through Q16) places zero at

$$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_C)}$$

- Zero moved to left-half plane to aid compensation
- Good practical choice is

$$\omega_z = 1.2\omega_t$$

- satisfied by letting

$$R_C \cong \frac{1}{1.2 g_{m1}}$$

since $\omega_t \cong g_{m1}/C_C$ and $\omega_z \cong 1/(R_C C_C)$ if $R_C \gg 1/g_{m7}$

Design Procedure

Design example: Find C_C with R_C=0 for a 55^o phase margin

- Arbitrarily choose C'_C=1pF and set R_C=0

- Using SPICE, find frequency ω_t where a –125° phase shift exists, define gain as A'

- Choose new C_C so ω_t becomes unity-gain frequency of the loop gain, resulting in a 55^o phase margin.

  Achieved by setting $C_C = C_C A'$

- Might need to iterate on C_C a couple of times using SPICE

Design Procedure

Next: Choose R_C according to

$$R_C = \frac{1}{1.2\omega_t C_C}$$

– Increasing ω_t by about 20 percent, leaves zero near final ω_t

– Check that gain continues to decrease at frequencies above the new ω_t

Next: If phase margin is not adequate, increase C_C while leaving R_C constant.

Design Procedure

Next: Replace R_C by a transistor

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{16} V_{eff16}}$$

SPICE can be used for iteration to fine-tune the device dimensions and optimize the phase margin.

Process and Temperature Independence

- Can show non-dominant pole is roughly given by

$$\omega_{p2} \cong \frac{g_{m7}}{C_1 + C_2}$$

- Recall zero given by

$$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_C)}$$

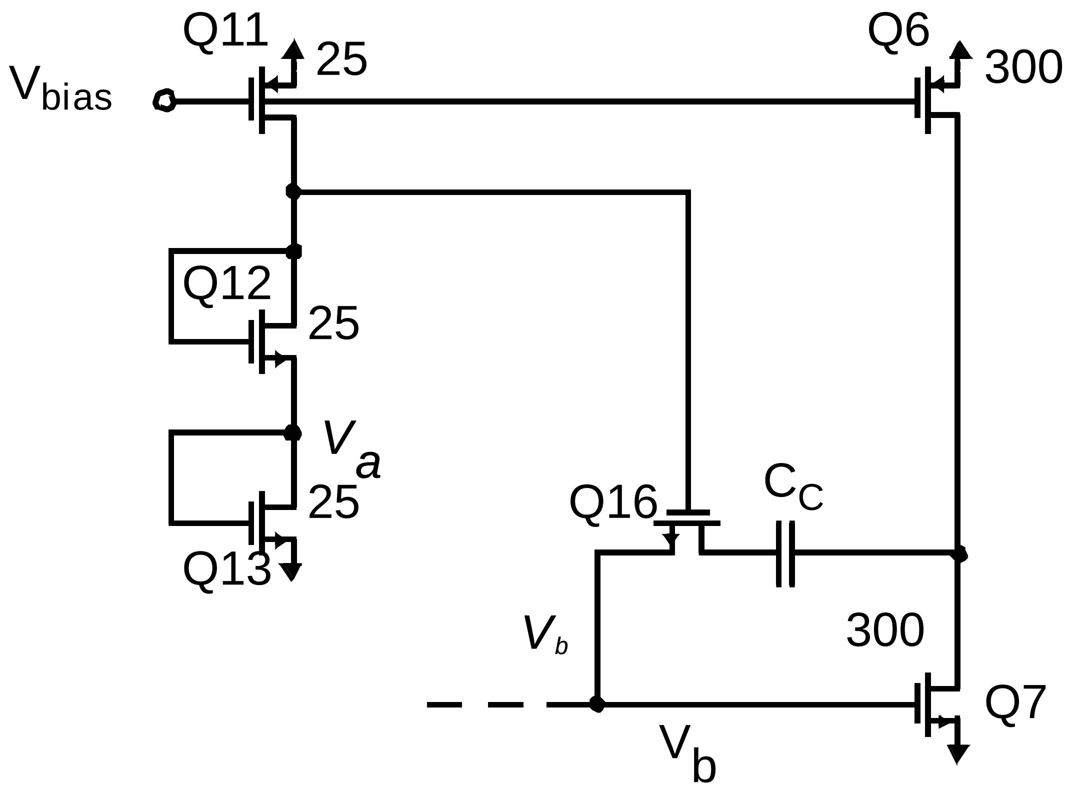
- If R_C tracks inverse of g_{m7} then zero will track ω_{p2}:

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}(W/L)_{16} V_{eff16}}$$

$$g_{m7} = \mu_n C_{ox}(W/L)_7 V_{eff7}$$

Process and Temperature Independence

- Need to ensure V_{eff16}/V_{eff7} is independent of process and temperature variations



- First set $V_{eff13}=V_{eff7}$ which makes $V_a=V_b$

Process and Temperature Independence

$$\sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}}$$

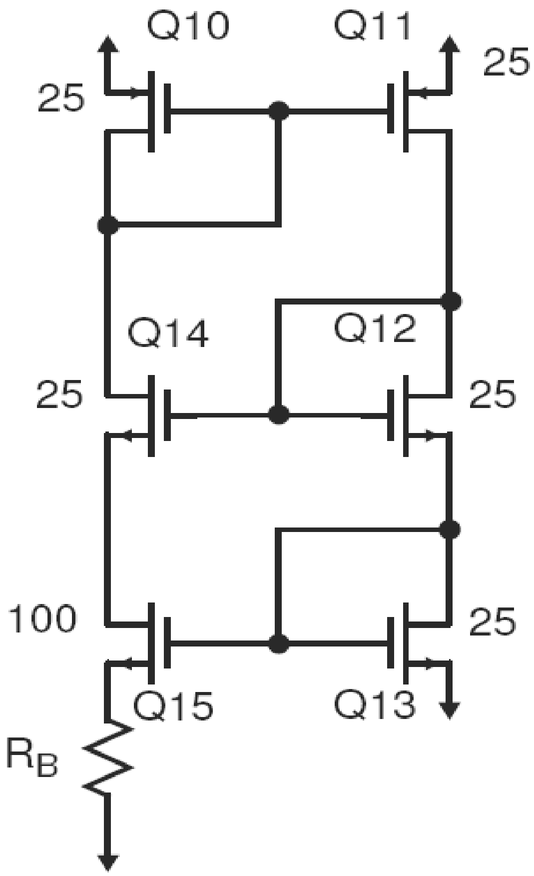
$$\frac{I_{D7}}{I_{D13}} = \frac{(W/L)_7}{(W/L)_{13}}$$

- Since $V_a = V_b$ and gates of Q12 and Q16 same

$$V_{eff12} = V_{eff16}$$

$$\frac{V_{eff7}}{V_{eff16}} = \frac{V_{eff13}}{V_{eff12}} = \frac{\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}}}{\sqrt{\frac{2I_{D12}}{\mu_n C_{ox}(W/L)_{12}}}} = \sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}$$

Stable Transconductance Biasing



- Can bias on-chip g_m to a resistor

$$V_{GS13} = V_{GS15} + I_{D15} R_B$$

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D15} R_E$$

- But $I_{D13} = I_{D15}$ and rearrange

$$\frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}}\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right] = R_B$$

- Recall $g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}$

$$g_{m13} = 2\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right] / R_B$$

Stable Transconductance Biasing

- Transconductance of Q_{13} (to the first order) is determined by geometric ratios only.
- Independent of power-supply voltages, process parameters, temperature, etc.
- For special case $(W/L)_{15}=4(W/L)_{13}$

$$g_{m13}=1/R_B$$

- Note that high-temperature will decrease mobility and hence increase effective gate-source voltages.
- Roughly 25% increase for 100 degree increase
- Requires a start-up circuit (might have all 0 currents)