ELEC 401: Analog CMOS Integrated Circuit Design

A Brief Overview of ADCs

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Reference

- Main reference

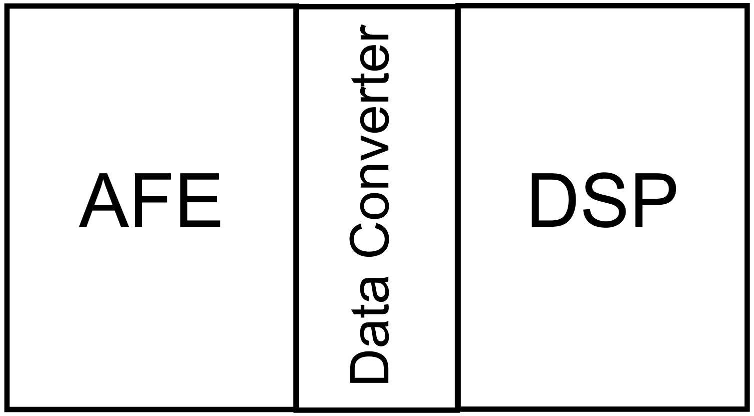
📖 D. Johns and K. Martin, *Analog Integrated Circuit Design*, 1st Edition, John Wiley, 1997

📖 T. Chan Carusone, D. Johns and K. Martin, Analog Integrated Circuit Design, 2nd Edition, John Wiley, 2011

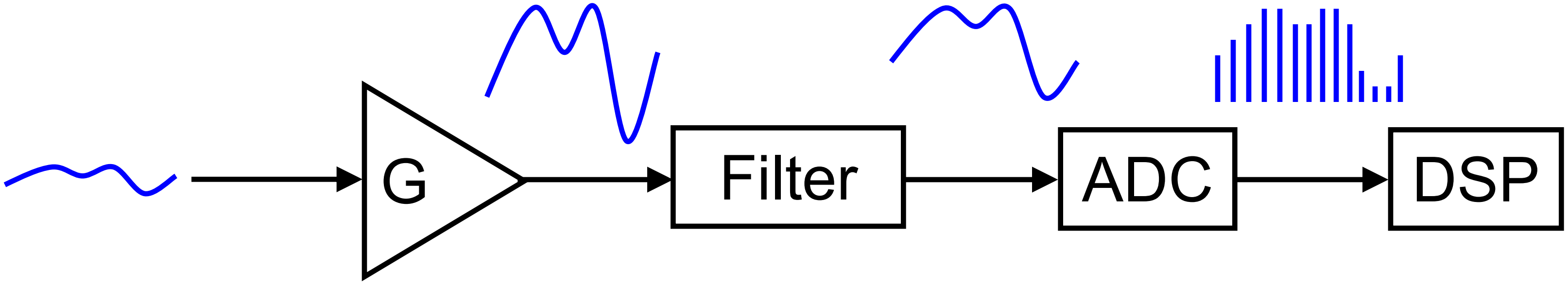
Why Analog-to-Digital Converters?

- Interface real-world signals with digital electronics
  - Most physical signals (temperature, sound, light, pressure, RF signals, sensor outputs) are analog. Digital systems (processors, FPGAs, SoCs, microcontrollers) can only process digital data, so conversion is required.
- Enable digital signal processing (DSP)
  - Functions such as filtering, compression, modulation, demodulation, and machine-learning inference require signals to be in digital form.
- Allow storage in digital memory
  - It is much easier to store digital signals than analog signals;
- Improve noise immunity
  - Digital signals are more robust to noise during processing and transmission.
- Enable precise, repeatable computation
  - Digital operations are deterministic and support complex algorithms that are difficult or impossible in analog circuits.
- Enable software-defined functionality
  - Once a signal is digitized, functionality can be changed by software updates rather than hardware redesign.

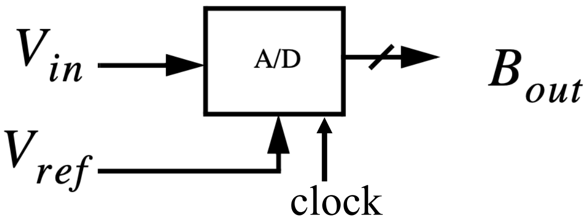
Typical Real World System



- Example:



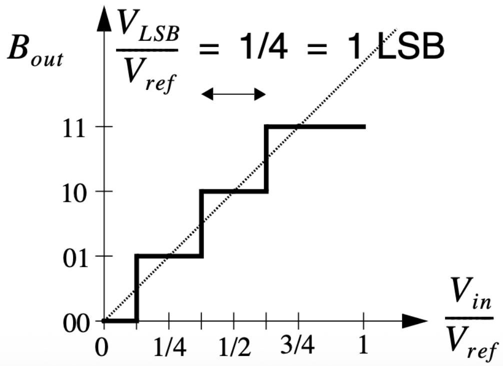
ADC Basics



$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm x$$

$$\text{where } \left(-\frac{1}{2}V_{LSB} < x < \frac{1}{2}V_{LSB}\right) \qquad (1)$$

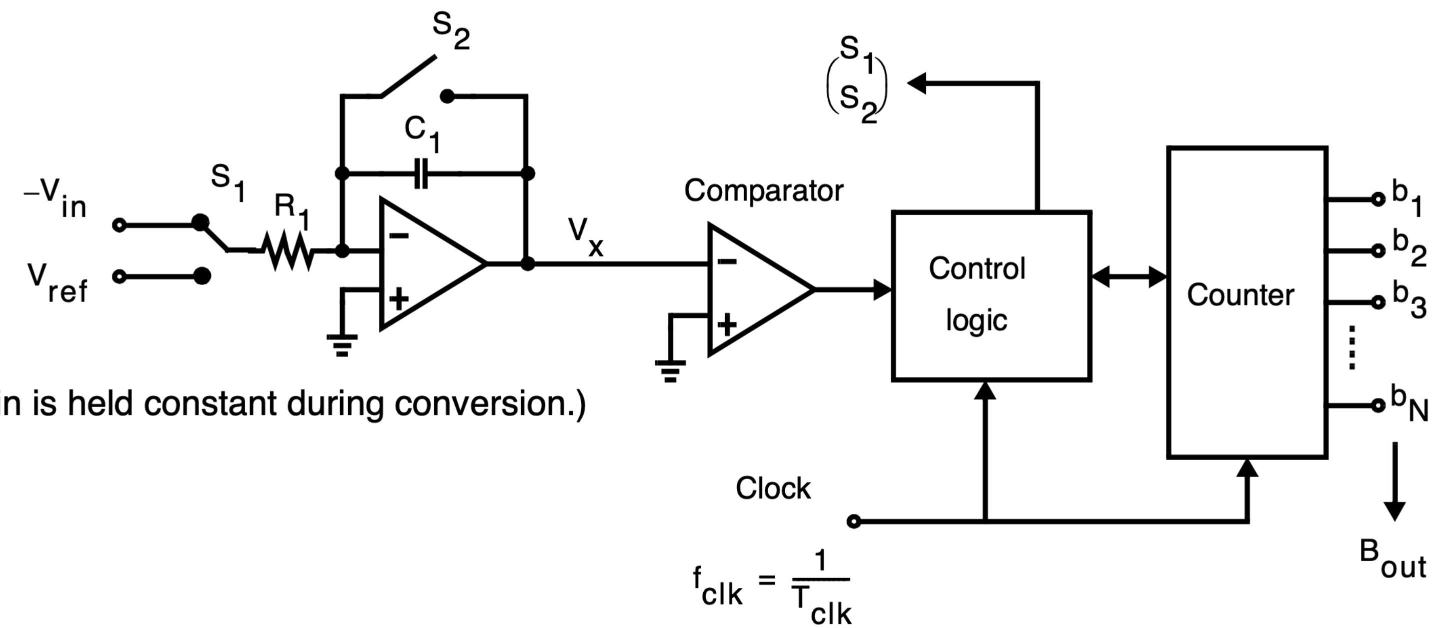
- A range of valid input values produce the same output signal — quantization error.



Different ADC Architectures

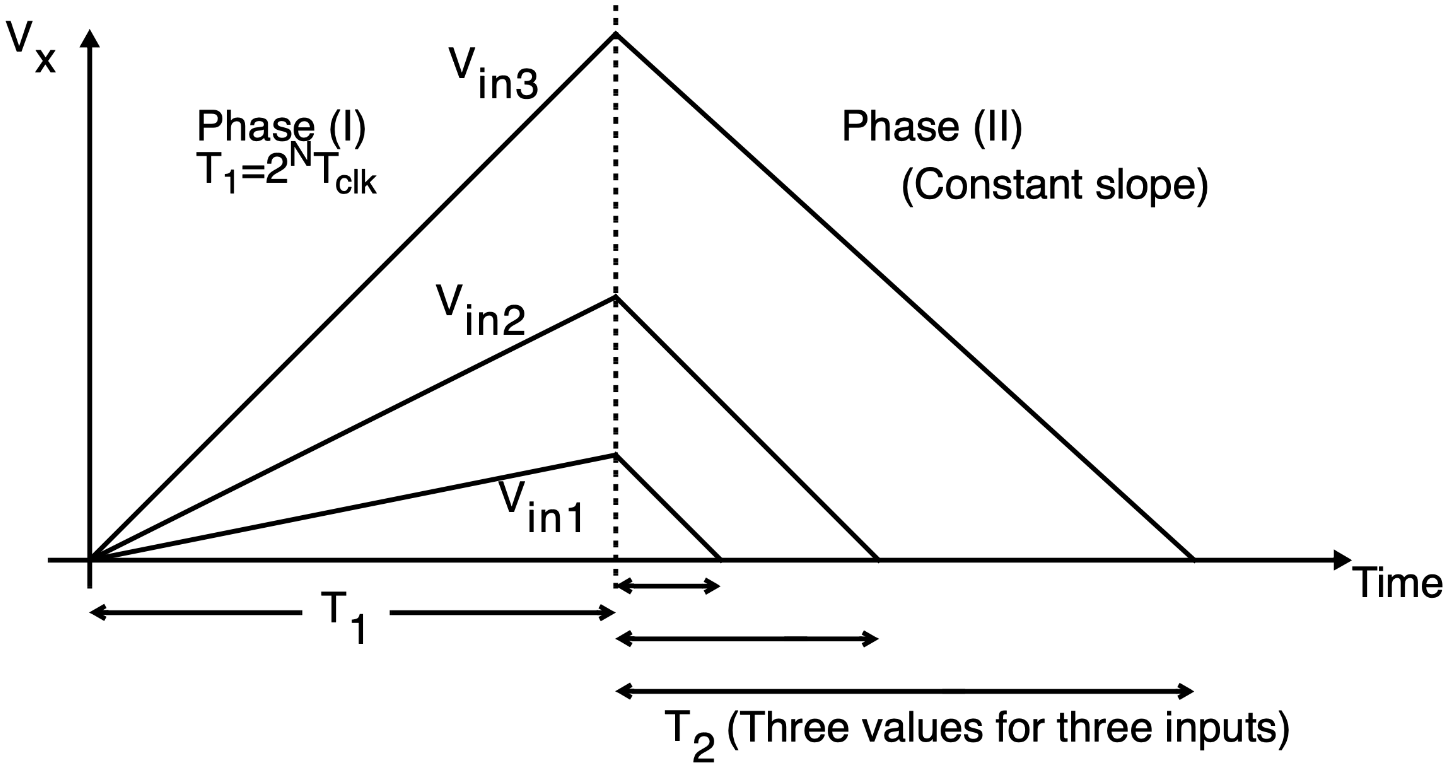
Low to Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low to Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling (not Nyquist-rate)	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

Integrating ADCs



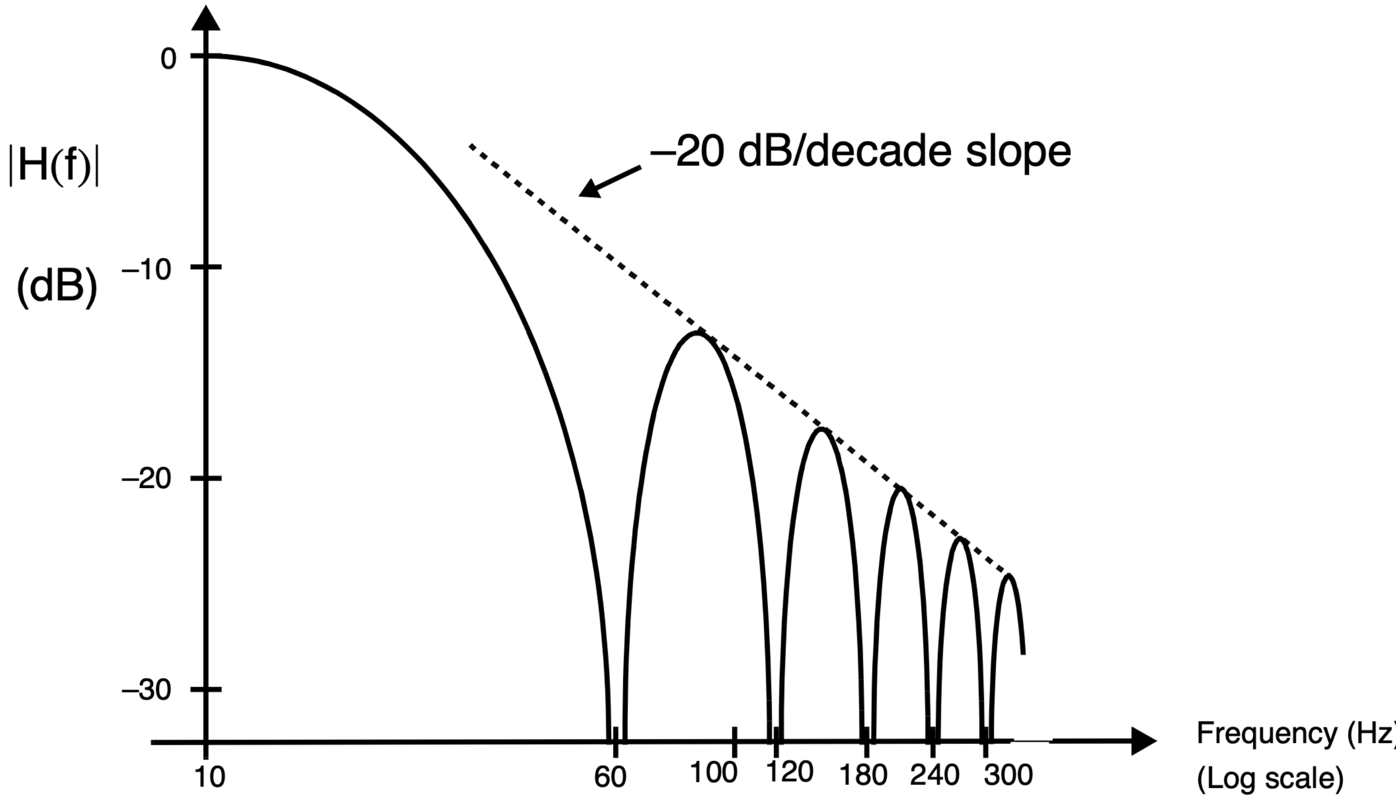
(Vin is held constant during conversion.)

Integrating ADCs



- Count at end of T_2 is digital output
- Does not depend on RC time-constant

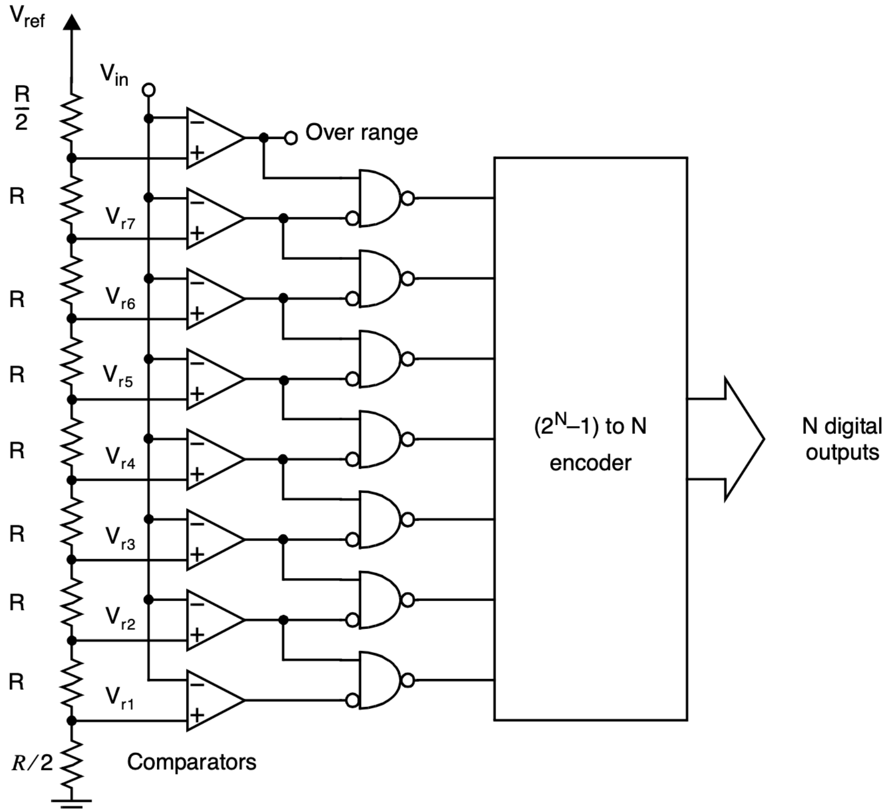
Integrating ADCs



- Notches the input frequencies which are multiples of $1/T_1$

Flash (Parallel) ADCs

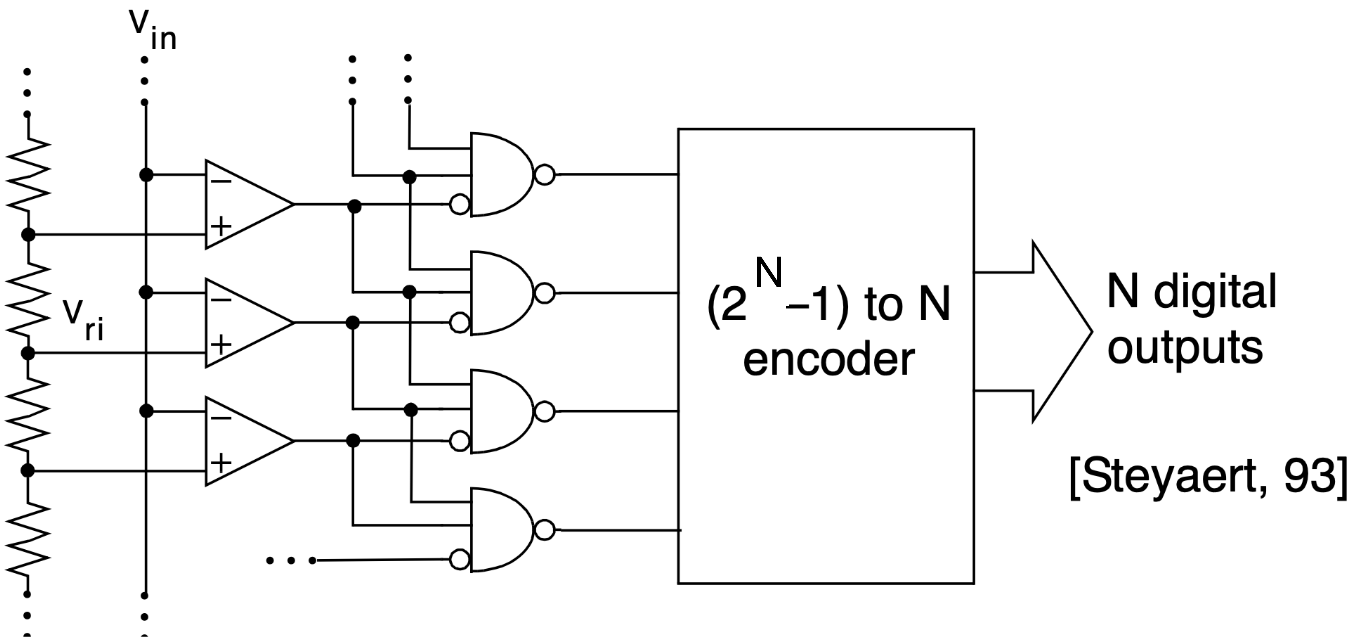
- Peetz, 86; Yoshii, 87; Hotta, 87; and Gendai, 91



- High-speed
- Large size and typically power hungry
- 2^N comparators
- Speed bottleneck is usually the large capacitive load at input
- Thermometer code out of comps
- Nands used for simpler decoding and/or bubble error correction
- Use comp offset cancellation

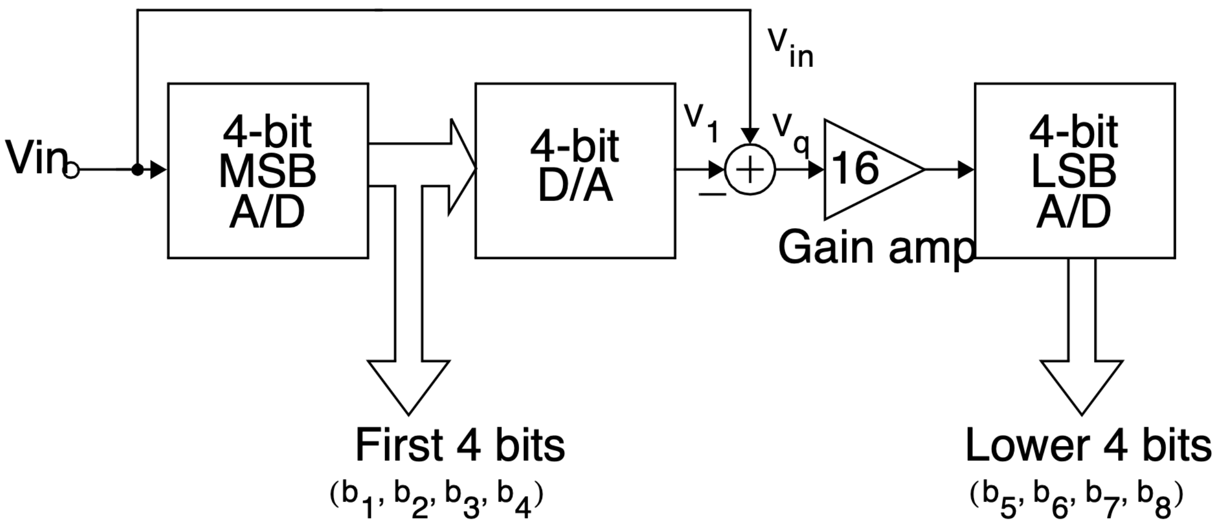
Flash ADCs: Bubble Errors

- Thermometer code should be 1111110000
- Bubble error (noise, metastability) — 1111110100
- Usually occurs near transition point



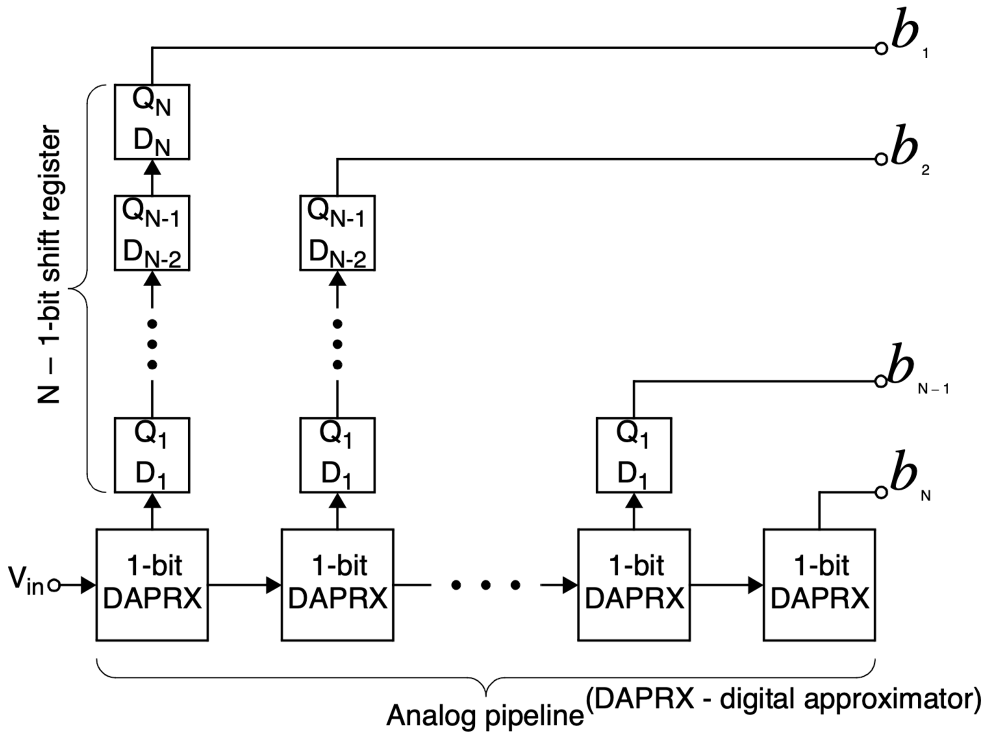
[Steyaert, 93]

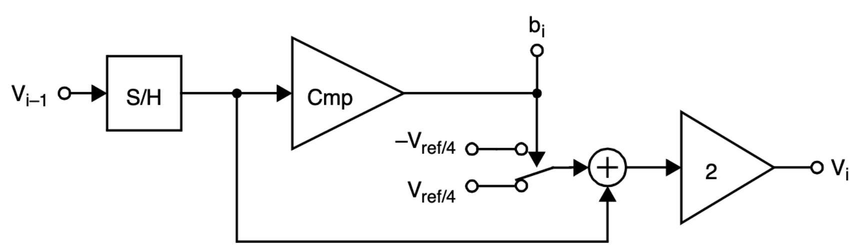
Two-Step ADCs



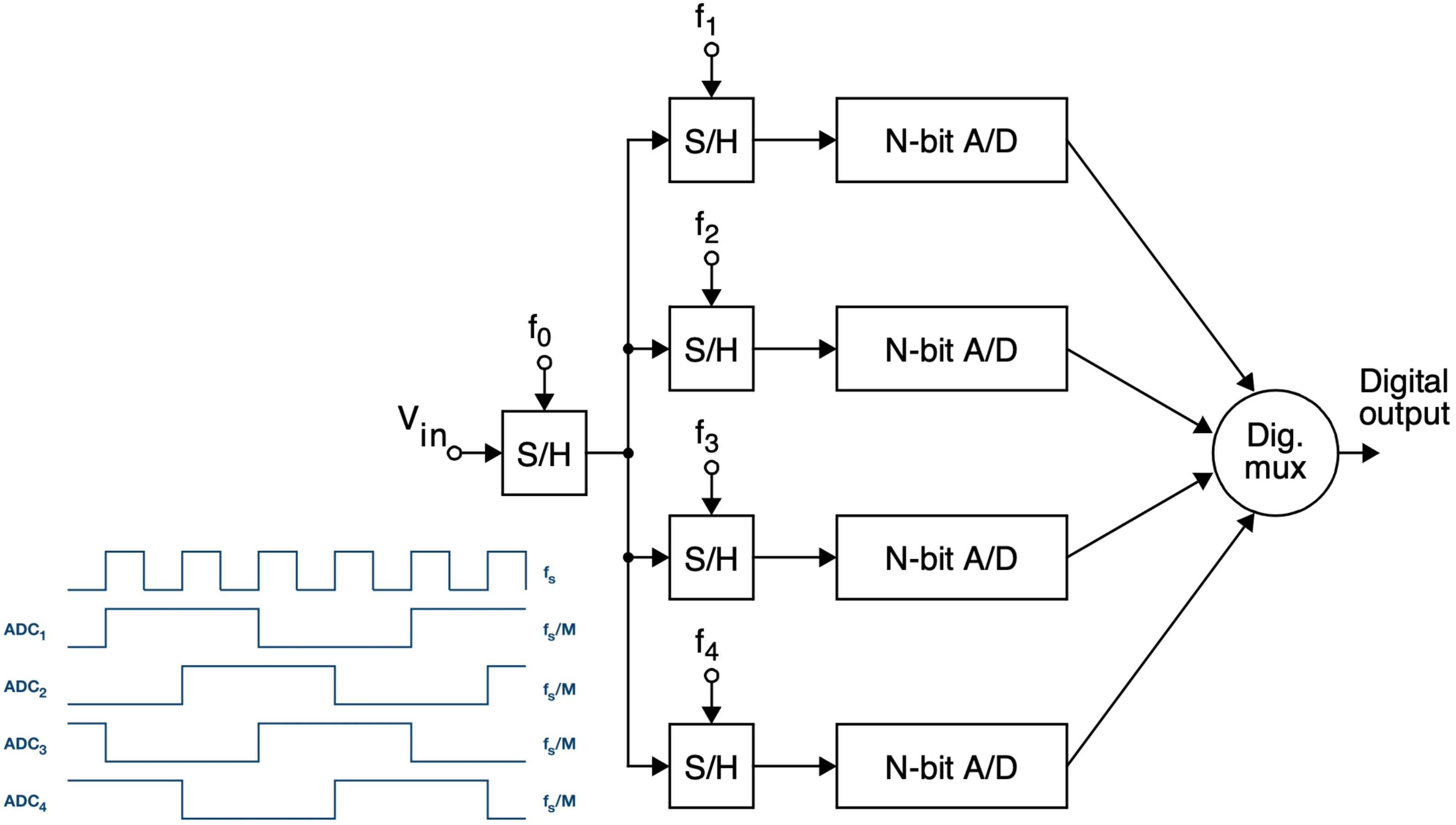
- High-speed, medium accuracy (but 1 sample latency)
- Less area, power, and capacitive loading than flash
- 32 comparators for 8-bit two-step (256 for flash)

Pipelined ADCs





Time-Interleaved ADCs



- Use parallel A/Ds and multiplex them