UNIVERSITY OF BRITISH COLUMBIA

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EECE 479 – Introduction to VLSI Systems

Fall 2007

Review for the Final Exam

The final exam date, time, and location will be as announced on the university exam schedule. You will have up to 150 minutes to complete the exam.

You are allowed to bring ***two*** single-sided ***handwritten*** sheets of notes to the midterm (or one double sided sheet). I suggest you bring a calculator.

The 2005 and 2006 exams are on the course web-site, along with answers. Although the questions will be different you should expect the style and format of the questions to be similar.

The final exam will cover the entire course, including all Slide Sets, and all notes/problems that were presented on the board. The emphasis will be on the material since the midterm, but there will be a few questions on the material before the midterm as well.

The following summarizes the material from Slide Set 10 onwards. You also should read the summaries on the handout "Review for the Midterm" that you received in October (it is on the web site too).

Slide Set 10: Implementation Options: We talked about FPGAs, Gate Arrarys/Structured ASICs, Standard Cells, Datapath layouts ("snap-together" cells), SoC design, and platform based design. You should be able to compare these methods in terms of area, power, speed, and design time.

Slide Set 11: MOS Circuit Styles: NMOS Technology, Pseudo-NMOS, DCVS, Dynamic Logic, Domino Logic, Differential Domino, np-CMOS. For each of these, you should be able to design or analyze a simple gate, and explain the advantages or disadvantages of each circuit style. We talked a bit about charge sharing as well (it would be good to understand this).

Slide Set 12: More about timing. You should be able to estimate the delay of a network using the Elmore Delay (using resistances and capacitances that you calculate). The network might contain long wires, meaning you'd have to understand the pi-model for a wire. In addition, you should be able to compare different circuits using Logical Effort.

Slide Set 13: Power: There were two parts to this: estimating power and designing for low power. For the first part, you should expect a question which requires you to calculate the activity of nodes, and hence estimate dynamic power. You should understand the difference between dynamic, static, and short circuit power. Given a power-reduction method, you should be able to talk about how it reduces power, and what component of power (switching, short-circuit, or leakage) that it reduces.

Slide Set 14: Design for Testability. You should understand the different types of testing, and what sort of errors each type can help you find. You should understand what fault coverage is, and be able to estimate it given a circuit and set of test vectors. You should understand what

scan-design is, and be able to estimate the overhead inherent in scan design. You should understand what BIST is, and when it is useful.

This isn't a complete list. But it will give you a place to start.

In addition to the notes, there may be some questions related to the Assignments/Project. For example, in a previous exam, I asked people what ext2sim program did. I don't think you really can study this very much; if you have done and understood the project you will have no problem with these questions.

Finally, if you see a question on the test that you haven't seen before, don't freak out. There will likely be at least one question that requires you to think far beyond what we have talked about in class. If you see a question you can't answer, just think about it, and see if you can come up with a solution, or at least a partial solution.

REMINDER: OFFICE HOURS ARE SET UP FOR EVERY DAY BETWEEN NOW AND THE FINAL. THE SCHEDULE IS ON THE WEB SITE AND IS SUBJECT TO CHANGE. I WILL BE IN JAPAN FROM DECEMBER 6th SO IF YOU WANT TO SEE ME, YOU NEED TO DO SO BEFORE THEN. CINDY WILL HAVE EXTENDED OFFICE HOURS WHILE I AM GONE.