UNIVERSITY OF BRITISH COLUMBIA

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EECE 479 – Introduction to VLSI Systems

Fall 2007

Review for the Midterm

Remember that the midterm will be held on October 31st, in class, from 1:00pm to 2:15pm. Since there is another class booked in our room we will need to end precisely at 2:15pm. So please show up on-time, otherwise you won't have as long as everyone else to complete the midterm.

You are allowed to bring one single-sided ***handwritten*** sheet of notes to the midterm (for the final exam, you will be allowed to bring two hand-written sheets). I actually don't know what you could put on this sheet that would be useful, but some people find it more comforting to have some notes available.

A midterm from last year is on the course web-site. Although the questions will be different (sorry!) you should expect the style and format of the questions to be similar. Note that there are some differences in the material each year.

In terms of material, the midterm will cover everything up to the end of Slide Set 10. More specifically, we have covered this (this is not complete list):

Slide Set 1: Introduction: not a lot to study here

Slide Set 2: Layout and CMOS gates: you might be asked to design a CMOS gate, asked about advantages and disadvantages of CMOS vs. NMOS, convert from circuit design to layout and vice-versa

Slide Set 3: Pass Transistor Logic: you should be able to design/analyze a circuit constructed using pass-transistor logic. You should also be able to speak intelligibly about degraded outputs, whether they are a problem, and ways to avoid them.

Slide Set 4: Layout and Design Rules: I have given a lot of pointers about what makes a good layout in these notes. You should understand why each of these pointers is important (ie. speed, design time, etc.). I wouldn't expect you to memorize design rules, however, you should be able to use these rules to comment on layouts, as well as quickly estimate the size of a layout.

Slide Set 5: Resistance and Capacitance: The interaction between layout parameters and the speed of a circuit is important. This involves understanding how layout affects the resistance of a path and the capacitance of a node. You should be able to calculate these quantities given a layout and process information. Don't memorize the actual constants in the tables, because this information would be given to you if you need it, but the relationship between layout parameters and resistance/capacitance (and hence speed) is important. As an example, see Question 5 on last year's midterm. You should be able to estimate the delay of inverters and more complex gates, and be able to size transistors to achieve equal worst-case pull-up and pull-down times.

Slide Set 6: This slide presented some additional layout hints, including transistor folding. You should be able to tell me the advantages/disadvantages of various layouts, and should be able to quantify the advantages of transistor folding.

Slide Set 7: You should be able to talk about dynamic latches, static latches, and master-slave flip-flops. You should understand clock skew and how it affects system design. You should understand two-phase clocking, and be able to correctly label the timing-types of nodes (as in the first question of Assignment 4… the answers to these questions will be on the website…. don't worry about the second question for now, since that involves dynamic logic, which we'll talk about after the midterm).

Slide Set 8: Verilog: There is a lot of information about the CAD flow here that you should know. You should the basics of Verilog. I won't ask you to write any Verilog on the exam though.

Slide Set 9: Memories: You should understand how memory cells work, and the basic design considerations for all the peripheral circuits (decoders, wordline drivers, etc.). You also talked about DRAM cells, so it is good to understand how they work.

Slide Set 10: Implementation Options: We talked about FPGAs, Gate Arrarys/Structured ASICs, Standard Cells, Datapath layouts ("snap-together" cells), SoC design, and platform based design. You should be able to compare these methods in terms of area, power, speed, and design time.

This isn't a complete list. But it will give you a place to start.

I am sure you didn't realize we had covered this much! In addition to the notes, there may be some questions related to the Assignments. I don't think you really can study this very much; if you have done and understood the assignments, you will have no problem with these questions.