THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
EECE 479 – Introduction to VLSI Systems

Use of one single-sided hand-written sheet and a calculator is permitted.
Answer all problems.
Time: 75 minutes.

This examination consists of 10 pages. Please check that you have a complete copy. You may use both sides of each sheet if needed.

MY ANSWERS

Surname First name

Student Number

#	MAX	GRADE
1	5	
2	7	
3	5	
4	6	
5	5	
6	4	
7	4	
TOTAL	36	

READ THIS →

IMPORTANT NOTE: The announcement "stop writing" will be made at the end of the examination. Anyone writing after this announcement will receive a score of 0. No exceptions, no excuses.

All writings must be on this booklet. The blank sides on the reverse of each page may also be used.

Each candidate should be prepared to produce, upon request, his/her Library/AMS card.

Read and observe the following rules:

No candidate shall be permitted to enter the examination room after the expiration of one-half hour, or to leave during the first half-hour of the examination.

Candidates are not permitted to ask questions of the invigilators, except in cases of supposed errors or ambiguities in examination-questions.

***Caution** - Candidates guilty of any of the following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:*

Making use of any books, papers or memoranda, calculators, audio or visual cassette players or other memory aid devices, other than as authorized by the examiners.

Speaking or communicating with other candidates.

Purposely exposing written papers to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

REMINDER: $m=10^{-3}$, $\mu=10^{-6}$, $n=10^{-9}$, $p=10^{-12}$, $f=10^{-15}$

Eg: $32\ ps = 3.2 \times 10^{-11}\ s$

1. TRUE OR FALSE: Label each statement with "T" or "F". Be very clear. Answers that look like a combination of a T and F will be wrong. [1 mark each]

Statement	T/F
A CMOS gate with n inputs always has $2n+1$ transistors.	F
Since an SRAM cell contains more transistors than a DRAM cell, SRAM will typically be slower than DRAM.	F
Transistor folding is a technique to reduce the gate capacitance of a wide transistor.	F
A NAND gate composed entirely of minimum-sized transistors will have a pull-up time (time to drive the output from 0 to 1) that is smaller than the pull-up time of a NOR gate composed entirely of minimum-sized transistors.	T
A VLSI Designer might use an "H-Tree" distribution network to achieve *low skew* in the clock distribution network.	T

2. SHORT ANSWERS:

a) In layout tools like Magic, explain what "extraction" is used for. Do not use the word "extract" in your answer. [2 marks]

To create a text file from a layout. The text file contains a description of the trasistors, parasitics, and their connections.

b) What is high-level synthesis? Be specific. Do not use the words "synthesis" or "high level" in your answer. [2 marks]

Create an RTL-level description from an algorithmic description

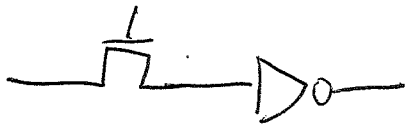
c) Give one *advantage* of using a **Structured ASIC** compared to using an **FPGA**. Be specific. [1 mark]

- more dense
- faster
- cheaper in large volumes

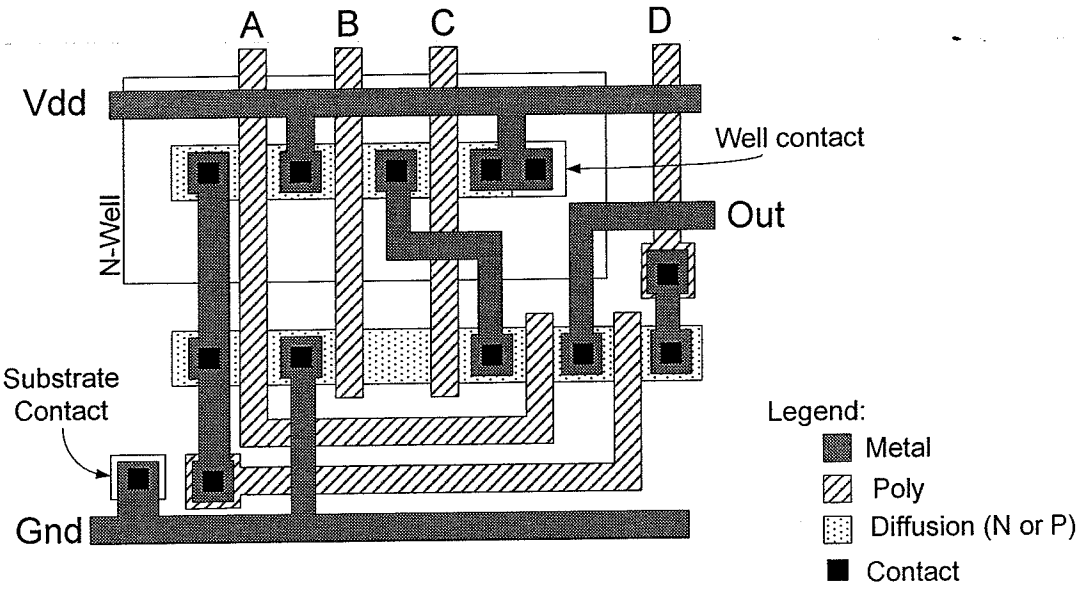
d) In Verilog, a variable can be declared as either a **reg** or a **wire**. Clearly and concisely explain the difference between **reg** and **wire**. [1 mark]

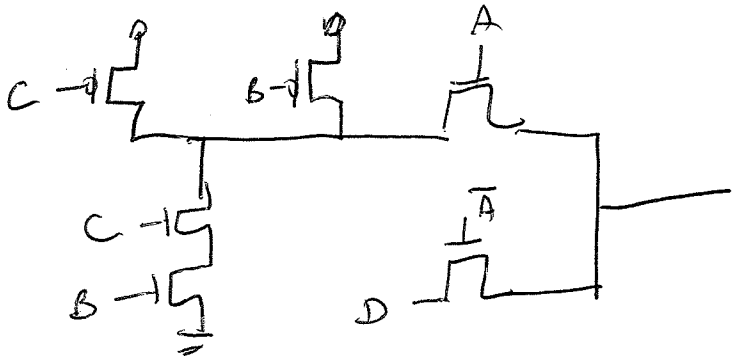
reg: created by an always block
wire: created by an assignment

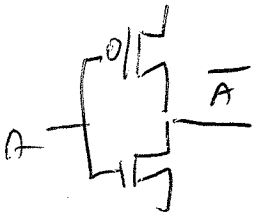
e) Draw a transistor-level schematic for a *dynamic latch*. [1 mark]



3. a) The following circuit has inputs **A, B, C, and D**, and output **Out**. Write the function implemented by the layout. Present your answer as a logic equation. [3 marks] Use reverse of previous page for rough work.







Out = $A(\overline{BC}) + \bar{A}D$.

b) Does this circuit suffer from degraded outputs? [1 mark]

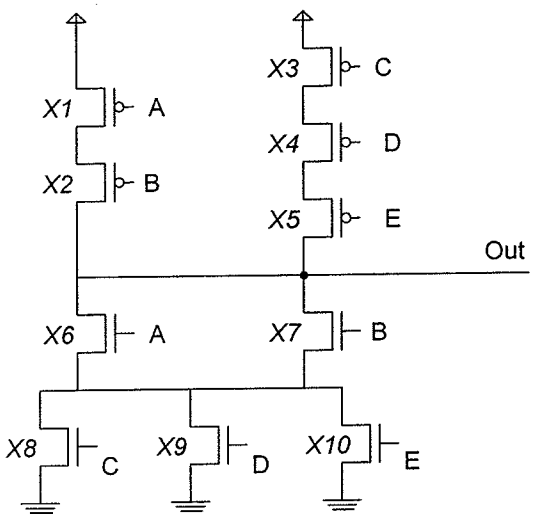
(YES) **NO** (circle exactly one)

c) Does this circuit suffer from static power consumption? (other than that caused by leakage current). [1 mark]

YES (NO) (circle exactly one)

4. TRANSISTOR SIZING:

Consider the following circuit. Assume this is constructed using the process described in the box to the right of the circuit diagram (this is a different technology than the one used in class; if it matters, use this new technology).



λ = 0.075μm (so the minimum transistor length is 0.15 μm)
Min. Transistor Width = 0.2μm
Cgate = 2.8 fF/μm of transistor width
Cndiff = 2 fF/μm of transistor width
Cpdiff = 2 fF/μm of transistor width
*Ron,n = 12 KΩ * L/W*
*Ron,p = 24 KΩ * L/W*
Vdd = 1.5 volts

a) If the parasitic capacitance on the output wire (the load capacitance) is 100fF, and assuming all transistors are all of minimum width and length, give a transition of the inputs that will cause the worst-case transition delay. Give your answer in terms of the input values before the transition and the input values after the transition. Write your answer in the box below [1 marks]

	A	B	C	D	E
Input values before the transition	1	0	1	0	0
Input values after the transition	1	0	0	0	0

(continued on next page...)

other answers are possible. A correct answer would have pull down path on before transition, and the pull up path CDE on after transition (but not the pull up path AB).

b) Now we will change the transistor sizes. Suppose all transistors are to be of minimum length. Further, suppose all NMOS transistors are to have width *Wn* (so they all have the same width) and all PMOS transistors are to have width *Wp* (so they all have the same width). If *Wn=0.6μm*, what value of *Wp* will give equal worst-case rise and fall times? Show your work and write your answer in the box. Express your answer in μm. [2 marks]

worst case pull up path: $(24k\Omega)\left(\frac{L}{W_p}\right)*3$

worst case pull down path: $(12k\Omega)\frac{L}{W_n} * 2$

$\Rightarrow W_p = 3W_n$

$= 1.8\mu m$

Wp = 1.8 μm **μm**

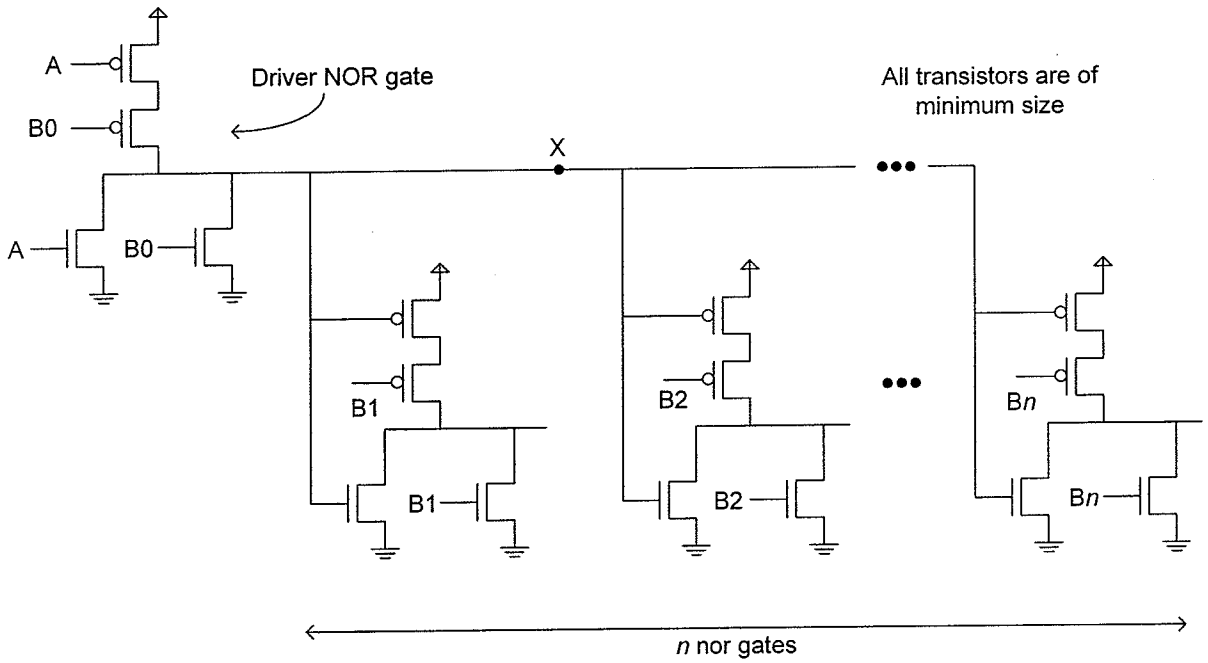
c) Now suppose we remove the restriction that all PMOS transistors must have the same width (but, all NMOS transistors still have *Wn=0.6μm).* Can we reduce the size of any of the PMOS transistors while maintaining an equal worst-case pull-up and pull-down time? [1 mark]

YES **NO** (circle exactly one)

d) If you circled YES, indicate what transistors can be reduced, and what they can be reduced to. If you circled NO, show this mathematically. [2 marks]

reduce A and B to 1.2μm

5. TIMING:
Consider the following circuit. The circuit consists of a NOR gate (labeled "driver NOR gate" and consisting of the left-most four transistors in the diagram) driving *n* identical NOR gates (three of these NOR gates are shown in the diagram).



Suppose this is constructed using the following technology (you might not use all these numbers):

λ = 0.075μm (so the minimum transistor length is 0.15 μm)
Min. Transistor Width = 0.2μm
Cgate = 2.8 fF/μm of transistor width
Cndiff = 2 fF/μm of transistor width
Cpdiff = 2 fF/μm of transistor width
*Ron,n = 12 KΩ * L/W*
*Ron,p = 24 KΩ * L/W*
Vdd = 1.5 volts

Further assume that:
Initial value of A = 0 volts
Initial value of B0 = 0 volts
Initial value of B*i* = 0 volts for *i* between 1 and *n*
Initial value of node X = 1.5 volts
All transistors are of *minimum size* (W= *0.2μm* and L= *0.15 μm)*

Then assume inputs A and B0 switch to 1.5 volts simultaneously. Clearly, node X will fall.

Find the maximum value of *n* such that the delay of the driver NOR gate is less than 36ps. [5 marks]

Remember that the delay of the driver NOR gate is the time between inputs passing 50% of Vdd until node X passes 50% of Vdd.

Write your answer on the next page. You can remove this page from the exam booklet if you like. No writing on this page will be marked.

Write your answer to Question 5 in the box at the bottom of the page. You *must* show your work clearly in order to get full marks.

$R = \frac{1}{2}(12k\Omega)\frac{0.15}{0.2} = 4.5k\Omega$ (1)

$C_{diff} = (0.2 * 2) * 3 = 1.2\ fF$ (1)

$C_{gate} = 2n * 2.8 * 0.2 = 1.12\ n.$ (2)

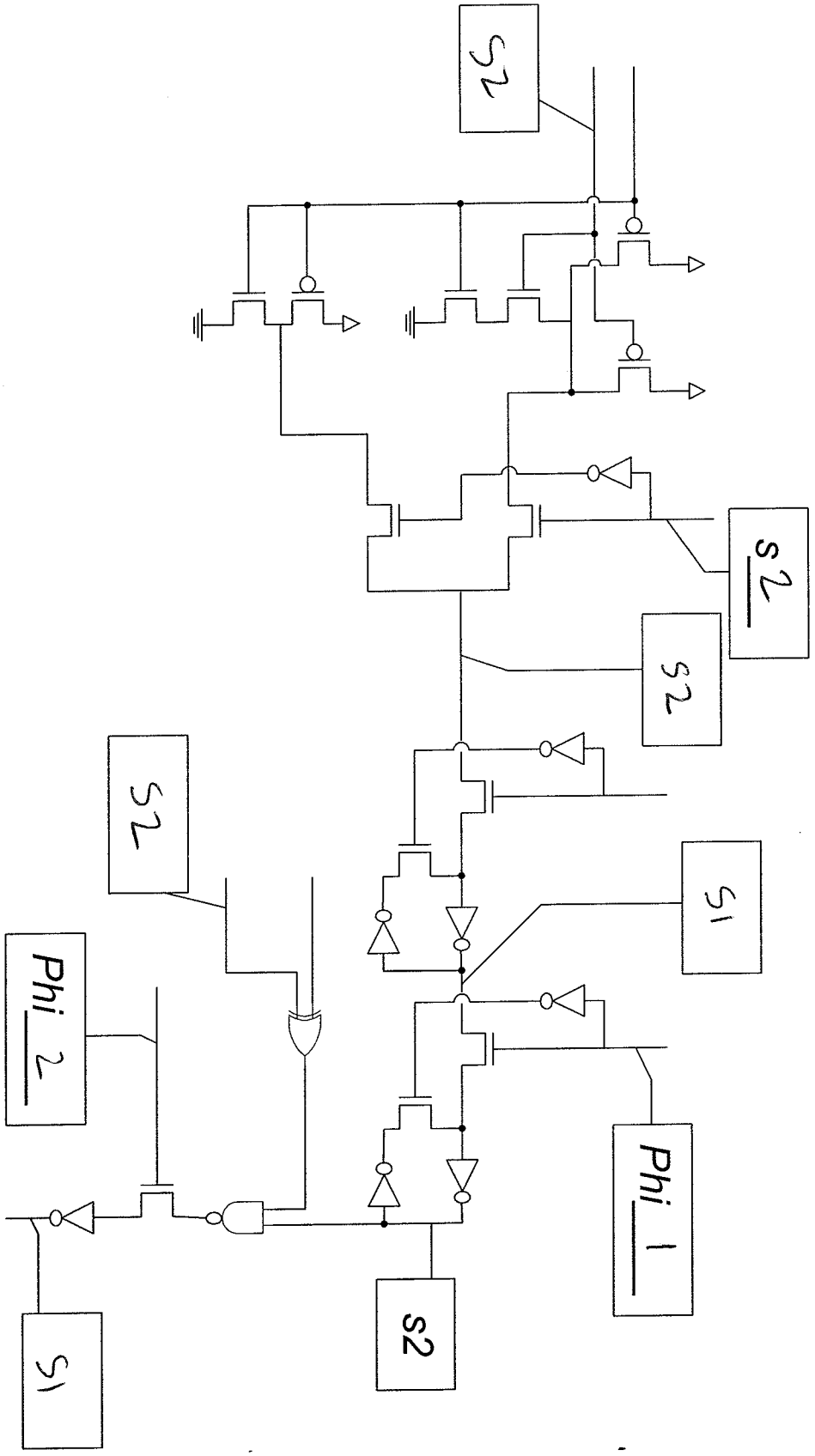
$36ps = (4500)(1.2fF + 1.12n)$ (1)

$n = 6.07$

$\rightarrow 6$

The maximum value of n for which the delay is less than 36 ps is 6

6. Consider the following two-phase clocked circuit. Using the labeling convention discussed in class, fill in each box below with one of: s1, s2, q1, q2, phi1, or phi2 depending on the timing type of the corresponding signal (hint: there are no v1 or v2 signals). One of the signals has been labeled as having type s2 for you; this is the place to start. [4 marks total]



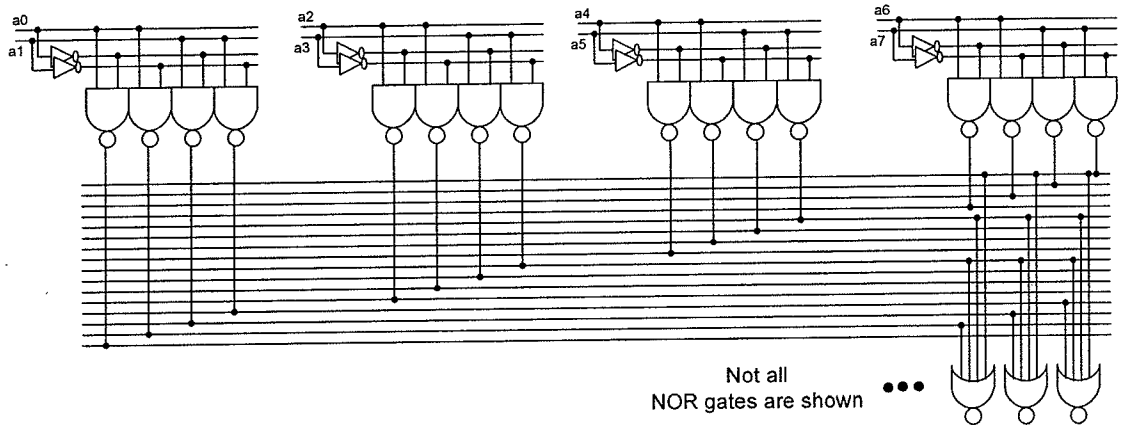
7. MEMORIES:

a) Clearly explain the purpose of a sense amplifier in a standard SRAM memory. [2 marks]

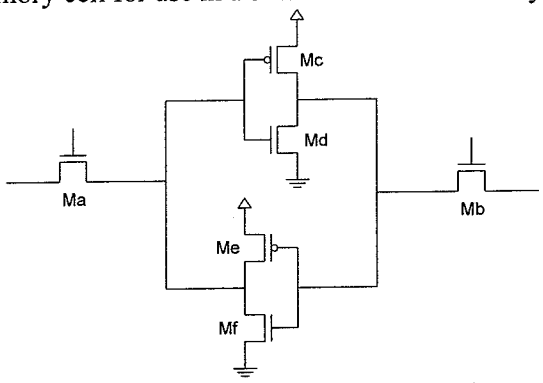
Used to detect differences between bit lines during a read.

b) Consider the following decoder. This decoder is to be used in a memory. Not all NOR gates are shown in the diagram. If I did draw all NOR gates, how many of them would there be? [1 mark]

There would be 256 NOR Gates.



c) Consider the following memory cell for use in a standard SRAM memory.



Assuming all transistors have the same length, which of the following is true?
(Circle exactly one) [1 mark]

(i) For correct operation, transistors Mf and Md should be wider than the rest.
ii) For correct operation, transistors Ma and Mb should be wider than the rest.
iii) For correct operation, transistors Mc and Me should be wider than the rest.
iv) The operation will operate correctly regardless of the transistor sizes. The transistor sizes only affect the speed of the circuit.

The End