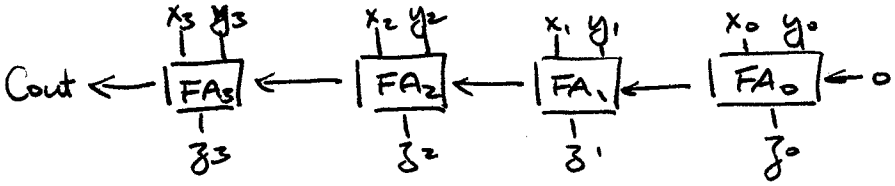
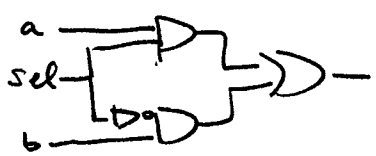
EECE 479 Assignment 1 Solutions - Fall 2007

2 1a) Full Adder, 4bit Ripple Carry



2-1 Mux



Gate Count:

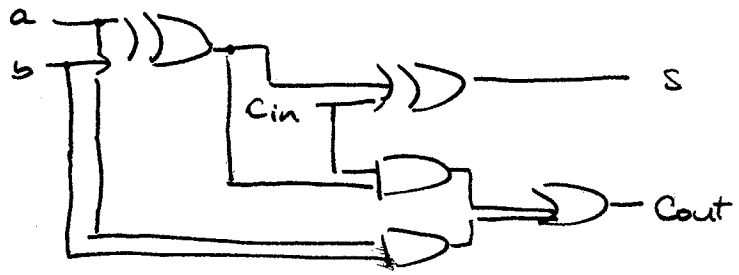
3, 4bit Ripple Carry adders + 4bit mux

= 3 (4 FA x 5 gates/FA) + 4 (4 gates)

= 60 + 16

= 76 gates

Full Adder Unit



2 5) Mux = 3 delay

z_3 = 3 delay (FA_0) + 2 delay (FA_{1-2}) + 2 delay (FA_3)

* Cout is used for the multiplexer's select line
* for FA_{1-3}, by t = 3 delay, A⊕B is ready

= 3 + 4 + 2

= 9 delay

3 + 9 delay = 12 delay total

12 delay x 0.2 = 2.4 ns.

2) Truth Table:

a	b	c	x	z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$X = AC + BC + AB$

$z = A \oplus B \oplus C$

This implements a full adder

3) Truth Table

e	a	out
0	0	z
0	1	z
1	0	1
1	1	0

This implements a tri-state buffer

12 1c) 4 marks for multiplexer correct
4 marks for adder correct
4 marks for overall structure correct
- marks deducted for overly complicated answers