UNIVERSITY OF BRITISH COLUMBIA

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EECE 479: Introduction to VLSI Systems

Fall 2007

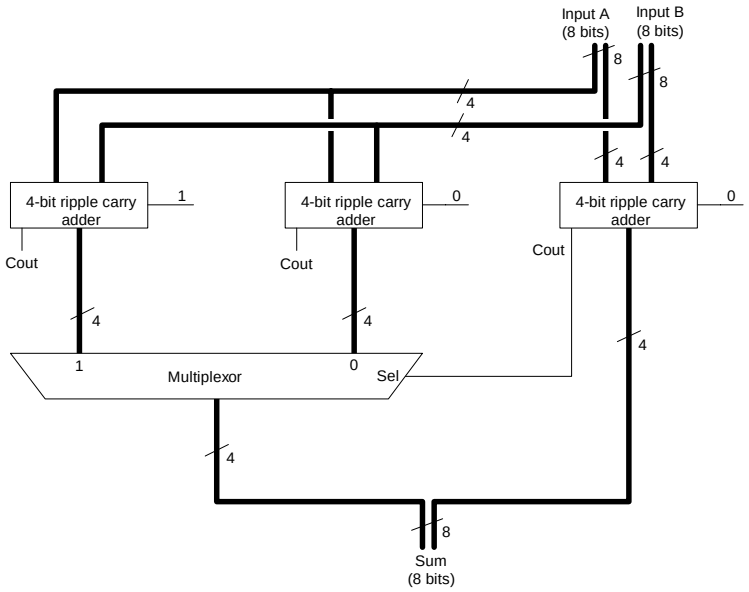
Assignment 1: Warm-up

Due: September 13, 2007 (see late policy on course information sheet)

Do this assignment on your own (not in groups). One handin per person.

In this course, we will be dealing with circuits at a range of abstractions: from behavioural right down to transistor-level. In this warm-up assignment, you will review both ends of this spectrum.

1. Consider the following adder (which you have probably seen before). This is a carry-select adder. This adder adds two eight-bit numbers and consists of three 4-bit adders. The right-most 4-bit adder is used to add the low-order 4 bits of the inputs. The other two 4-bit adders are used to add the upper-order 4 bits. The left-most adder assumes that the carry-in to bit 4 is 1, while the middle adder assumes that the carry-in to bit 4 is 0. The multiplexer chooses one of the two results based on the actual carry-out from the right-most adder.



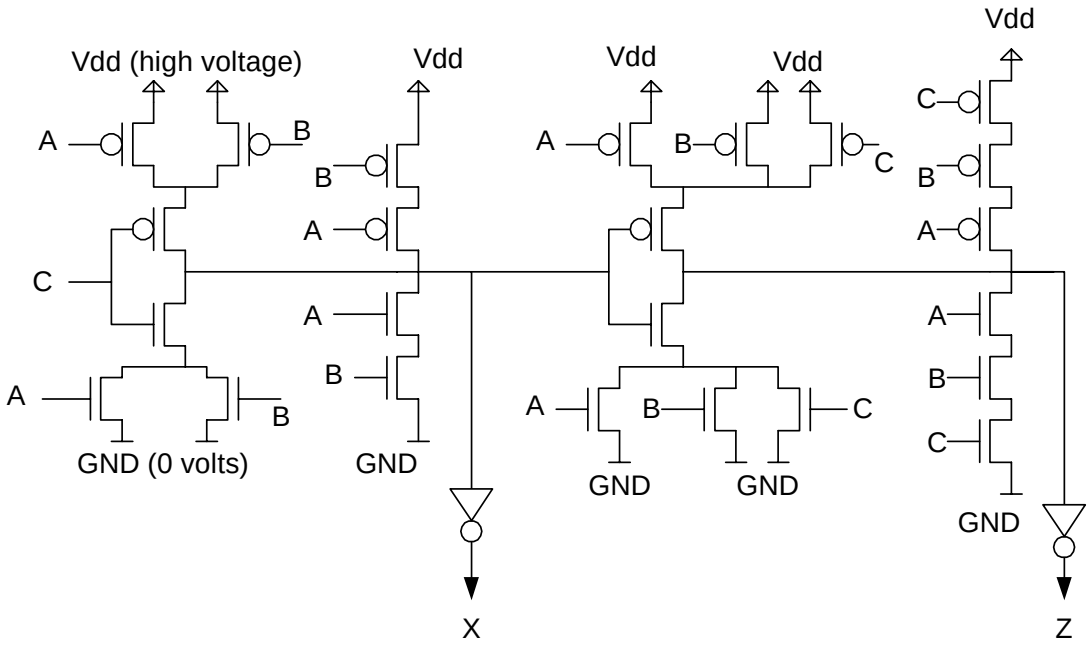
a) *Estimate* the number of gates required to implement this circuit, assuming 2- and 3- input basic gates are available (inverters too). Clearly state any assumptions.

b) *Estimate* the longest path through the circuit, assuming each gate has a delay of 0.2ns. In other words, if all inputs are present at time 0, find the time at which the slowest output line becomes valid. Clearly state any assumptions.

c) Write a VHDL or Verilog specification of this circuit. Each 4-bit adder and the multiplexer must be written as either a separate process or a separate design entity. Simulate the circuit using a simulator of your choice (eg. Quartus, MaxplusII, Synopsys, or anything else you have). Hand in your VHDL or Verilog code.

(Questions 2 and 3 on reverse…)

2. In this course we will be using a simple model for NMOS and PMOS transistor. An NMOS transistor acts as an open-circuit (between source and drain) when it's gate is 0, and a short-circuit (actually a small resistance) between the source and drain when it's gate is 1. A PMOS transistor is exactly the opposite: it operates as an open circuit when it's gate is 1, and a short-circuit when it's gate is 0. Given this simple model, write the function of the following circuit. The circuit has three inputs: A, B, and C, and two outputs X and Z. What is the function of this circuit? Hint: start with a truth-table. For each entry in the truth-table, write which transistors are closed and which are open, and hence, what the output values are. When you are done, you will have a complete truth table, and you can easily write the function and figure out what the circuit does. To get you started, it appears to me as if the output X is 0 when all inputs A,B, and C are 0.



3. Explain the operation of the following circuit in all modes of operation. What can this circuit be used for?