Slide Set 1

Overview of VLSI: Complexity, Wires and Switches

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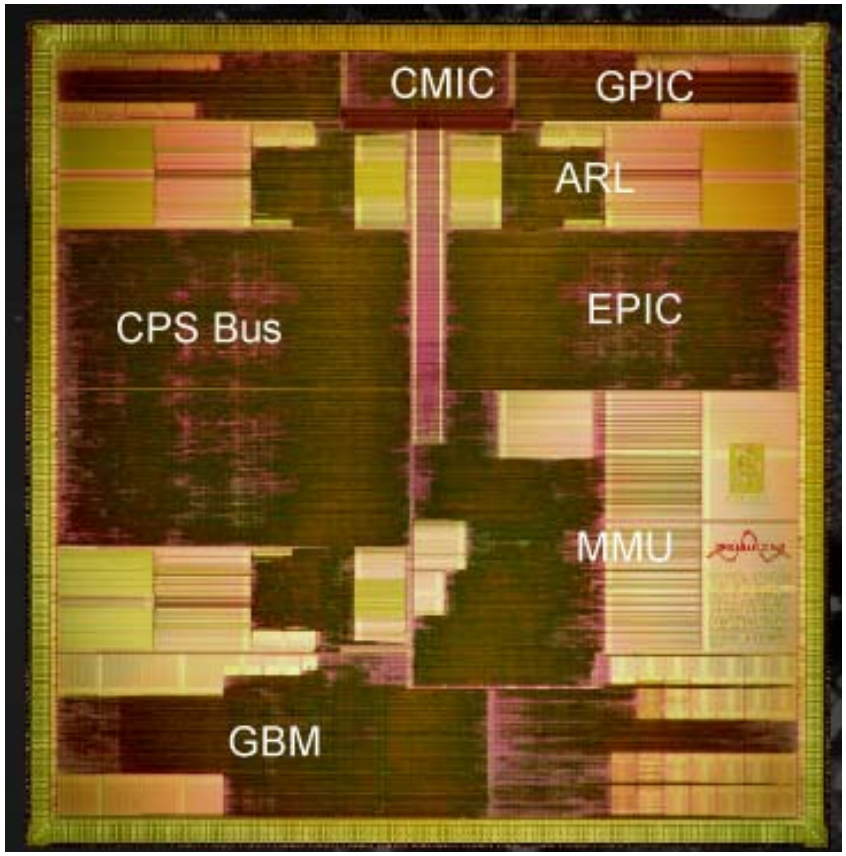
Note: Some of these slides are from Shahriar Mirabbasi and Res Saleh and others

What is VLSI?



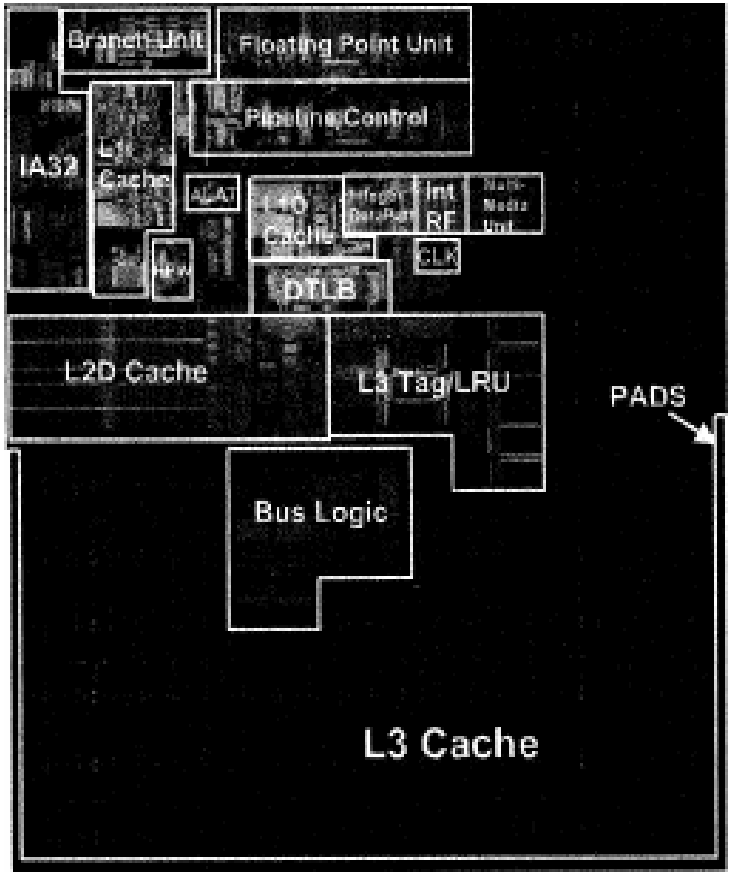
24 100 Meg + 2 Gig Port Ethernet Switch

- **60 Million Transistors**
- **Over 4 Million Gates**
- **8Mb of Embedded RAM**

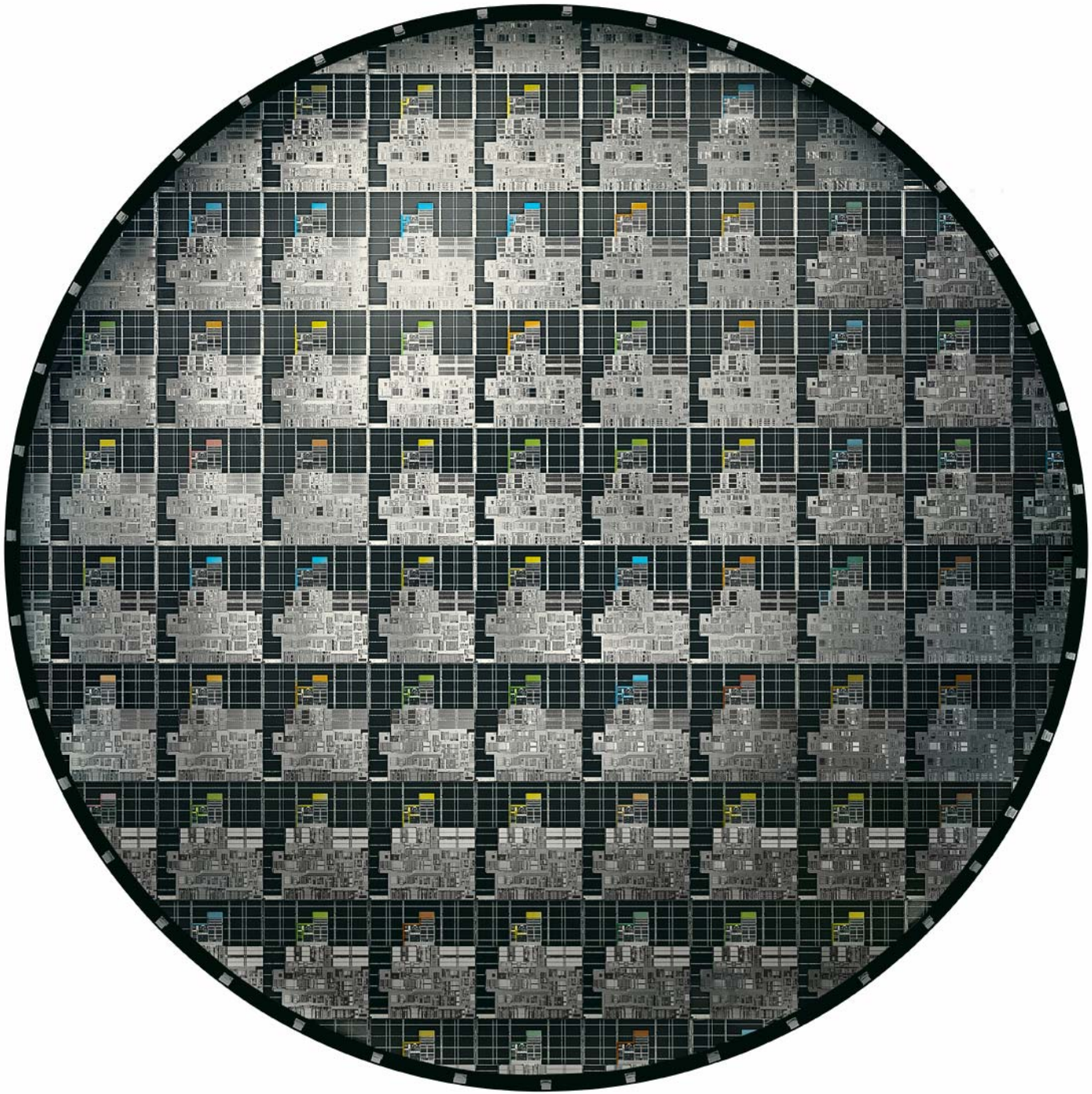
Source: Henry Samulei, Broadcom, D.A.C. 2001

Intel Itanium Processor

0.13 μm Technology, 410,000,000 transistors in a 374mm^2 area

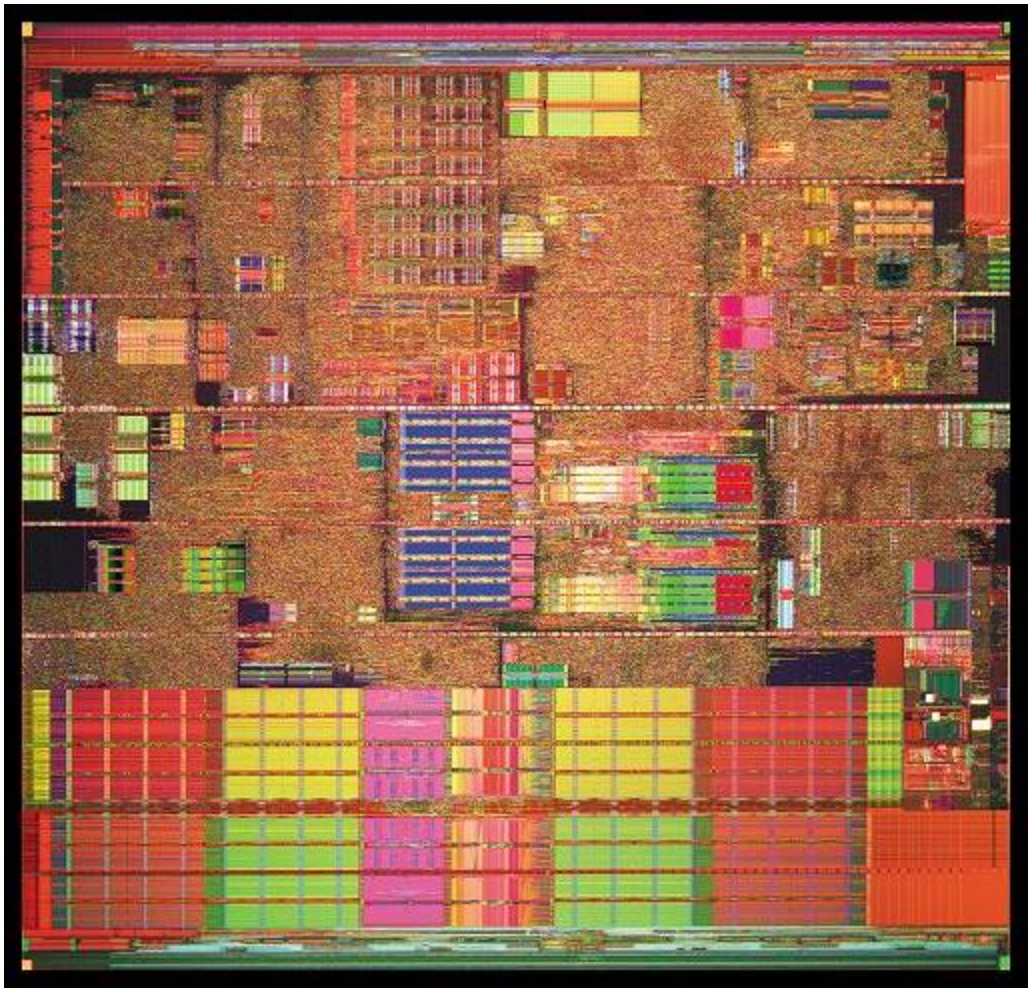


Source: ISSCC 2003



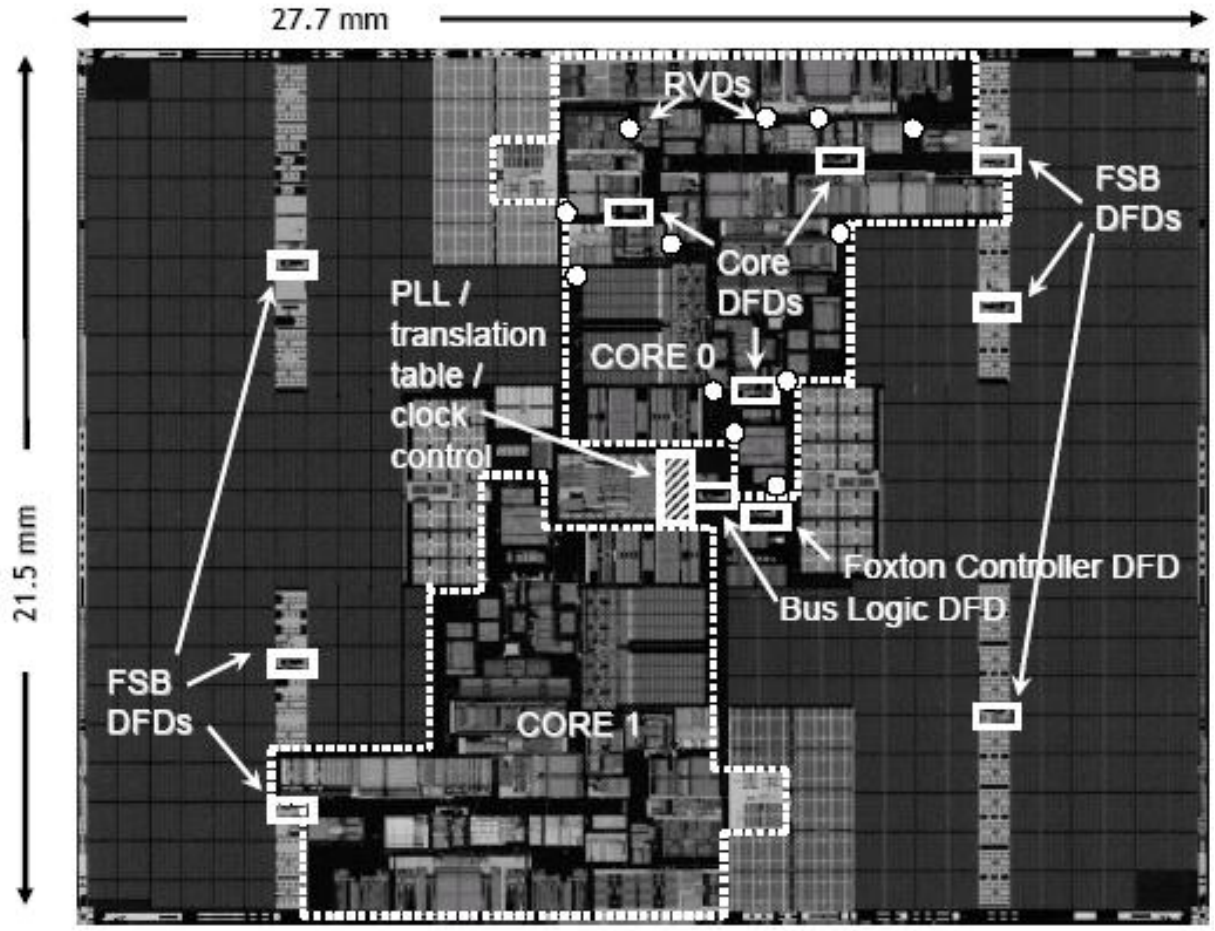
Prescott Pentium 4

- 122 mm^2 125 million transistors



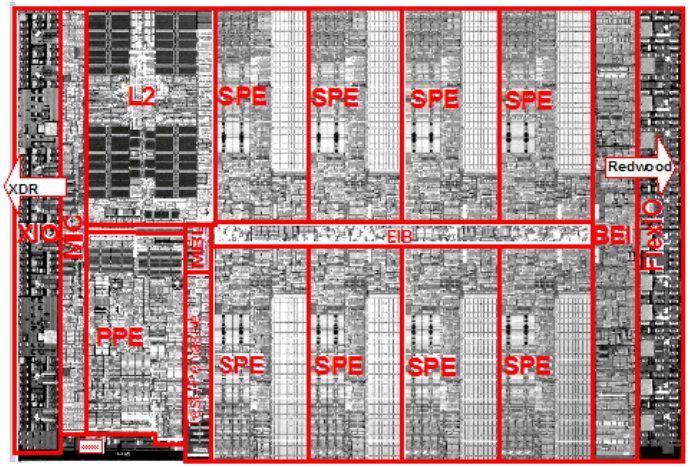
Dual-Core Intel Itanium 2 processor (Montecito)

1.72 billion transistors, 27.72 mm x 21.5 mm

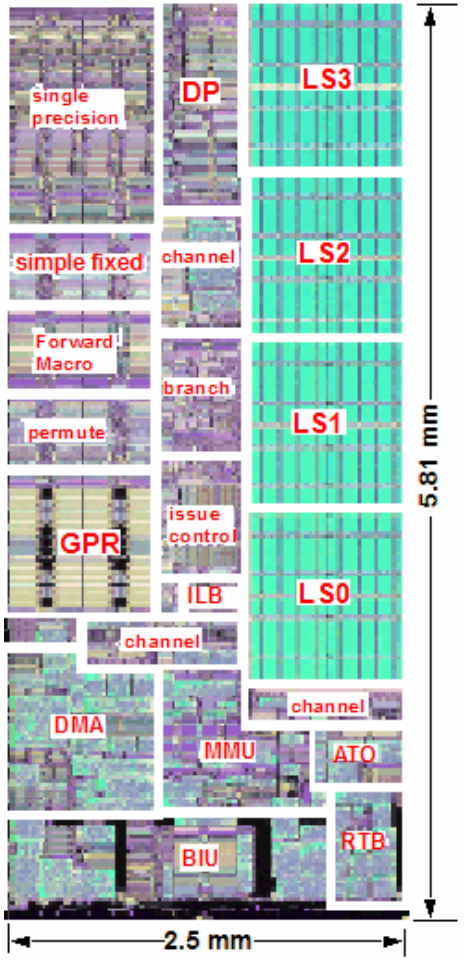


Cell Processor

- PowerPC Processing Element (PPE), Synergistic Processing Element (SPE), Internal Element Interconnect Bus(EIB), Shared Memory Interface Controller (MIC), Double precision FPU (DP)m
- 90nm, 4GHz, 256 GFLOPS (single), 25 GLOPS (double), 25 GB/s memory bandwidth (RAMBUS), 50-80W
- Trend is to augment processor with parallel functional units to improve efficiency



IBM/Sony/Toshiba Cell Processor

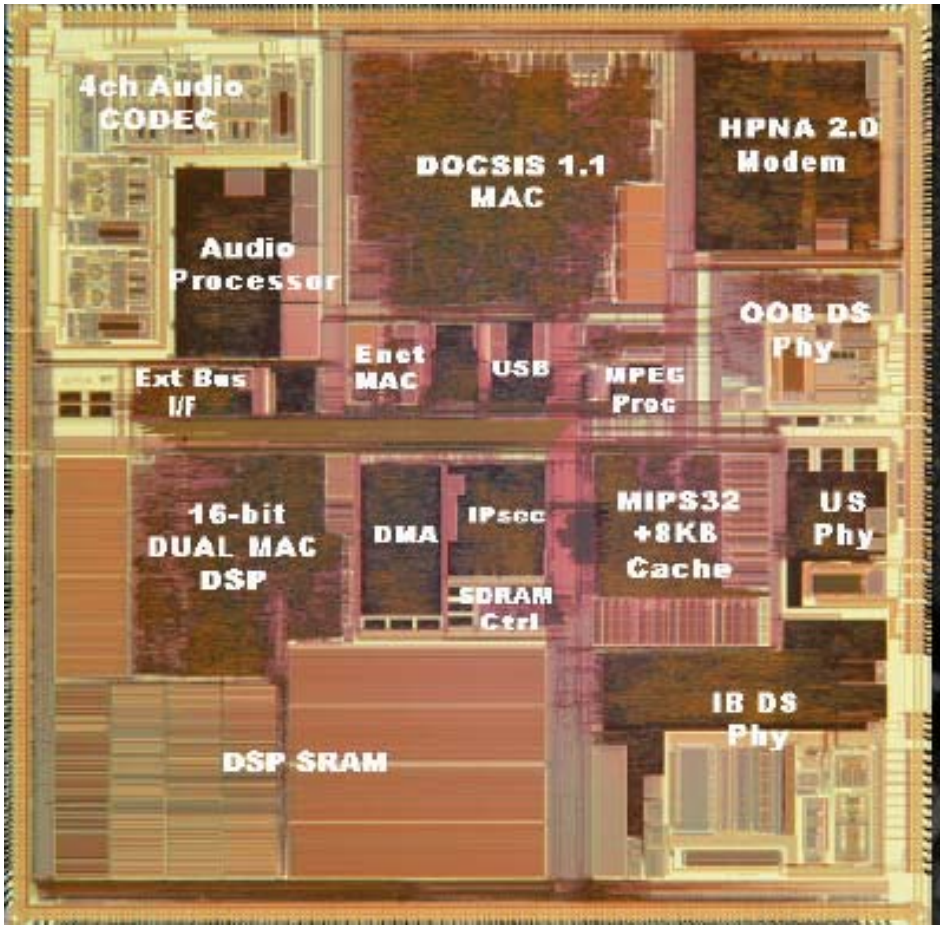


Synergistic Processing Element: 4 FMADD/cycle

Source: http://www.realworldtech.com/includes/templates/articles.cfm?ArticleID=RWT021005084318&mode=print

VLSI Beyond Digital

Cable Modem Residential Gateway



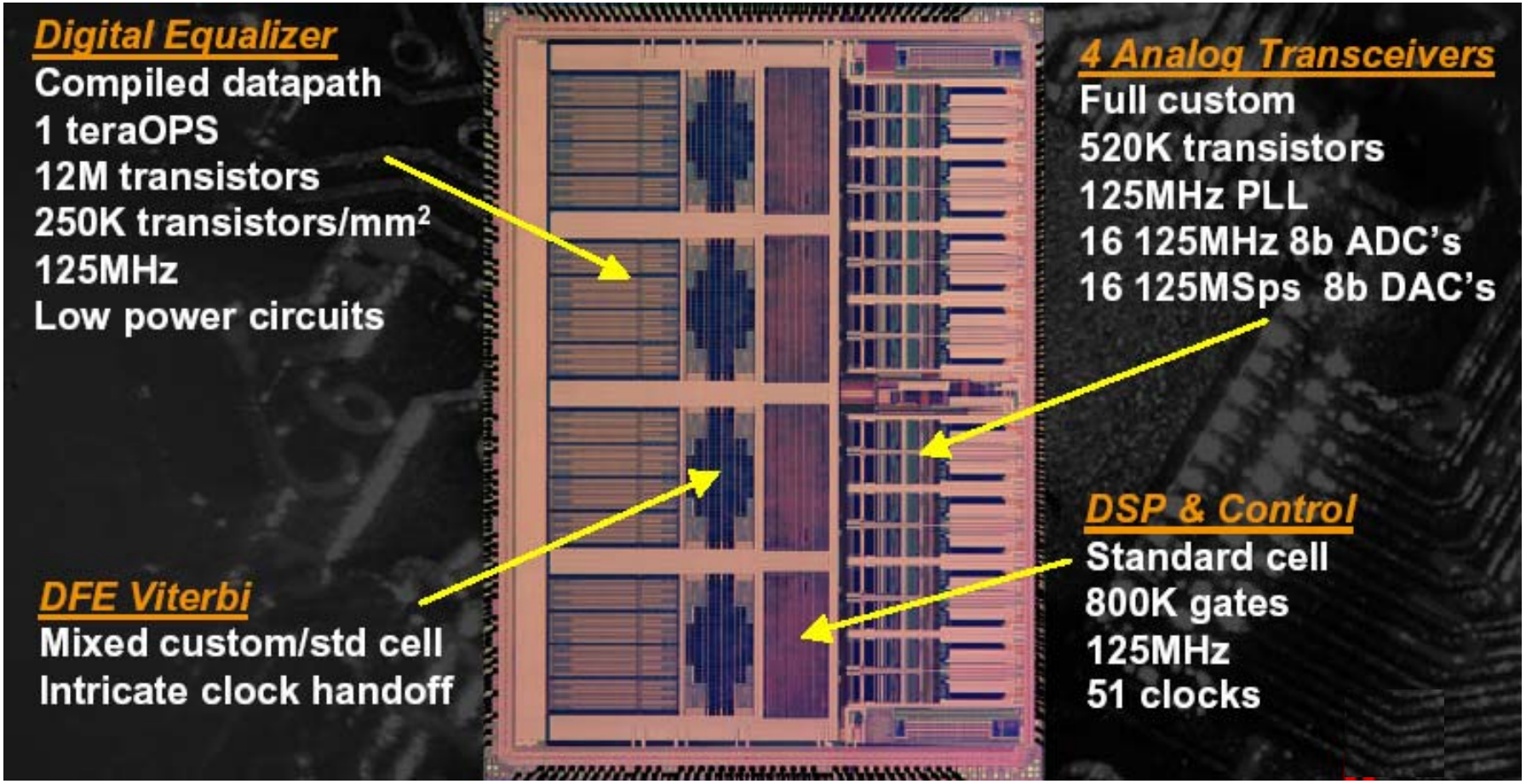
Single Chip Gateway

Over 25 million transistors
Over 4 million gates
~3Mb of embedded SRAM
150+ internal RAM instances
MIPS core @ 100MHz
DSP core @ 144MHz
AFE's @ up to 200MHz
7 PLL's, 12 ADC's and DAC's
100+ internally generated clocks
1.4 Watts with all sections active
454 ball PBGA package

Source: Henry Samulei, Broadcom, DAC 2001

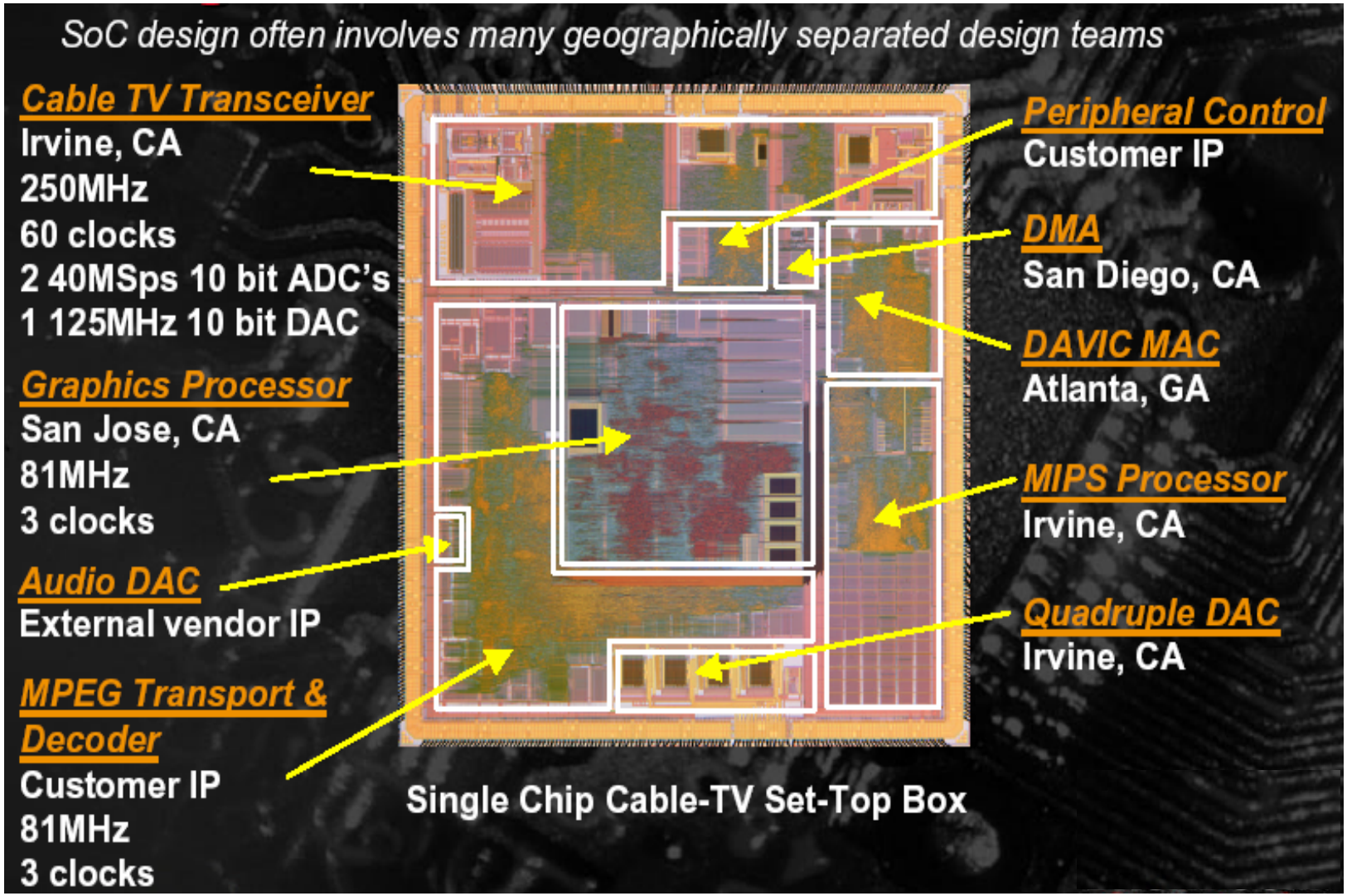
VLSI Beyond Digital

0.13 μm Quad 10/100/1000Base-T Transceiver:



Source: Henry Samulei, Broadcom, DAC 2001

System-on-a-Chip (SoC)



Source: Henry Samulei, Broadcom, DAC 2001

Cell Processor Design Teams

From: Takahashi et al, Custom Integrated Circuits Conference, Sept 2007

What is on an Integrated Circuit?

Conducting layers which form the wires on the IC.

- There are many layers of wires (used to have 1 layer of metal, now advanced processes have 7-8 metal layers). Wires have electrical properties like resistance and capacitance.

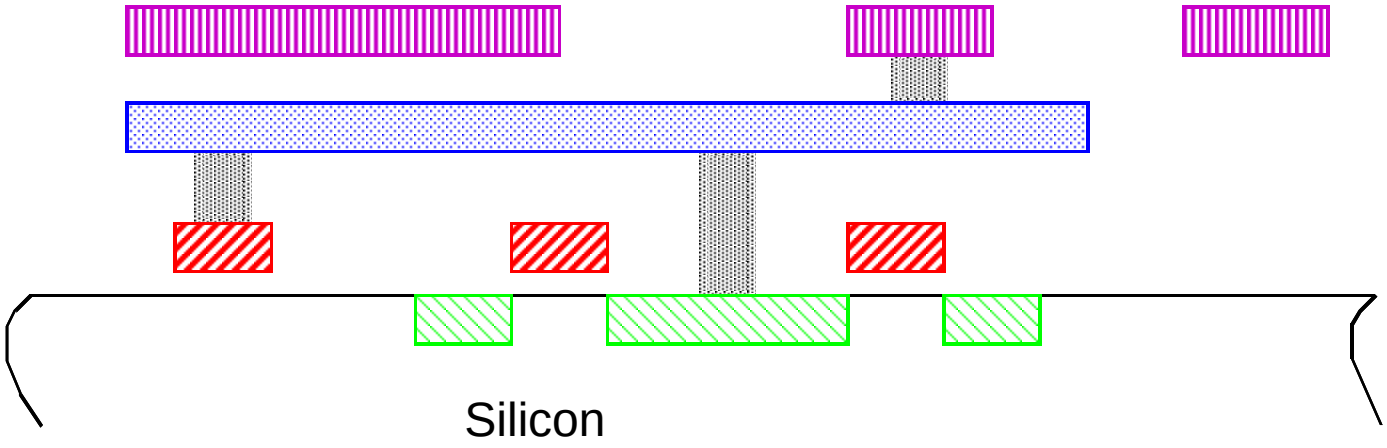
  (Requires insulators and contacts between layers.)

Transistors (the free things that fit under the wires).

- There are a few kinds of transistors. In this class we will study MOS ICs, so we will work with MOS transistors. These transistors can be thought of as a voltage controlled switch. The voltage on one terminal of the transistor determines whether the other two terminals are connected or not.

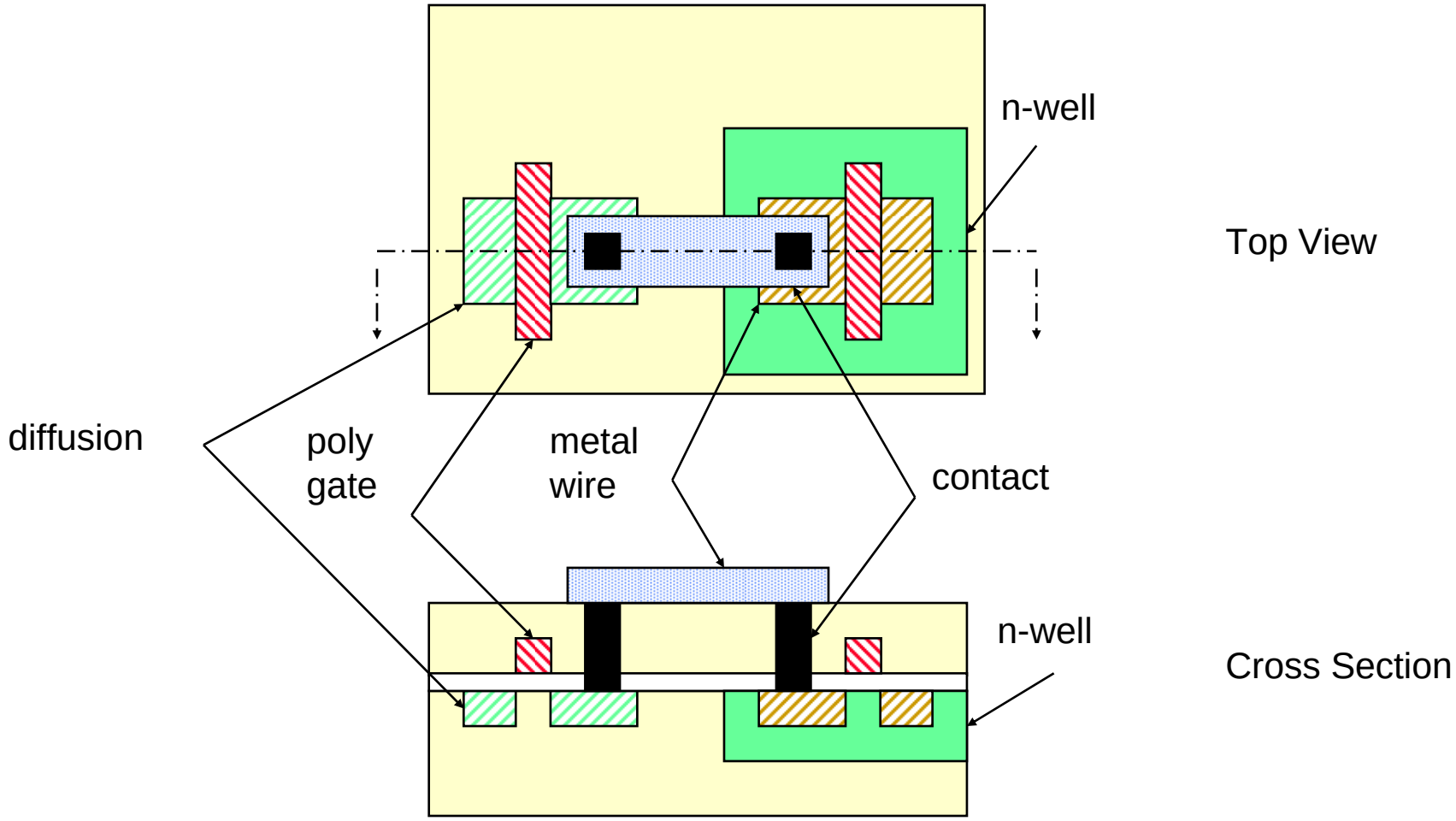
Physical Topology of an Integrated Circuit

- The transistors are built in the silicon, and then there are lots of wiring layers deposited on top. In cross-section it looks like (abstractly):

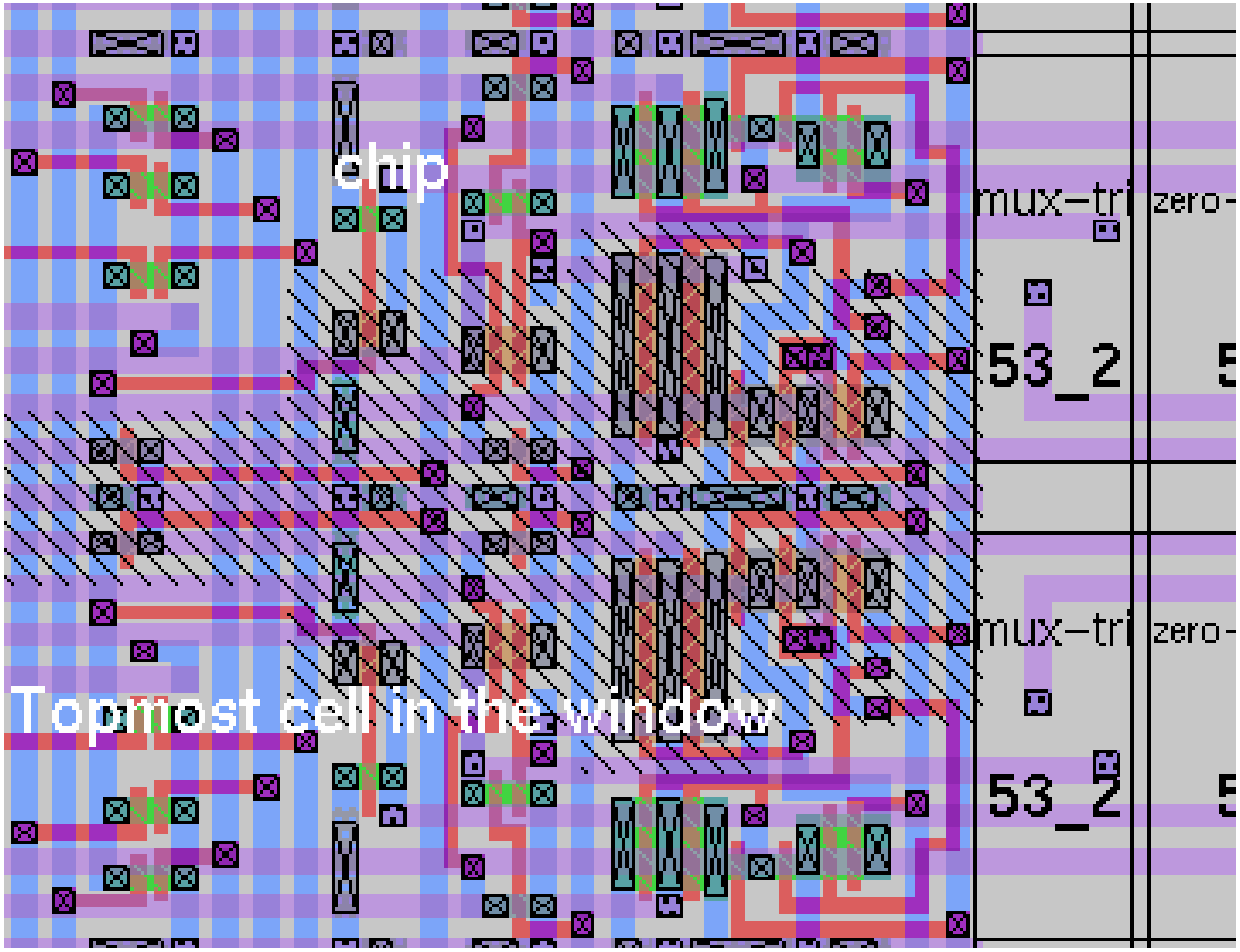


In the technology that we will use in the class (which can be scaled from 2μ to 0.06μ) there are 4 primary layers. The top two layers are metal wires, and then there is a polysilicon layer and a diffusion layer (together poly and diff can form “active” devices – more on that later).

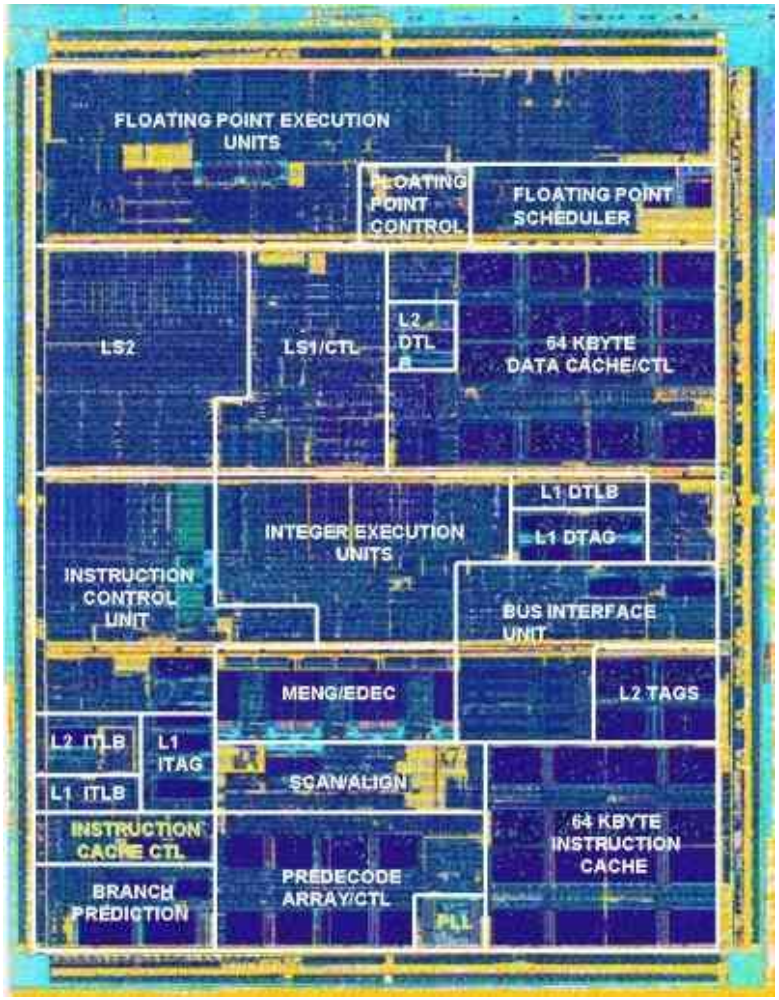
Top View and Cross Section:



Example Datapath Layout:



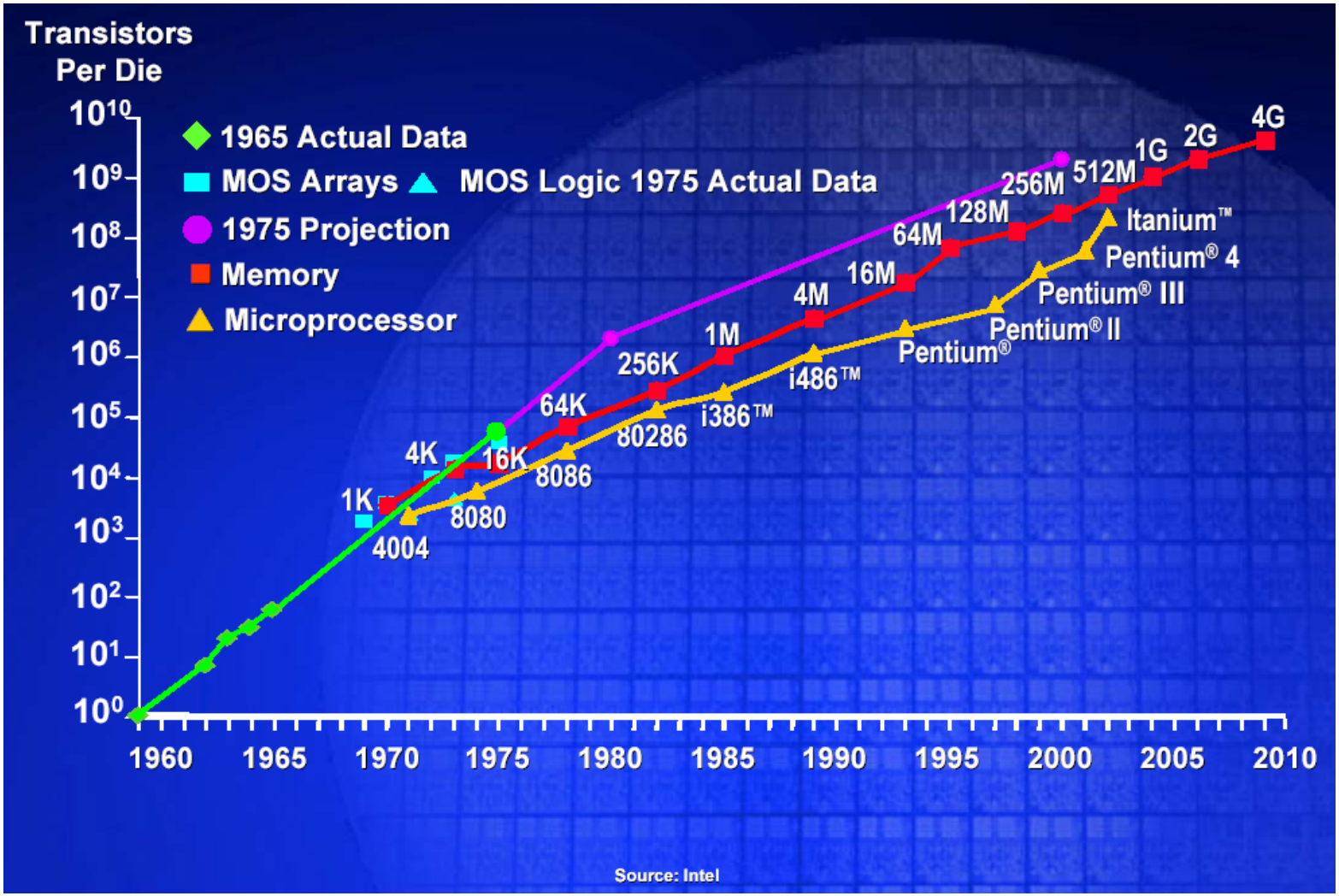
AMD K7


FLOATING POINT EXECUTION UNITS
FLOATING POINT CONTROL
FLOATING POINT SCHEDULER
LS2
LS1/CTL
L2 DTL B
64 KBYTE DATA CACHE/CTL
L1 DTLB
L1 DTAG
INTEGER EXECUTION UNITS
INSTRUCTION CONTROL UNIT
BUS INTERFACE UNIT
MENG/EDEC
L2 TAGS
L2 ITLB
L1 ITAG
L1 ITLB
SCAN/ALIGN
INSTRUCTION CACHE CTL
64 KBYTE INSTRUCTION CACHE
BRANCH PREDICTION
PREDECODE ARRAY/CTL
PLL

Gordon Moore estimated in 2003 that the number of transistors shipped in a year had reached about 10,000,000,000,000,000,000 (10^{18}). That's about 100 times the number of ants estimated to be in the world.

Source: Intel

Integrated Circuit Complexity



Gordon Moore's Presentation at ISSCC 2003

Moore's Law

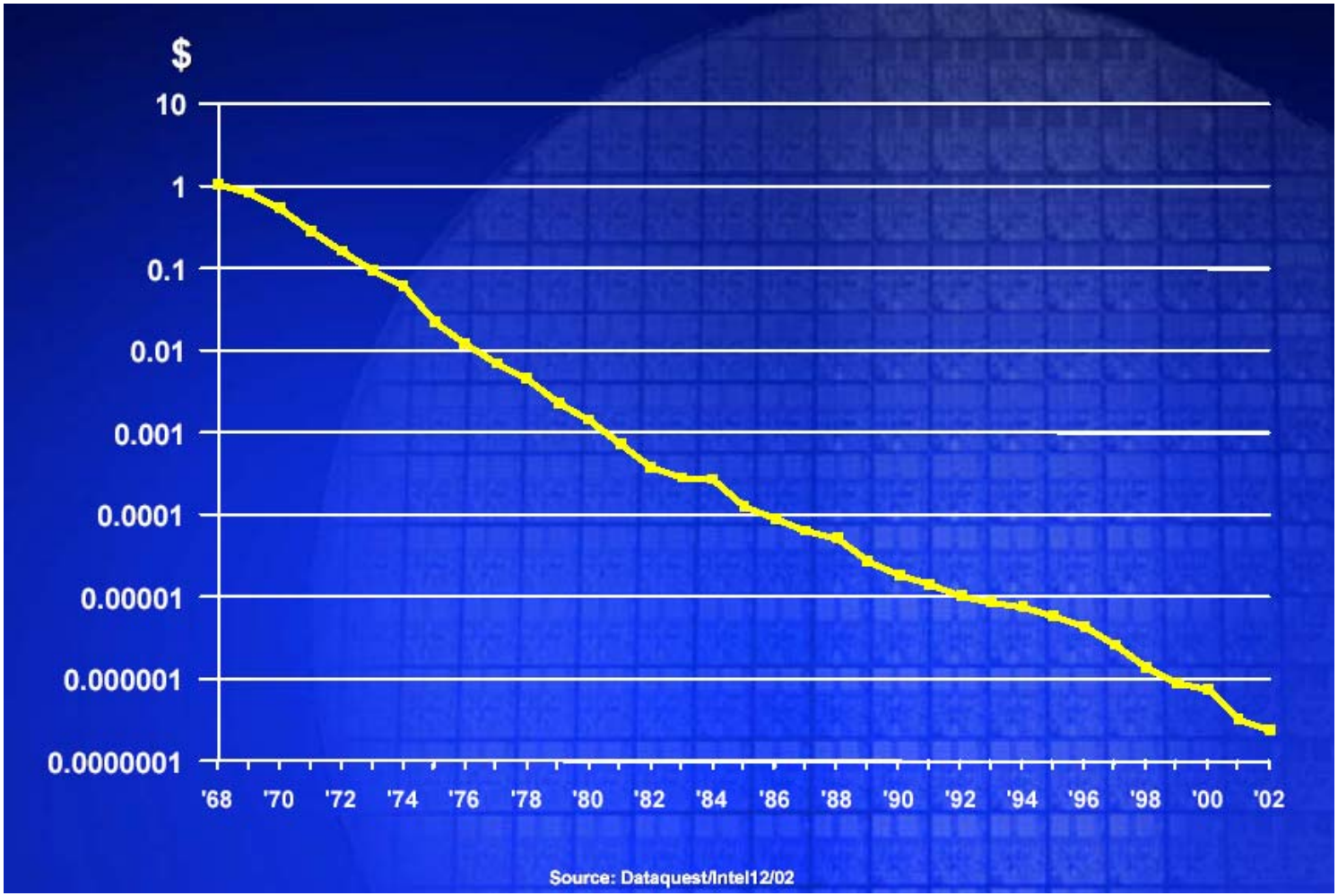
"The number of transistors incorporated in a chip will approximately double every 24 months."

- Gordon Moore, Intel Co-founder

In 1978, a commercial flight between New York and Paris cost around $900 and took seven hours. If the principles of Moore's Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.

Source: Intel

Average Cost of a Transistor



Gordon Moore's Presentation at ISSCC 2003

What applications might need all these transistors?

General purpose processors may not provide enough speed for:

- Rigid Body Game Physics
- Fluid Simulation
- Portfolio management
- Text Mining
- Signal / Image processing systems
- Derivative Pricing
- Stochastic optimization
- Dense and sparse matrix primitives

For these types of applications, we need something better…

Sense of Scale: What about speed?

Typical Gate Delay is about 0.1 ns

This is, roughly, the time it takes light to travel 1 inch.

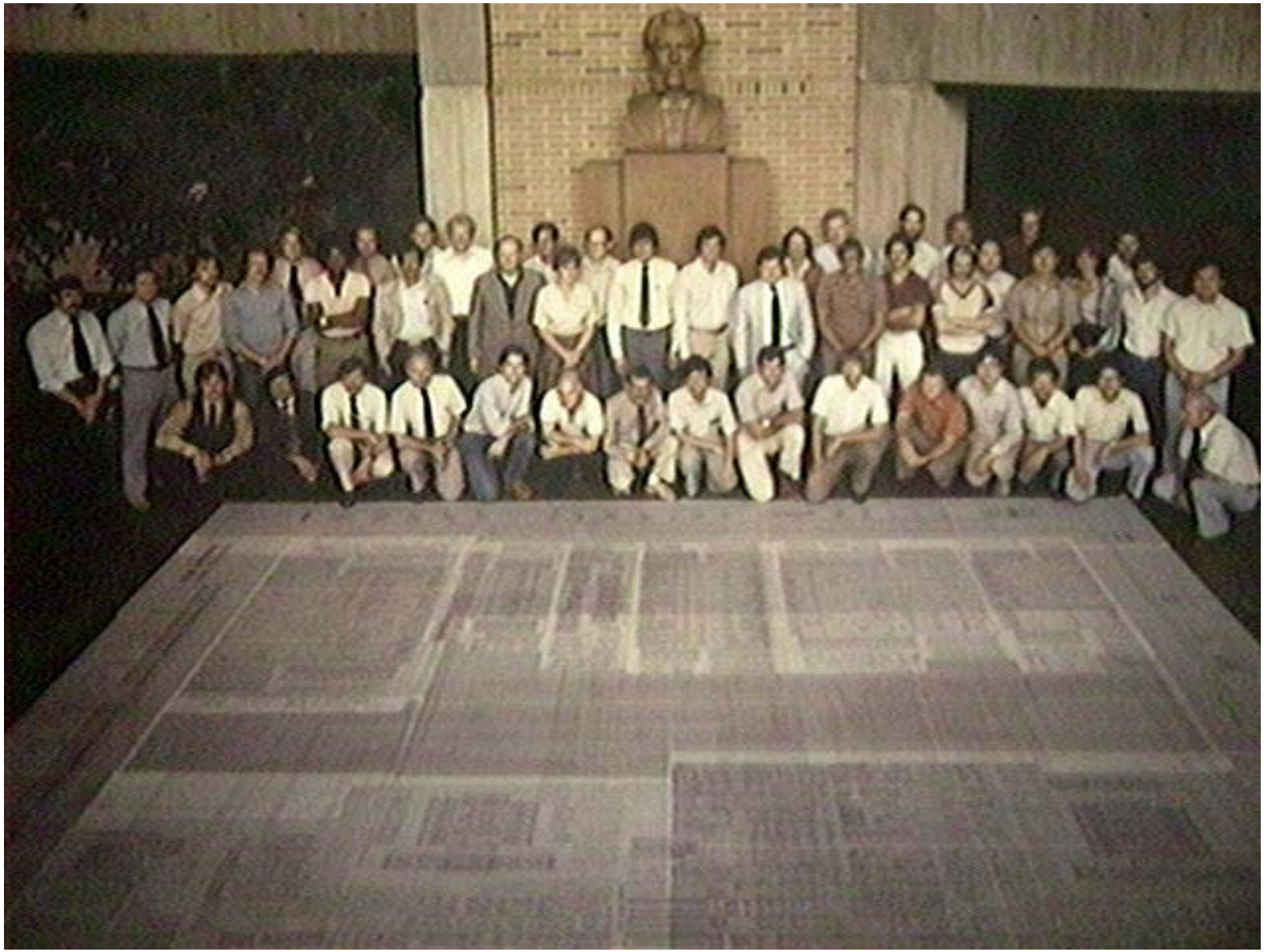
How many gate delays per clock cycle in a 3Ghz processor?

In this course we will answer one question:

Modern Integrated Circuits are the most complex thing ever designed by mankind

- 30,000,000 parts and all of them have to work!

How can we hope to design anything this complex?!??!



CAD Tools

Today, we use CAD tools for every stage of the design process

- Design modeling
- Design entry
- Simulation
- Pre-fabrication processing

Do these tools negate the need for a smart engineer?

NO! They are only tools.

But a lot of the tedious work has been eliminated

Design Levels

- Specification
  - what the system (or component) is supposed to do
- Architecture
  - high-level design of component
    - state defined
    - logic partitioned into major blocks
- Logic
  - gates, flip-flops, and the connections between them
- Circuit
  - transistor circuits to realize logic elements
- Device
  - behavior of individual circuit elements
- Layout
  - geometry used to define and connect circuit elements
- Process
  - steps used to define circuit elements

Can describe design at many different levels of abstraction

High-lighted levels we will discuss in this class

VLSI Design in this Class

- **VLSI Design exploits hierarchical design techniques and automatic design tools to achieve rapid turnaround times**
- **It allows designers to work at an abstract system level rather than at the level of silicon to build complex chips**
- **Our goal is to understand enough about the silicon level, physical design level, gate level, and RTL level to design a working chip**
- **We will explore issues of finite-state machine design, clocking schemes, and circuit implementation techniques**
- **The project will try to tie all the concepts together into one design which you will carry out for the 2nd half of the course**
- **This course will require a substantial amount of work, especially in the project phase (although you will work in groups)**
- **However, it is an extremely valuable course and is relevant to what is going on in industry today**

The TA

We have one TA that will be able to help you with both the classroom material and the assignments. You can contact her by email to set up an appointment.

Cindy Mark
http://www.ece.ubc.ca/~cindym
cindym@ece.ubc.ca

She will hold office hours if there is demand.

For More Introduction:

Read Chapter 1 of the course textbook (Wolf)