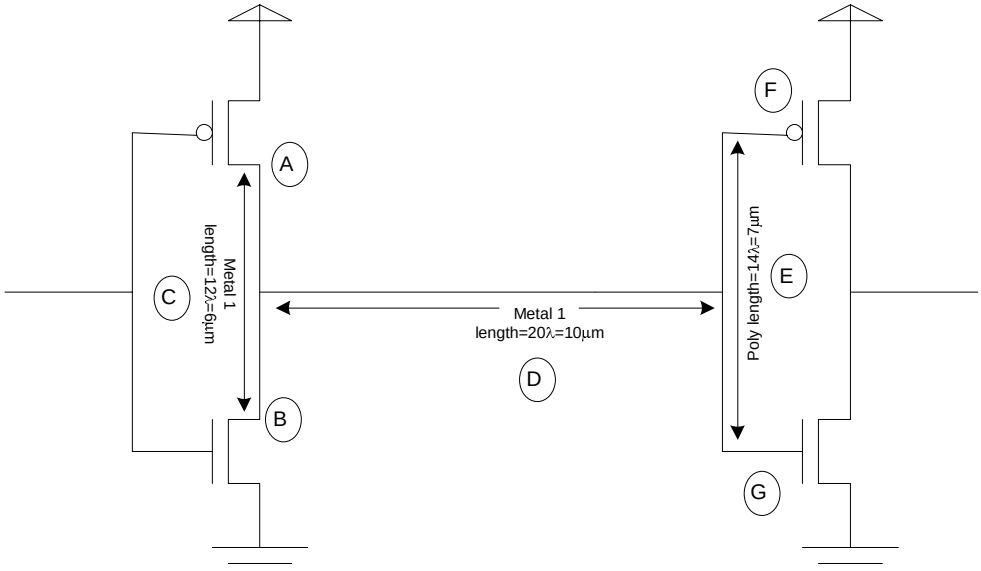
This diagram accompanies the example on page 16 of slide set 5. The problem is to find the parasitic capacitance attached to the node between the two inverters. We will work this out carefully in class.

All transistors are of width 4λ = 2μm



Total capacitance attached to this node is the sum of diffusion regions A and B, metal wires C and D, poly wire E, and gate regions G and F.