Slide Set 6

Cell Design Issues

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Based on Slides by Res Saleh, 2000
which were based on Slides by Mark Horowitz, Sanford U.

Overview

Iis time to talk a bit more about Cell design. Much of this you have seen before (eg. in Assignment 2), but there are some additional things that might help you with your project. There are two issues in cell layout: what are the internal constraints (how will the cell be built) and what are the interface constraints (how will the cell be used). Datapath cells and memory array cells have more interface constraints to allow them to connect by abutment. Standard cells have fewer constraints and are easier to design.

This lecture first looks at the timing model and then describes a number of ways to keep the delay small by using layout techniques. We then examine the details of standard cell layout, and then datapath layout.

Review: Simple Timing Model

RC Model:

- Model the transistor as a linear resistor
  - Resistance is equal to Rsq * L/W
  - nMOS - 13Kohms/sq
  - pMOS - 26kohms/sq
- Model the load as a capacitor
- Delay is RC

Hardest part of using this simple model is finding the load capacitance C. It comes from 3 sources:

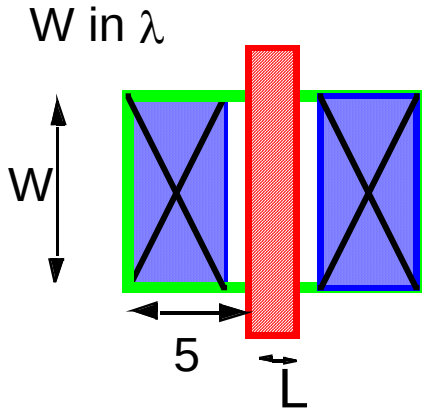
- Gate capacitance of driven transistors.
- Diffusion cap. of source/drain regions connected to the wire.
- Wire capacitance

Review: Rule of Thumb Capacitance Table

For our 1um technology:

For a transistor with min. L and diffusion region 5 or 6 um wide:

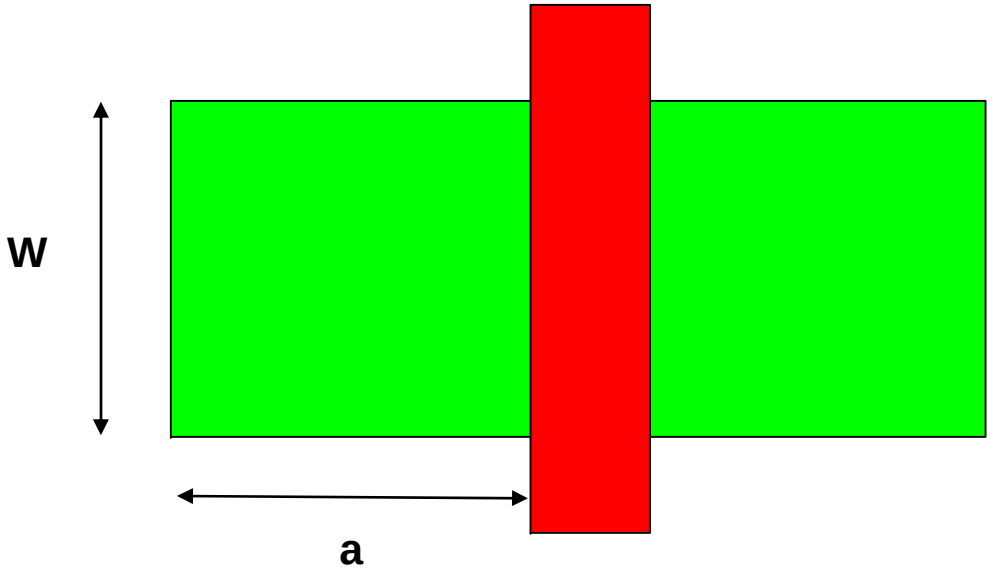
Transistor Cap	Capacitance per μ of transistor width
Gate (Poly over diff)	2.0 fF/μ
ndiff (5λ or 6λ wide)	2.0 fF/μ
pdiff (5λ or 6λ wide)	2.0 fF/μ



For a "typical" width wire (3 or 4λ):

Wire Cap	Capacitance per unit length	Length when C = Cinv
poly wiring	0.2 fF/μ	40μ
metal1 (3λ or 4λ wide)	0.3 fF/μ	30μ
metal2 (3λ or 4λ wide)	0.2 fF/μ	40μ

Diffusion Capacitance: More Detail

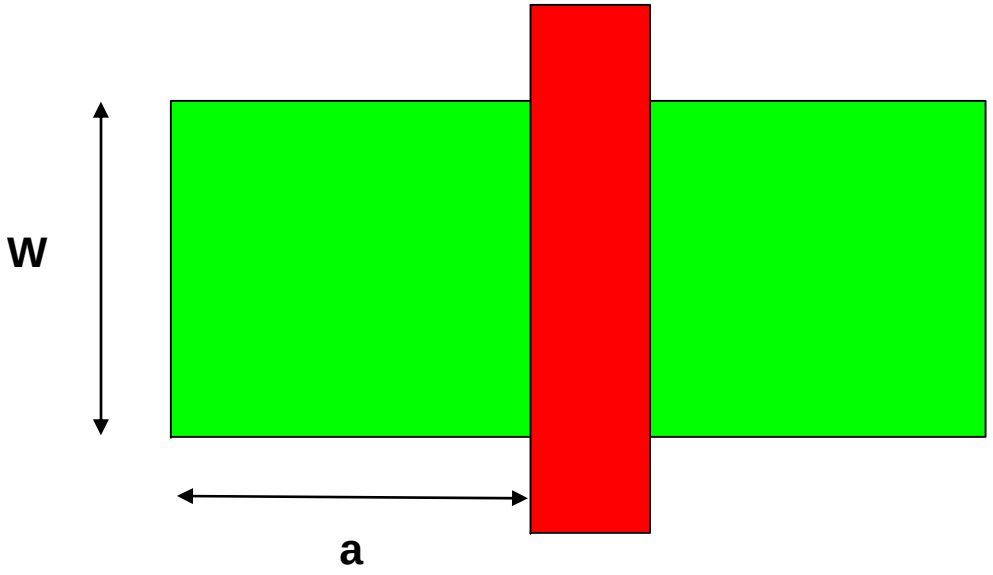


Diffusion Capacitance has two components:

a) a component proportional to area (W*a)

b) a component proportional to perimeter (W+a+W+a)

Diffusion Capacitance: More Detail



For our 1μm technology: (note these numbers are in terms of μ's, not λ's):

	Area Component	Perimeter Component
ndiff	0.2 fF/μ^2	0.5 fF/μ
pdiff	0.5 fF/μ^2	0.2 fF/μ

More Detailed Model for Diff. Cap.

In our simple model, we assumed that **a** was 5λ

NMOS Diffusion Capacitance:

$(5 / 2) * (W / 2) * 0.2\ fF/\mu^2 + (W/2 + W/2 + 5/2 + 5/2) * 0.5fF/\mu$

$= (0.75W + 2.5fF)$

Divide dimensions by 2, because they are in λ's, but the table on the previous slide is in μ's.

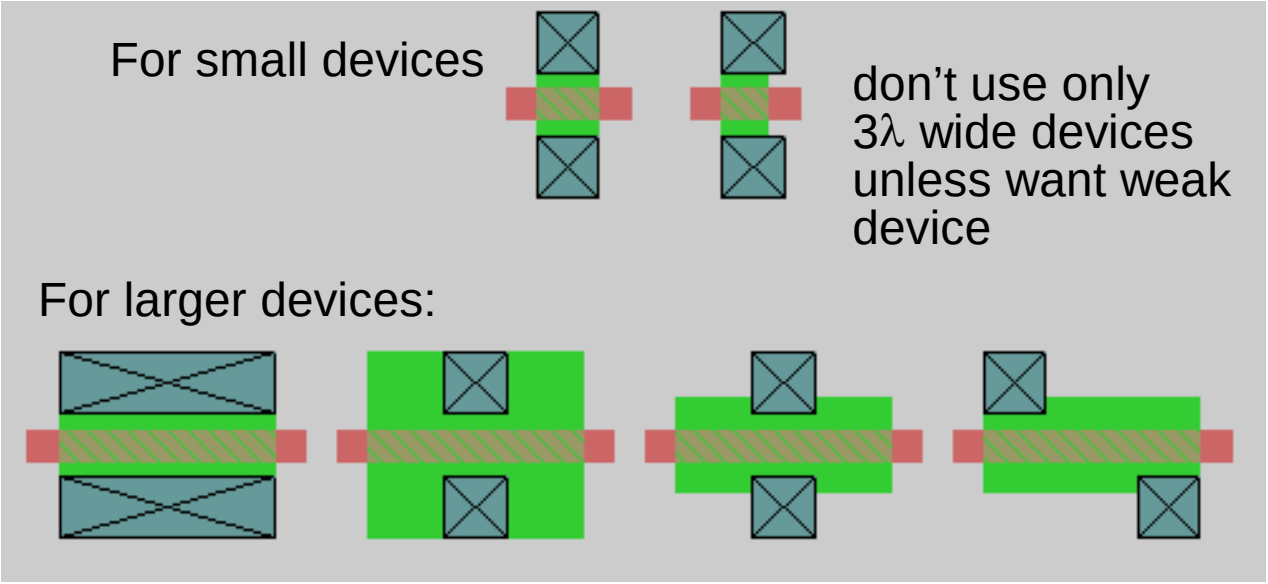
PMOS Diffusion Capacitance:

$(5 / 2) * (W / 2) * 0.5\ fF/\mu^2 + (W/2 + W/2 + 5/2 + 5/2) * 0.52F/\mu$

$= (0.825W + 1fF)$

Transistor Layout

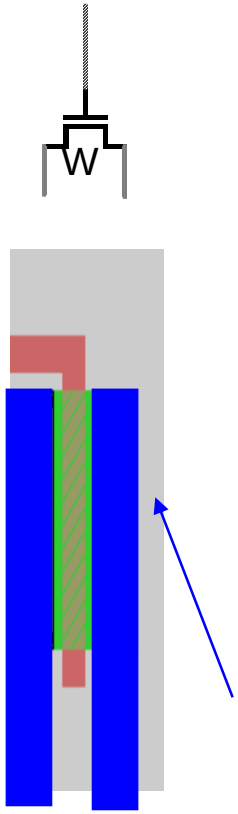
What does this mean for transistor layout?



Transistors should be at least as wide as contacts (4λ). Use as many contacts as possible for wider transistors. No diffusion anywhere else.

Using Folding to Reduce Drain Capacitance

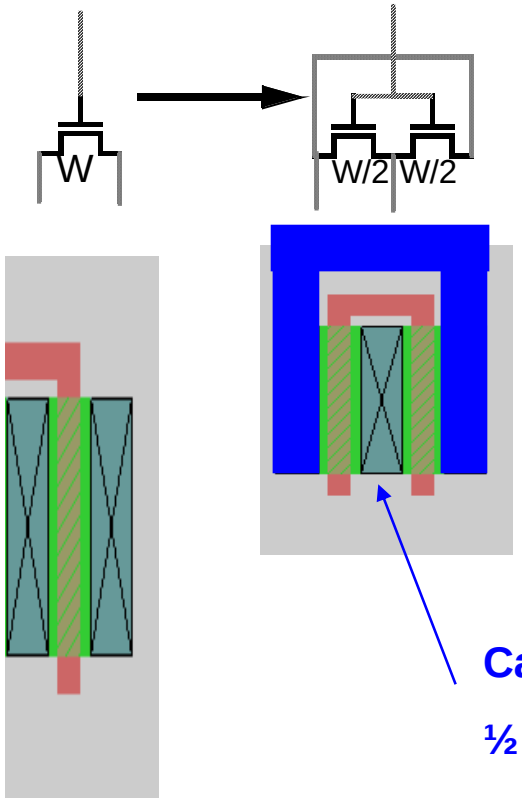
For very large transistors you end up with a bad aspect ratio. To make it a more square shape, fold the transistor. This **folding** also halves the size of the high capacitance diffusion regions of the drains.



Big capacitance looking into source or drain

Using Folding to Reduce Drain Capacitance

For very large transistors you end up with a bad aspect ratio. To make it a more square shape, fold the transistor. This **folding** also halves the size of the high capacitance diffusion regions of the drains.

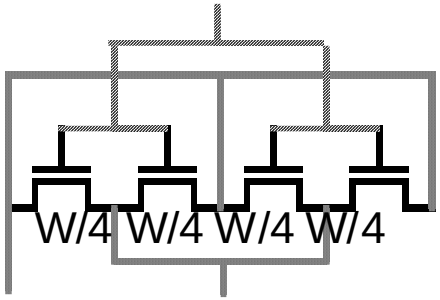


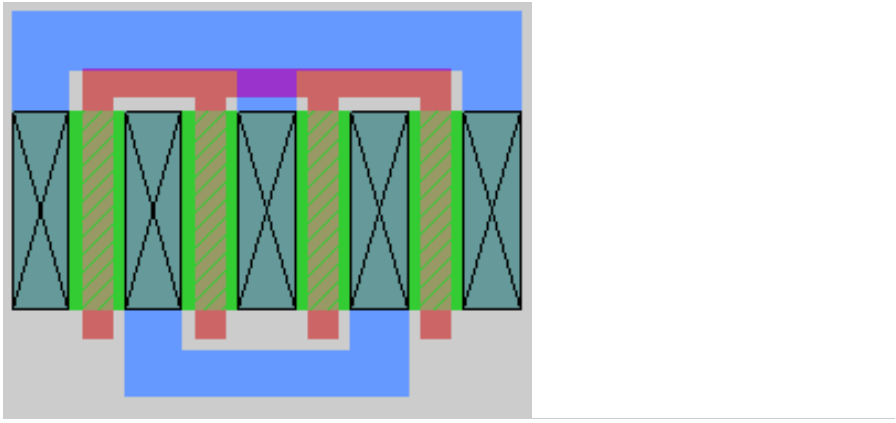
Capacitance seen looking in here is

½ what it is in the original layout

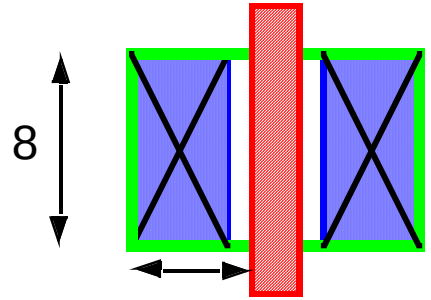
Using Folding to Reduce Drain Capacitance

Can fold it even more, but the payoff is less:





How Folding Transistors Reduces Diffusion Cap



Capacitance for an 8λ device

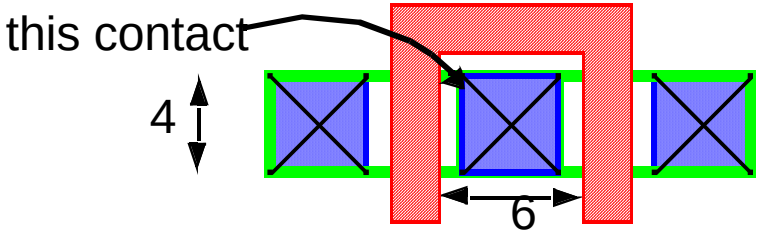
8.5 fF (nMOS)

7.6 fF (pMOS)

8 fF (Class)

$(8 / 2) * (5 / 2) * 0.2\ fF/m^2 + (8/2 + 8/2 + 5/2 + 5/2) * 0.5fF/m = 8.5\ fF$

Reduces the diff cap on one terminal (good if other term is VDD/GND).



Diff Cap =

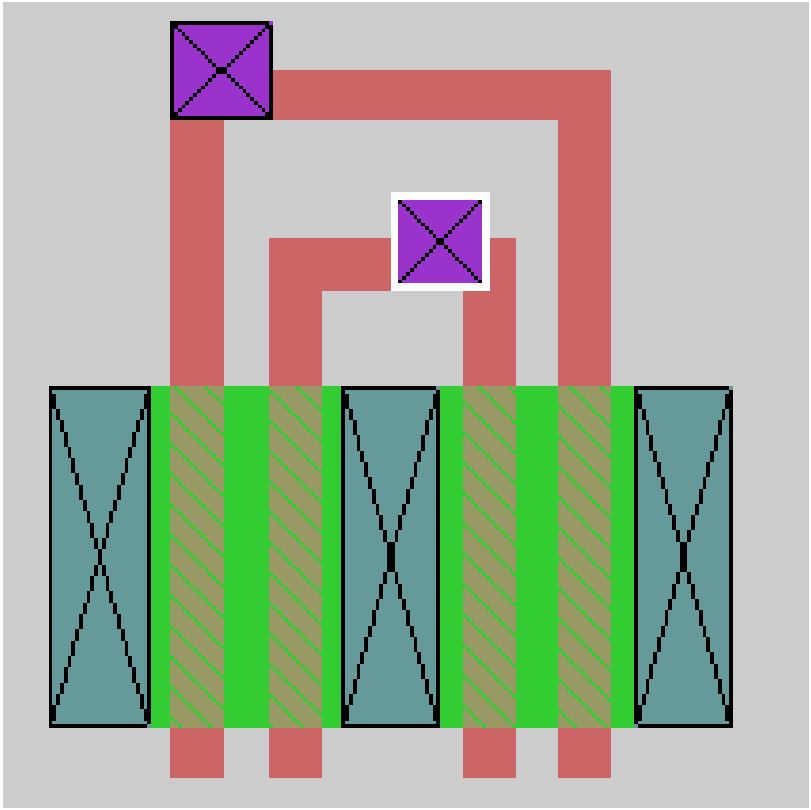
6.2 fF (nMOS)

5 fF (pMOS)

$(6 / 2) * (4 / 2) * 0.2\ fF/m^2 + (4/2 + 4/2 + 6/2 + 6/2) * 0.5fF/m = 6.2\ fF$

Folding Series Transistors

For series stack of devices fold the whole stack, not the individual transistors



Basic Cell Layout Issues

1. P-N spacing is large --> Keep pMOS together and nMOS together. Often mirror cells to keep nMOS in one cell close to nMOS in the other cell. Datapath cells sometimes mirror in both dimensions.
2. Vdd and Gnd distribution needs to be in metal, and often needs wide wires. Vdd runs near the pMOS groups, and Gnd runs near the nMOS
3. Poly should be used for intra-cell wires only
4. Layers alternate directions.
   M1 and M2 should run (predominantly) in orthogonal directions. Otherwise you can easily get into a situation where it is impossible to get any wire into a region.
5. Every cell should be DRC correct in isolation. If a bus or contact is created by abutment, put in both cells, and overlap the edges.
6. If you need to make several versions of something, put the common part in one cell, and then make multiple parents. Don't squash (flatten and copy) unnecessarily. Much easier to make fixes later.