Slide Set 11

MOS Circuit Styles: Pseudo-NMOS, Precharged Logic, …

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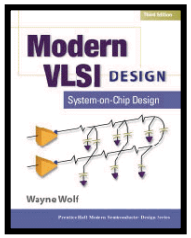
Reference for some of the slides: J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, 2nd Edition, 2003

Overview

Reading: Wolf, Section 3.5



So far we have talked about the two most common forms of logic, static CMOS gates and switch-logic. But there are other forms of gates that people have invented to improve on some of the characteristics of logic gates. We already talked about some of them and we'll introduce some new ones. These improved gates have limitations of their own, and which logic family is best strongly depends on the application. As was mentioned in previous lectures, static CMOS gates are extremely robust gates, and in many design styles they are the only gates that you are allowed to use. But in certain places, especially in custom layout, some alternate circuit configuration can come in handy to increase performance or reduce layout area.

Aside: Large Fan-in Gates

Fan-in refers to the number of inputs of a gate.

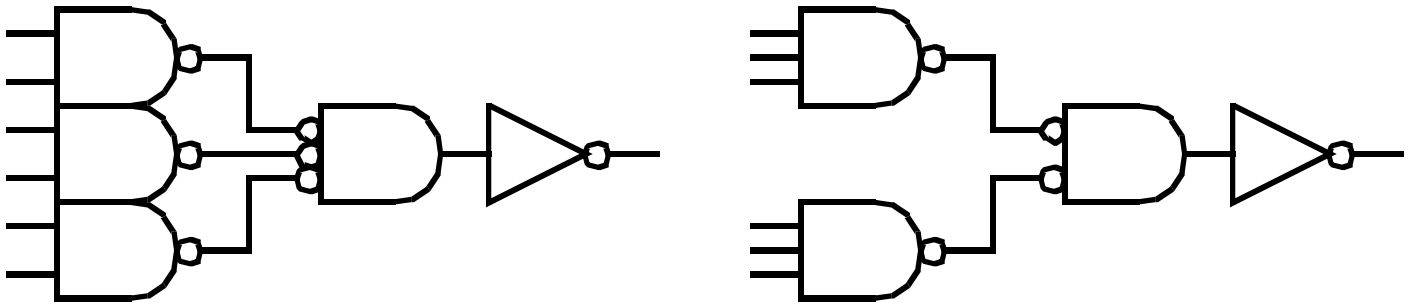
A gate with a large fan-in has a large number of inputs. We know that all CMOS logic gates need a series stack, where the number of transistors in the stack is usually on the order of the number of inputs. For NAND gates, it is a series pull down network, while for NOR gates it is a series pull up network.

Since series stacks are slow, to limit the height of the stack we need to limit the fan-in of the gate to 3 or 4.

If you need a large fan-in gate, what can you do? For example let's assume we want to implement a 6-input NAND gate.

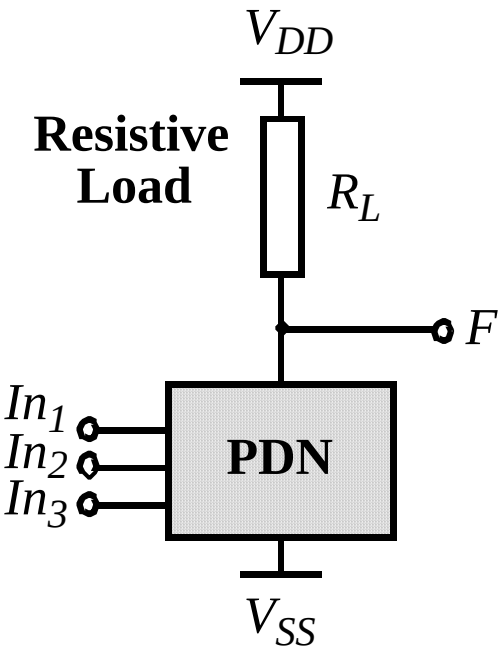
Example

The following two circuits both implement a 6-input NAND gate



NMOS Technology

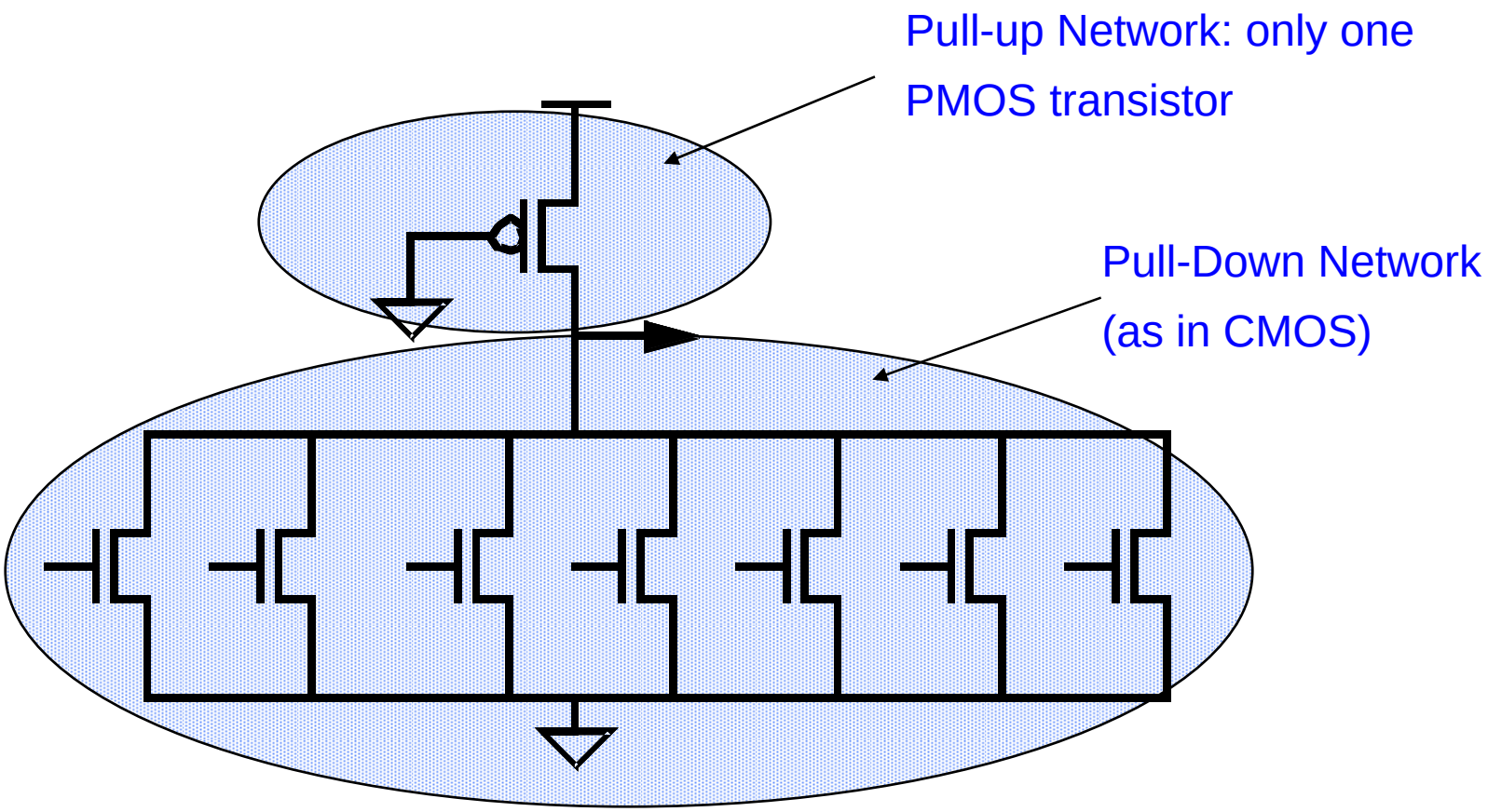
NMOS technology (70's & 80's) was great for high fan-in gates since a resistor or a *depletion* transistor (conducts even when V_{gs}=0) was used as the pull-up and one only needed to build the pull-down network. For NOR gates, the pull-down network used only parallel transistors.



(a) resistive load

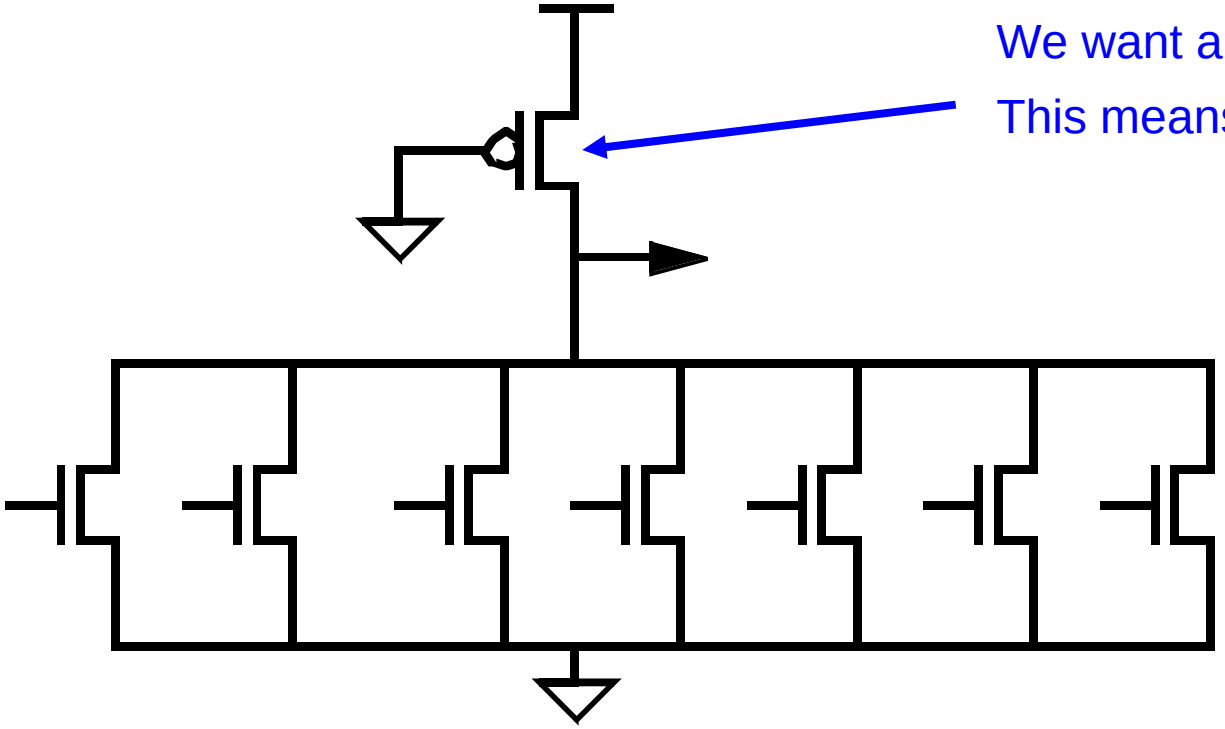
Pseudo-NMOS

CMOS technology does not have depletion pull-ups, instead we use a PMOS with its gate grounded as a PUN:



Advantages: fan-in of n requires n+1 transistors, potentially smaller area and higher speed

Pseudo-NMOS



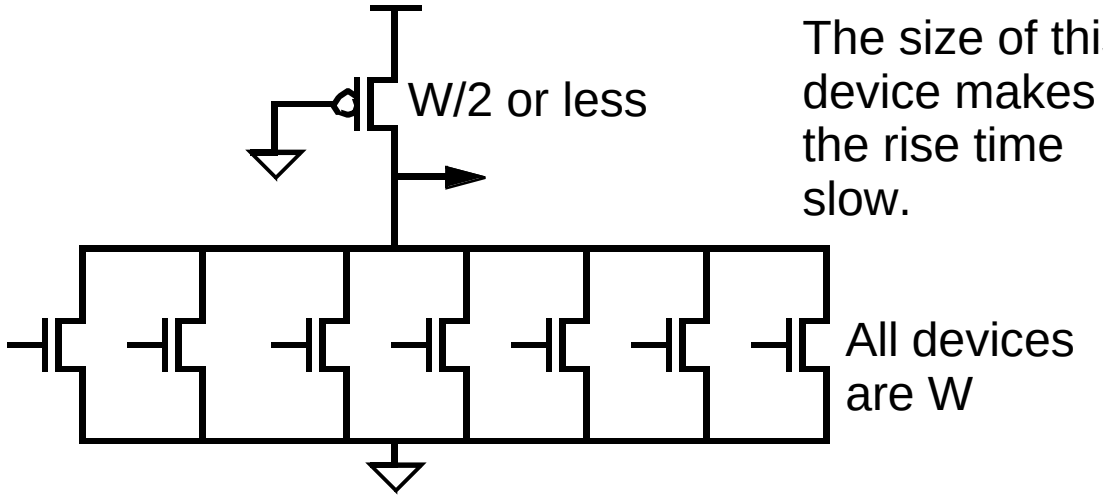
We want a big Ron,p

This means small W (or big L)

Problems: Static Power Consumption, Degraded ‘0’ output, Ratioed logic, typically have asymmetric response,

Pseudo-NMOS: Power and Sizing Issues

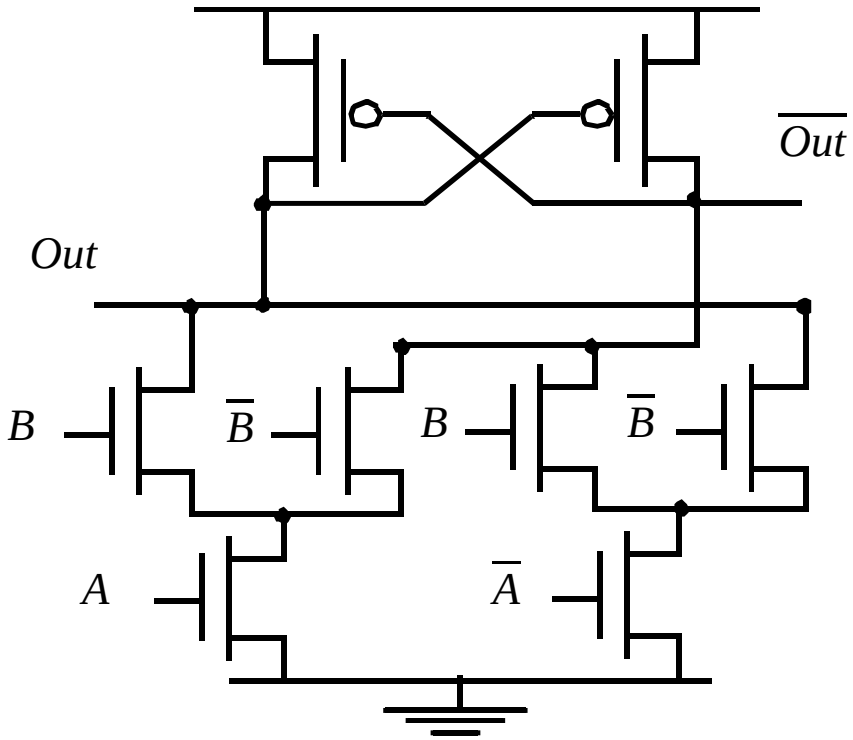
- NMOS technology (by itself) become unpopular due to its high power dissipation
- Every gate with its output low dissipated power (that's typically half the gates on a chip!); the same is true for Pseudo-NMOS



- To size the devices, we must ensure that the pull-down current is large enough to get a valid low output (however, never can get exactly 0V).
  - e.g., For 4:1 current ratio, the NMOS width (Wn) must be twice Wp
- Because functionality depends on device ratios, it is called RATIOED logic

Board Notes: Differential Cascode Voltage Logic

DCVSL Example



XOR-NXOR gate

Dynamic (Precharged) Logic

- In static circuits at any given time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* NMOS + *n* PMOS) transistors

- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires *n* + 2 (*n*+1 NMOS + 1 PMOS) transistors
  - takes a sequence of precharge and conditional evaluation phases to realize logic functions

Board Notes: Precharged Logic

Properties of Dynamic Logic

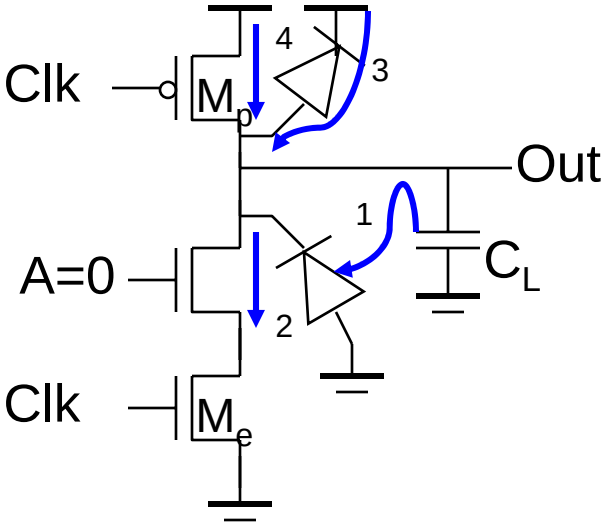
- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed: Sizing of the devices does not affect the logic functionality
- Faster switching speeds
  - reduced load capacitance due to fewer number of transistors per gate
  - no I_{sc}, so all the current provided by PDN used to discharge C_L
  - Ignoring the influence of precharge time on the switching speed of the gate, t_{pLH} = 0 but the presence of the evaluation transistor slows down the t_{pHL}

Properties of Dynamic Logic

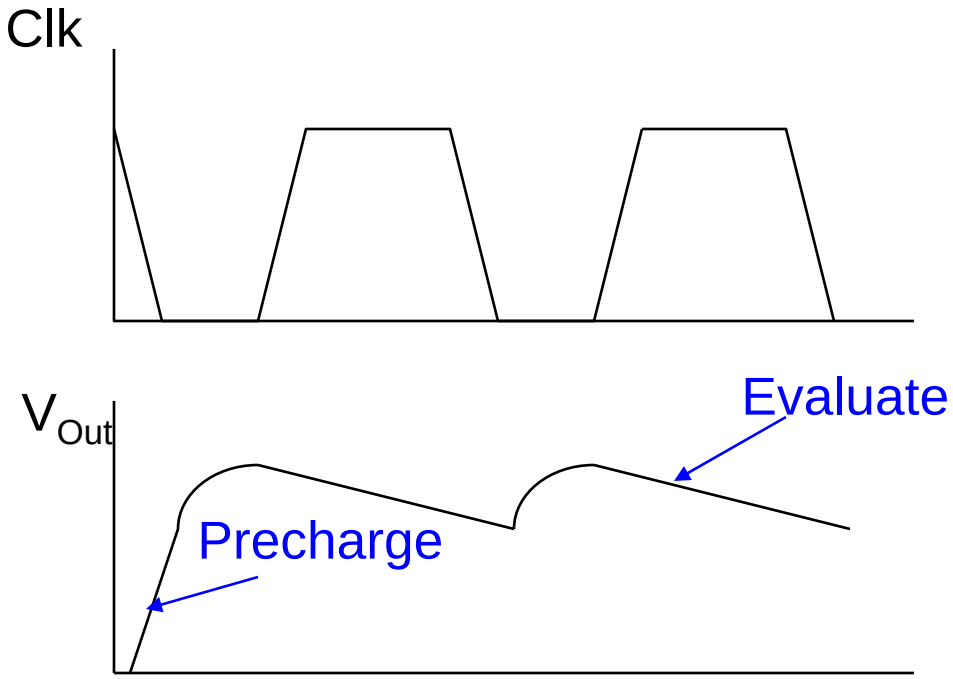
- Overall power dissipation usually higher than static CMOS:
  Although no static current path ever exists between V_{DD} and GND dynamic gates have
  - higher transition probabilities
  - extra load on Clk

- Needs a precharge/evaluate clock

Issues in Dynamic Logic Design: Charge Leakage



Leakage sources

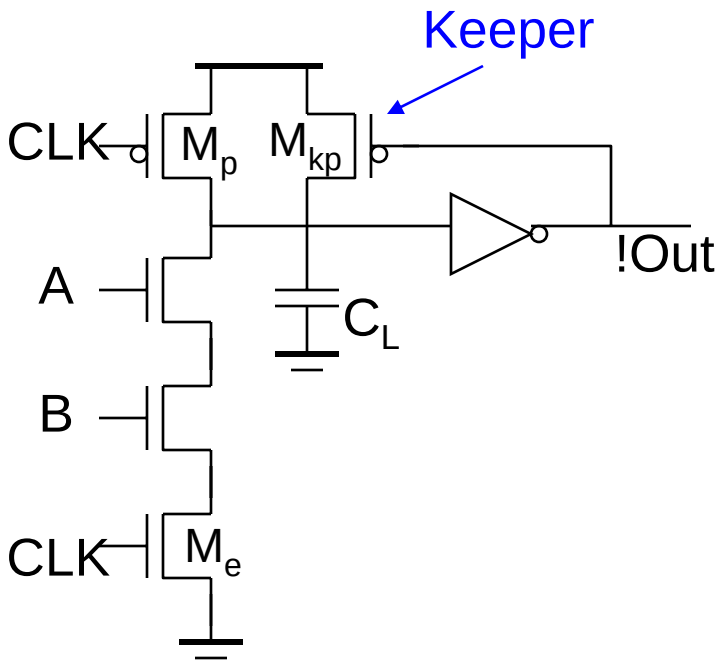


Once the output drops below the switching threshold of the fan-out logic gate, the output is interpreted as a low voltage.

Thus, due to leakage minimum clock rate of a few kHz is required

A Solution to Charge Leakage

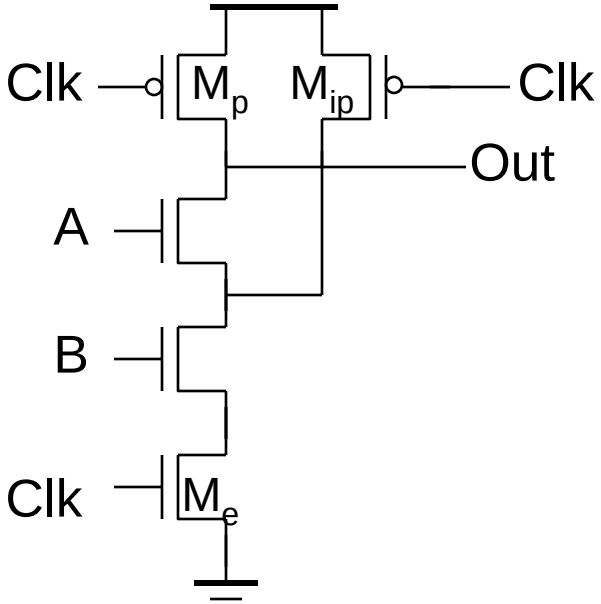
- **Keeper** compensates for the charge lost due to the pull-down leakage paths.



Same approach can be used as level restorer in pass transistor logic and dynamic latches

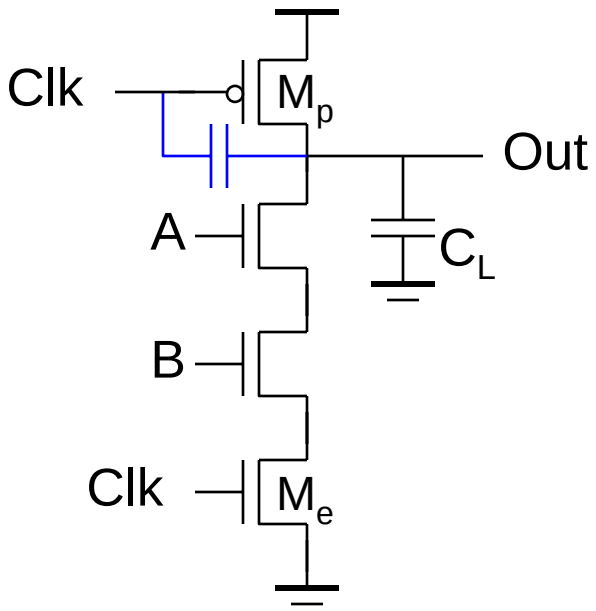
Board Notes: Charge Sharing

Solution to Charge Sharing



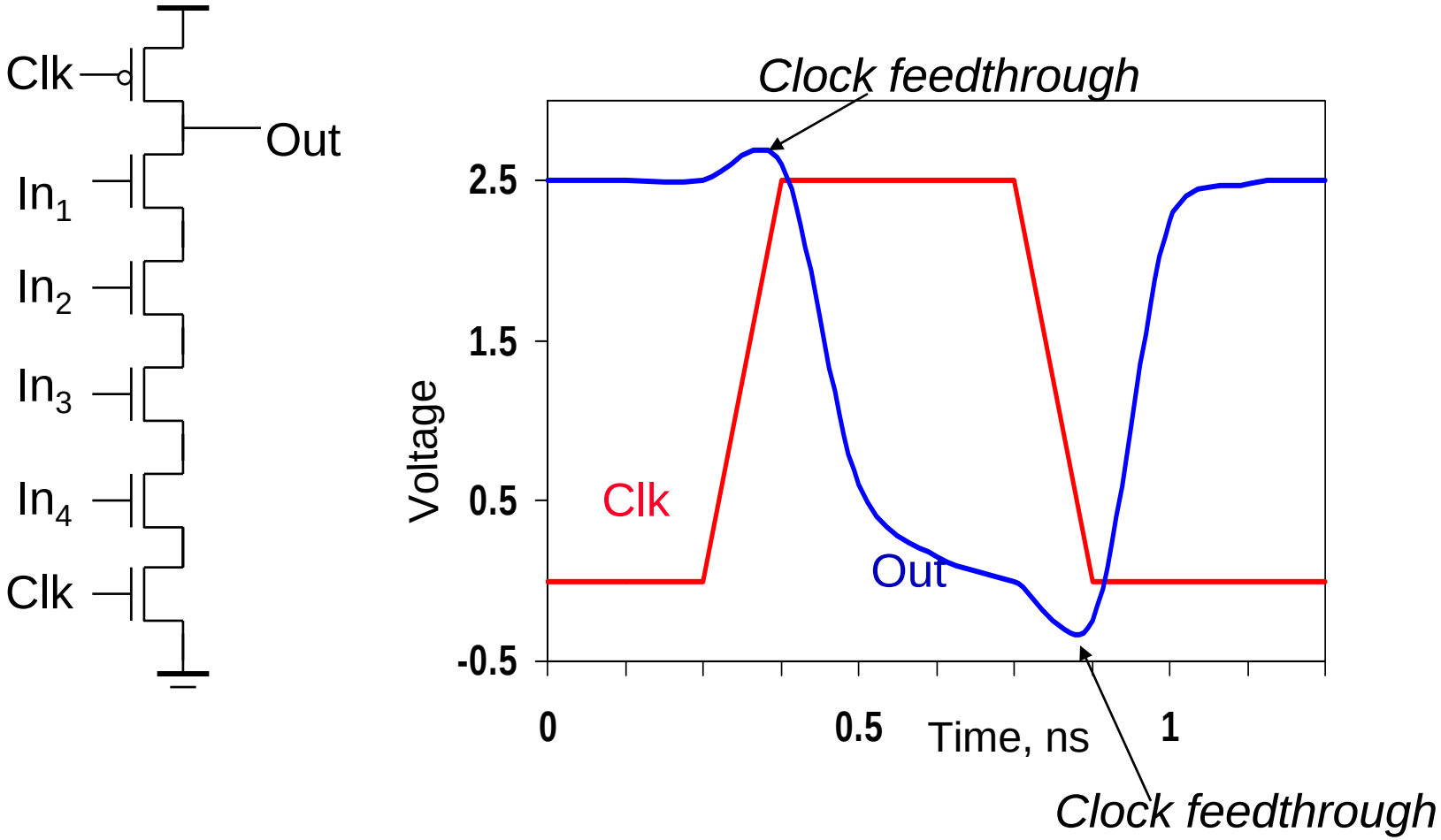
Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

Issues in Dynamic Logic Design: Clock Feedthrough



Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD} or below GND. The fast rising (and falling edges) of the clock couple to Out.

Clock Feedthrough

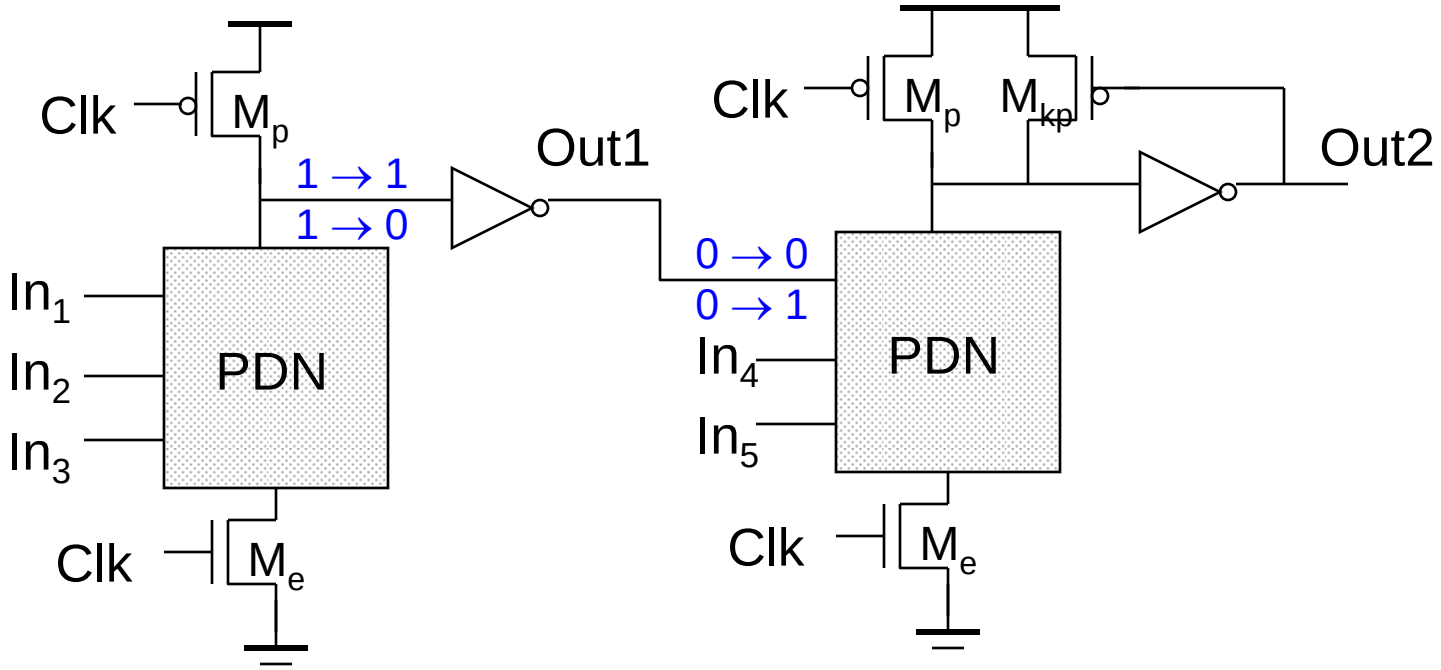


Other Issues

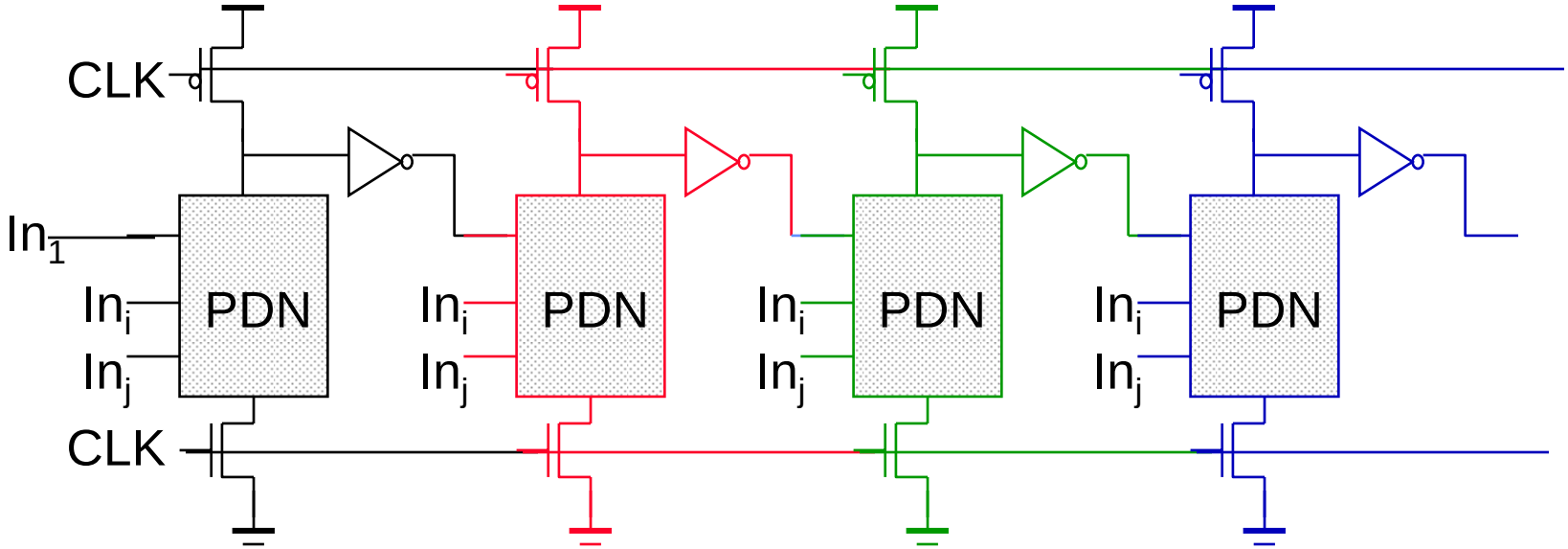
- Capacitive coupling (clock feedthrough is a special case of capacitive coupling)
- Substrate coupling
- Supply noise

Board Notes: Cascading Dynamic Gates and Intro to Domino Logic

Domino Logic



Why the Name Domino?

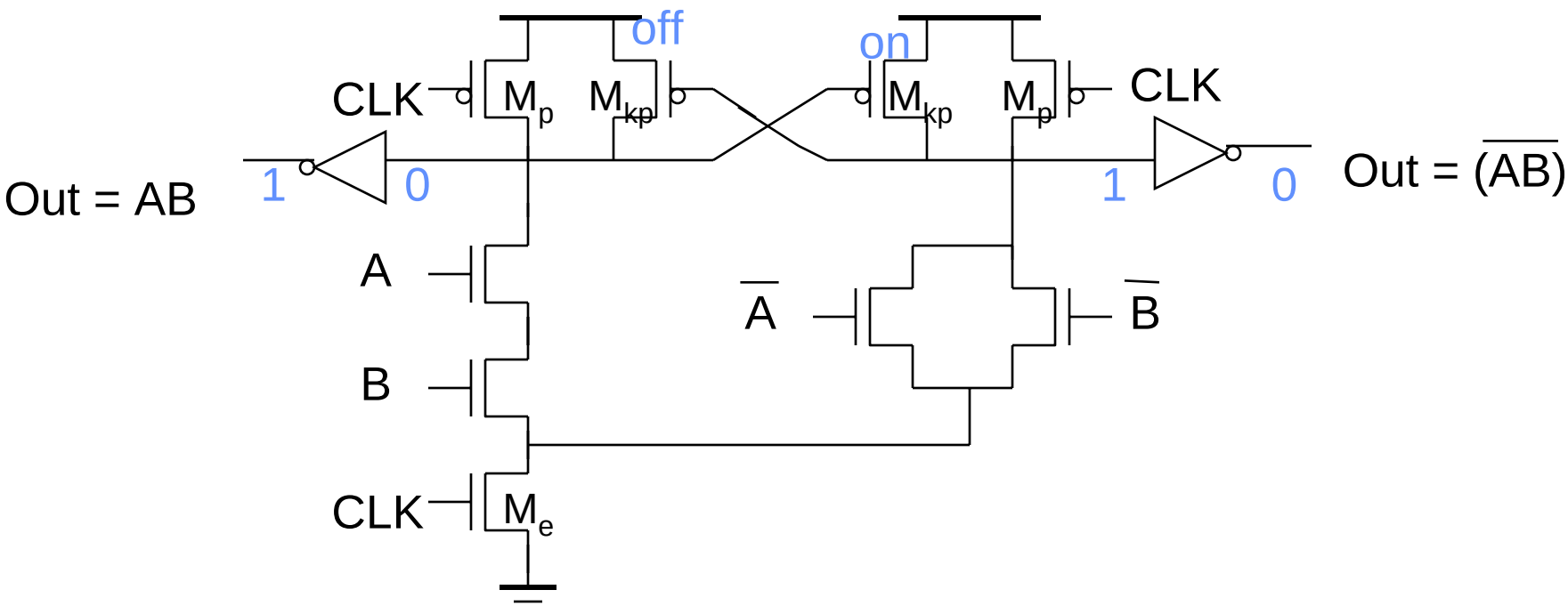


Like falling dominos!

Properties of Domino Logic

- Only non-inverting logic can be implemented, fixes include
  - can reorganize the logic using Boolean transformations
  - use differential logic (dual rail)
  - use np-CMOS (zipper)
- Very high speed
  - $t_{pHL} = 0$
  - static inverter can be optimized to match fan-out

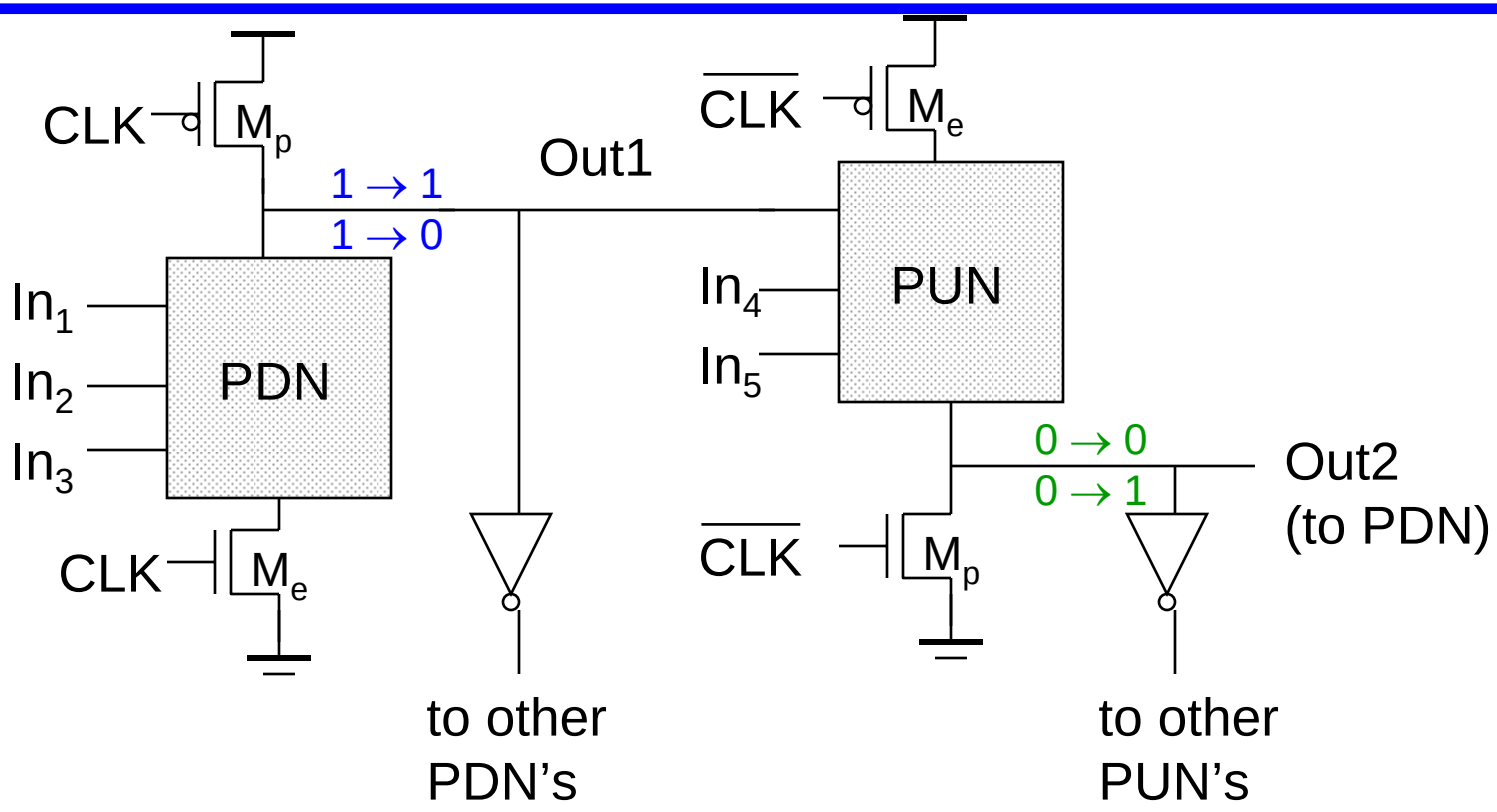
Differential (Dual Rail) Domino



Due to its high-performance, differential domino is very popular and is used in several commercial microprocessors!

Board Notes: Zipper Logic

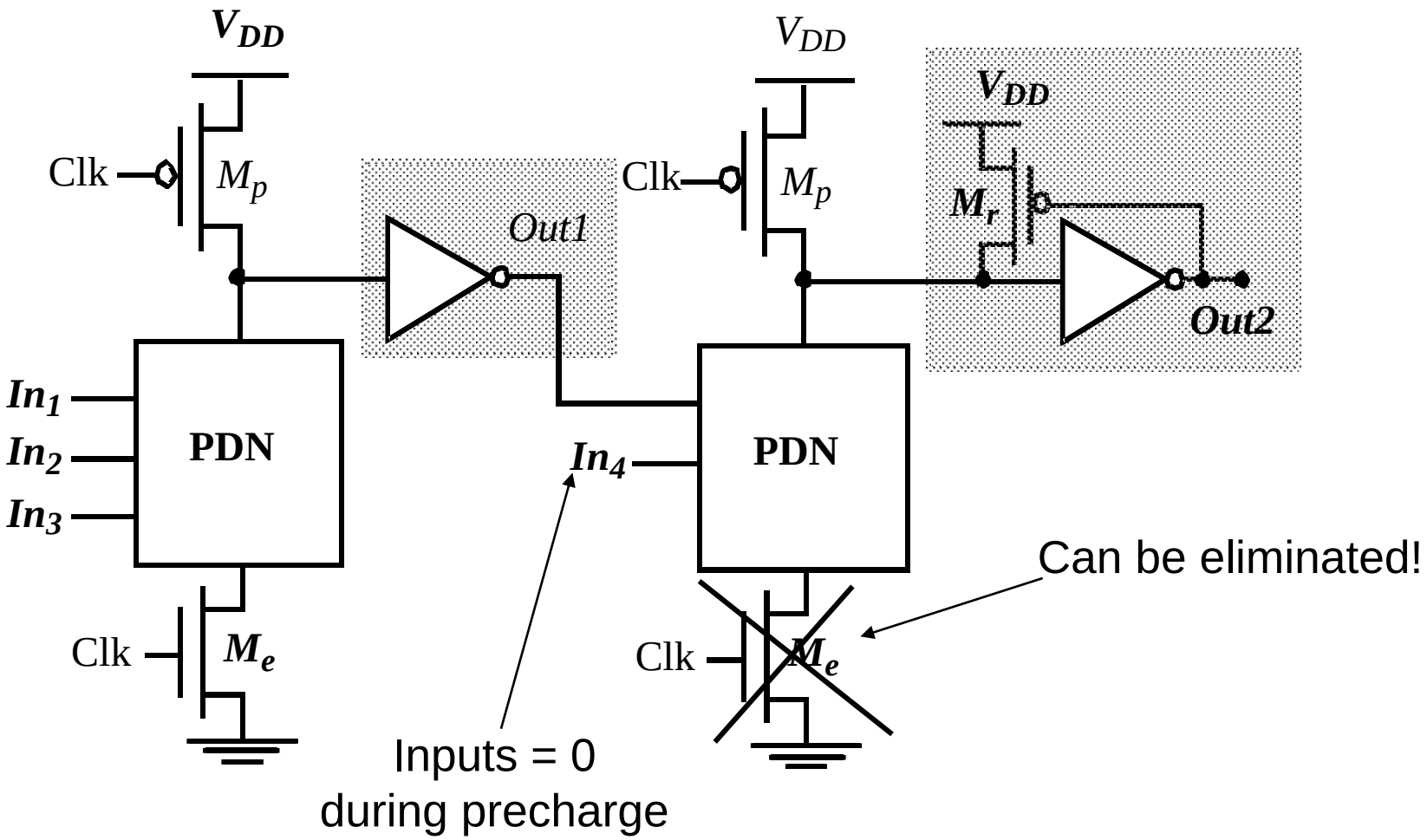
np-CMOS (Zipper)



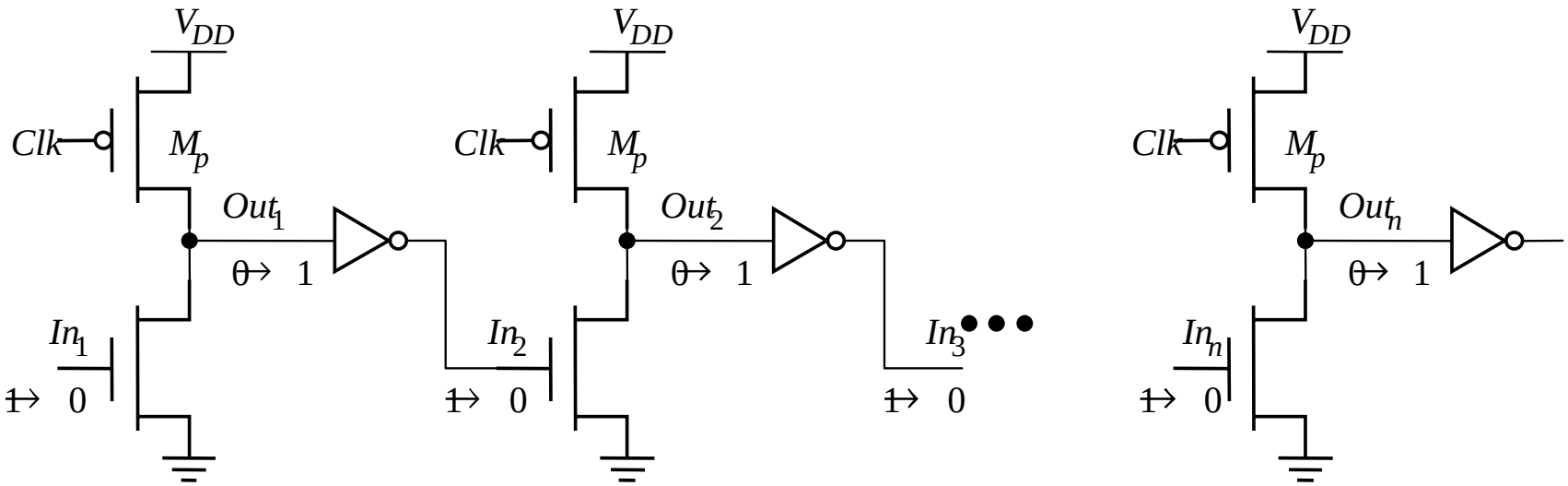
Only $0 \rightarrow 1$ transitions allowed at inputs of PDN

Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

Designing with Domino Logic



Footless Domino



The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current
A solution is to delay the clock for each stage