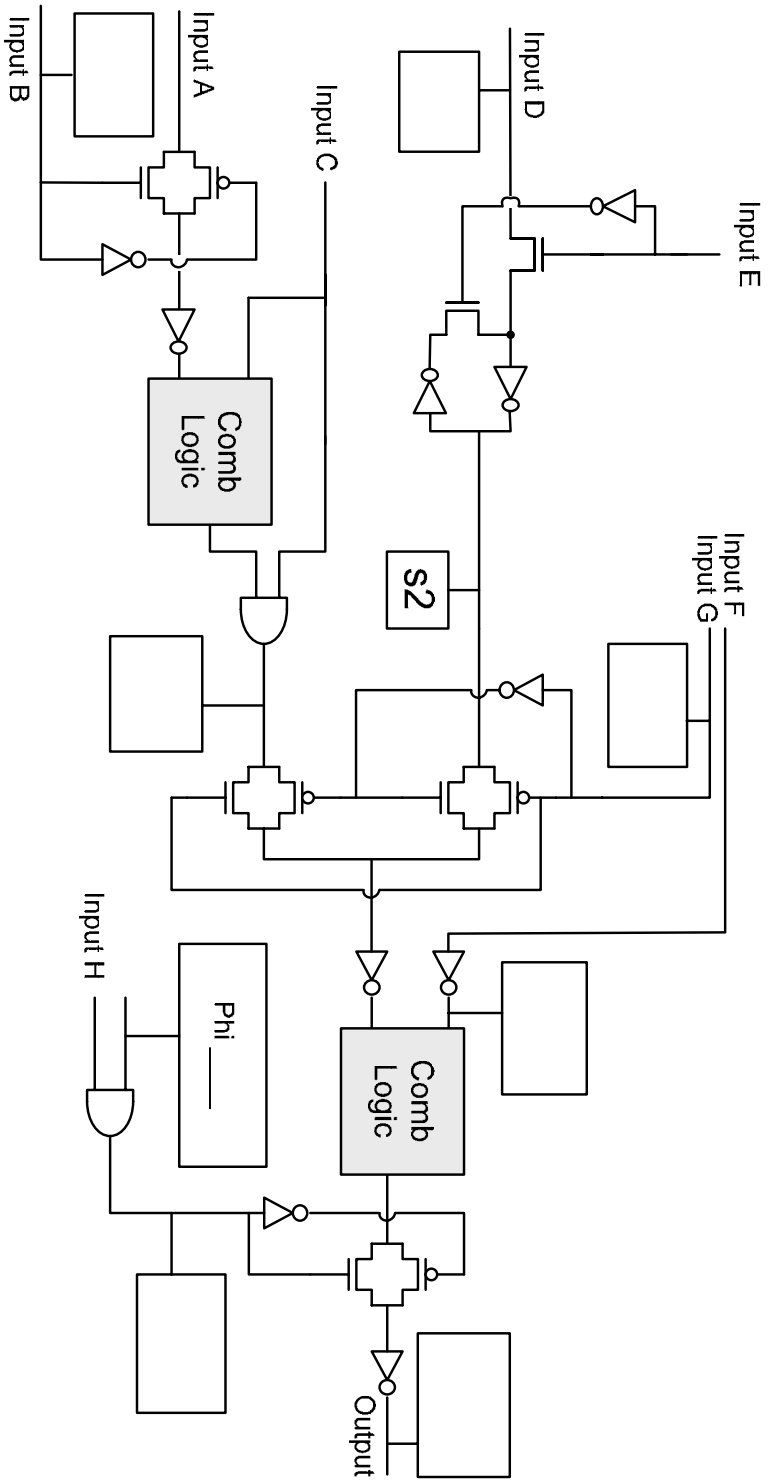
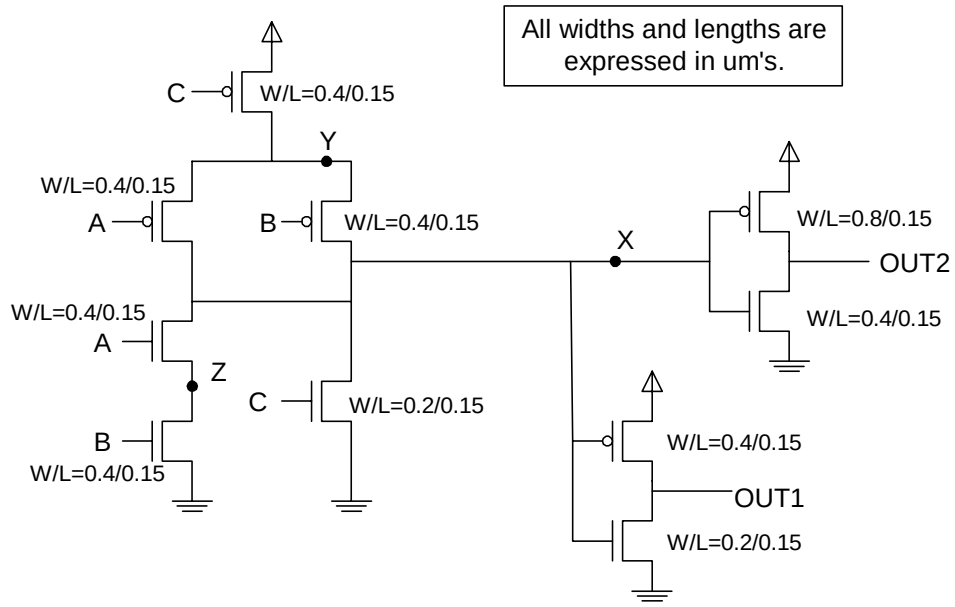
Consider the following two-phase clocked circuit. Using the labeling convention discussed in class, **fill in each box below with one of: s1, s2, q1, q2, v1, v2, phi1, or phi2** depending on the timing type of the corresponding signal. One of the signals has been labeled as having type s2 for you; this is the place to start.



Answer the following questions regarding the circuit below. You might find these numbers useful (you may not need all of them). Note this technology is different that the one in class. You should use this new technology.

λ = 0.06μm (so the minimum transistor length is 0.12 μm)
Cgate = 1.4 fF/μm of transistor width
Cndiff = 1.2 fF/μm of transistor width
Cpdiff = 1.0 fF/μm of transistor width
*Ron,n = 12 KΩ * L/W*
*Ron,p = 24 KΩ * L/W*
Vdd = 1.2 volts

Also assume the layout engineer for this gate wasn't very smart (clearly not from UBC) and so he/she did not share diffusion regions between transistors (so every transistor has its own source/drain region).



Assume the following nodes have the following initial voltage:

Node Z: initial voltage = 0 volts
Node Y: initial voltage = 1.2 volts
Node X: initial voltage = 1.2 volts

Also assume the inputs initially have the following voltages:

Input A: initial voltage = 0 volts
Input B: initial voltage = 1.2 volts
Input C: initial voltage = 0 volts

Suppose Input A switches from 0 Volts to 1.2 Volts. Clearly, Node X will fall. On the next page, work out the delay until Node X reaches 0.6 Volts (Vdd/2). Show your work!