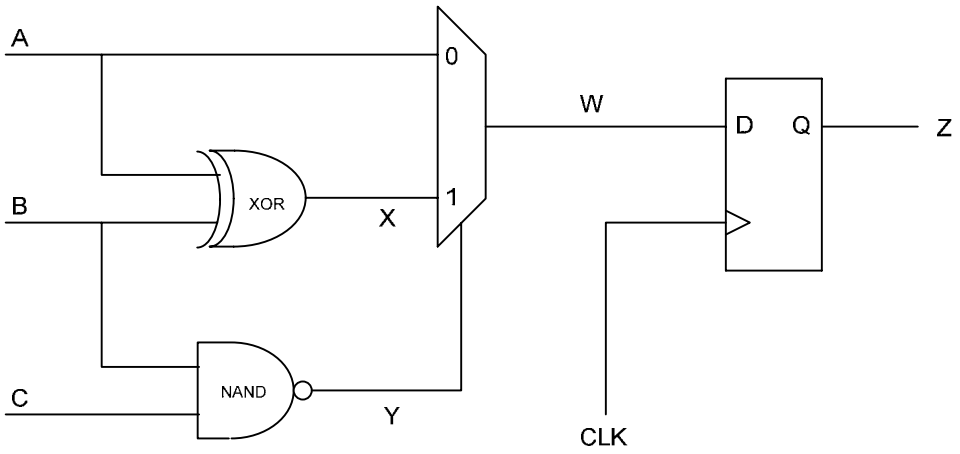
8) POWER

Consider the following circuit. A, B, and C are inputs, Z is an output, and CLK is the clock. Assume the clock is a normal single-phase clock that is high 50% of the time.



(a) On the next page, you are to determine the power dissipated by the circuit. Include all components of power we have talked about in class. Assume the process from Page 2 is used. You can also assume the following (you may not need all this information):

Parasitic capacitance at node A: 4 fF
Parasitic capacitance at node B: 3 fF
Parasitic capacitance at node C: 2 fF
Parasitic capacitance at node CLK: 6 fF
Parasitic capacitance at node X: 1 fF
Parasitic capacitance at node Y: 2 fF
Parasitic capacitance at node W: 4 fF
Parasitic capacitance at node Z (the output): 5 fF
Leakage power for multiplexer: 10 nW
Leakage power for flip-flop: 14 nW
Leakage power for NAND gate: 6 nW
Leakage power for XOR gate: 4 nW
Short-Circuit Power is 10% of Switching Power
Probability that input A is high: 0.3
Probability that input B is high: 0.5
Probability that input C is high: 0.8
Probability that input CLK is high: 0.5 (standard single-phase clock signal)
Clock Frequency: 100 Mhz

Answer the question on the next page. You can remove this page from the booklet if desired. No writing on this page will be marked.