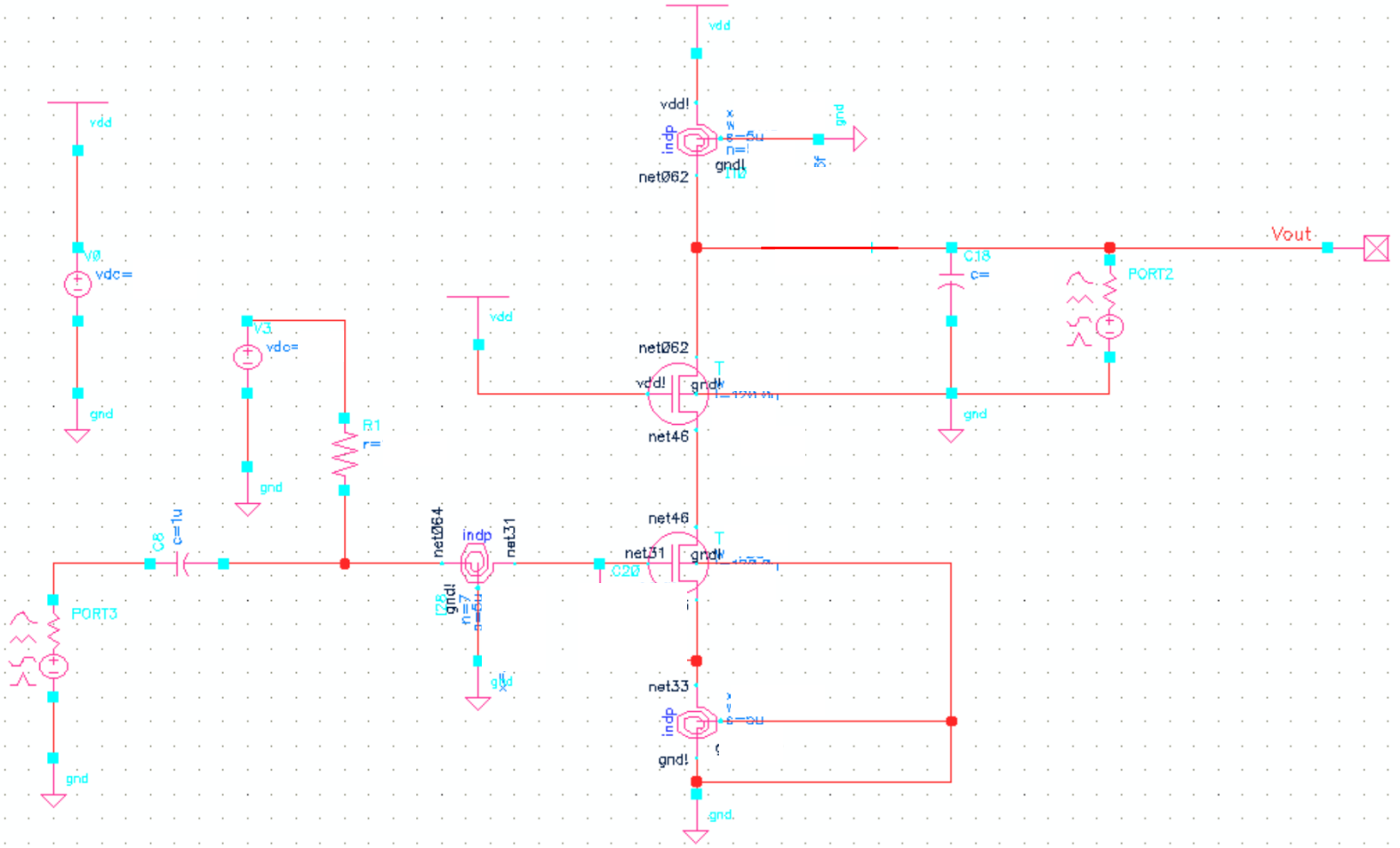
Lecture 7:
LNA Design

ELEC 404

Example Specifications

- Operating frequency f_0 and BW:
- Minimum voltage gain (A_v or S21): ~ 15dB
- Input Matching to 50/100Ω: S11 < -10dB
- Maximum Power Consumption: ~5-10mW
- Maximum NF: ~2-4dB
- Minimum IIP3: ~ 0dBm
- 1dB compression point: ~ -10dBm
- Supply Voltage Vdd

Example Design: L-degenerated CSLNA



Pick Ld at the Output Network

- Maximize load resistance R_p

- Depends upon the process
- Be aware of self-resonant frequency of L_d.

Pick Ld at the Output Network

- Check Q_{out} to ensure BW specification

- Find the required transconductance, G_m

Pick Qin at the Input Network

- Find Q_{in} for minimum S_N
- If gate-induced noise is ignored (!), "maximize" Q_{in} while meeting gain, linearity and BW specs
- Obtain Q_{in} from BW specification.

Find gm of the Main CS Transistor

- Find the required transconductance, G_m

- Find the Main CS transistor gm

Find W of the Main CS Transistor

- With Q_{in}, C_{ox} and L_{min}, calculate W.

Find gm of the Main CS Transistor

- Plot g_m, g_{ds}, V_{gs} vs. current density of the NMOS
- Operate the NMOS in weak to moderate inversion for noise vs. linearity tradeoff.
- With I_{den} and V_{gs}-V_{th}, calculate normalized-g_m.

- With normalized-g_m and W, calculate g_m.

Is the Gain Adequate?

- Compare the two values of gm of Main CS transistor

Find Ls

- Find f_T and L_s:

Find Lg

- Calculate L_g from f_0:

Complete the Design

- Connect the cascode device.

- Simulate and reiterate.

Output Matching

- If output matching is needed, design a tapped-cap transformation network.

- If unable to meet specs
  - Consider adding an explicit C_{GS}
  - Choose a different design topology.
- Simulate and reiterate.