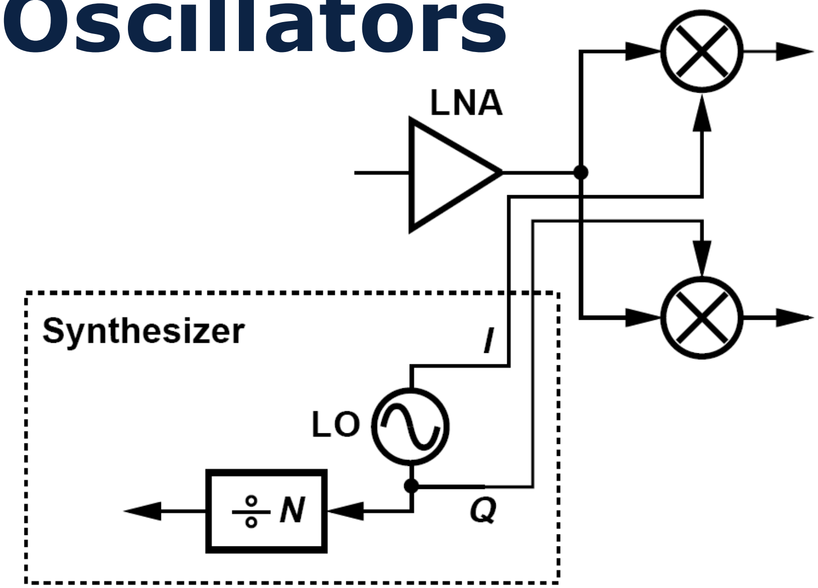
Radio-Frequency IC Design

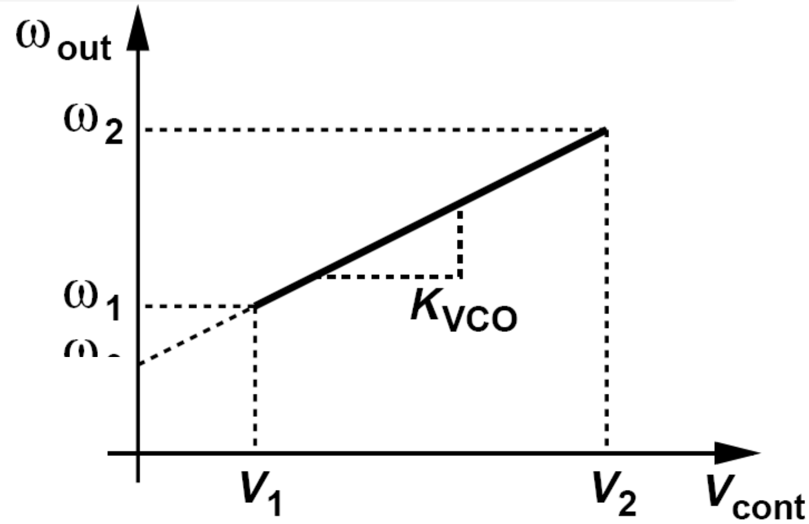
Lecture 10:
Voltage Controlled Oscillators



ELEC 404

Acknowledgement: *RF Microelectronics*. B. Razavi

VCO: Tuning Curve



$$\omega_{out} = K_{VCO} V_{cont} + \omega_0$$

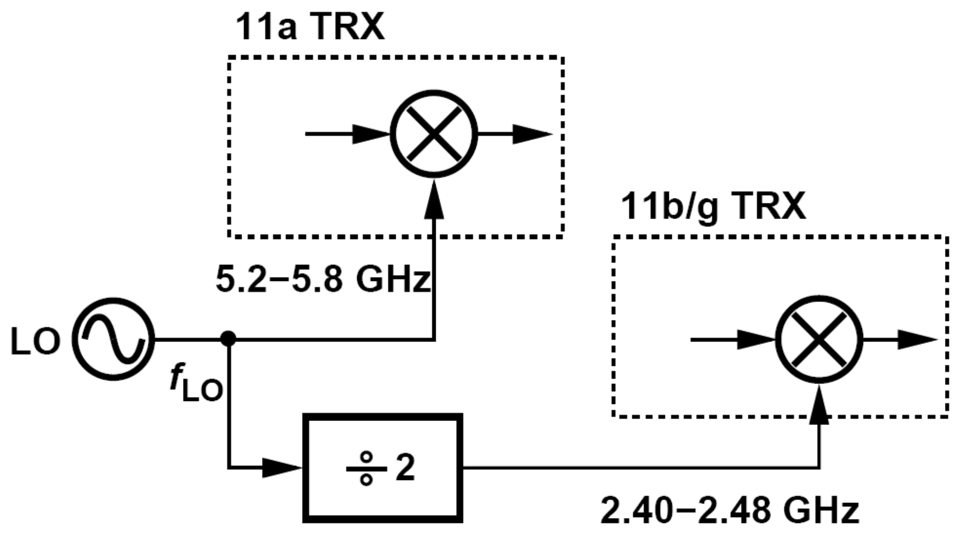
- **Center Frequency: (ω_1 to ω_2)/2**
- **VCO Gain/Sensitivity: K_{VCO} = Slope expressed in rad/s/V.**
- **Tuning Range: $\omega_2 - \omega_1$**
- **Tuning Range Includes:**

  (1) the system specification;

  (2) additional margin to cover process & temperature variations and errors due to modeling inaccuracies.

Tuning Range Example

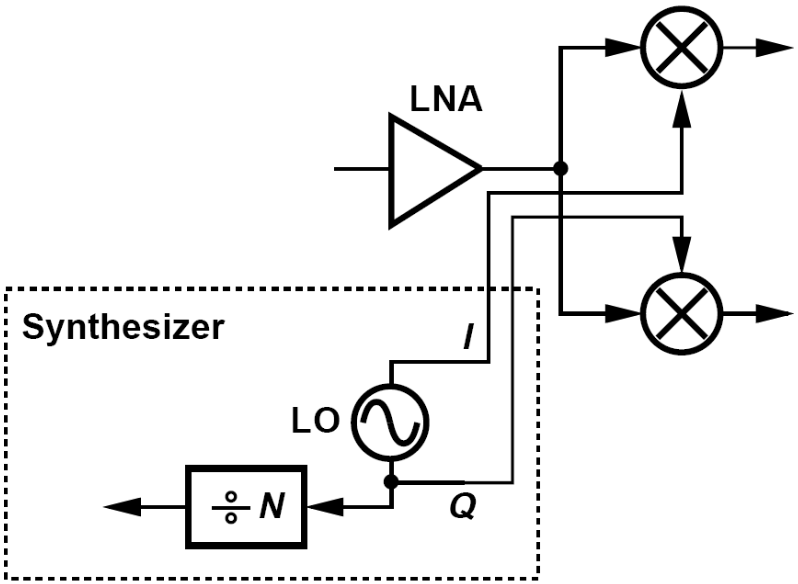
A direct-conversion transceiver must cover both the 2.4-GHz and 5-GHz wireless bands with a single LO. What is the minimum acceptable tuning range?



For the lower band, 4.8 GHz ≤ f_{LO} ≤ 4.96 GHz.
Thus, total tuning range of 4.8 GHz to 5.8 GHz ~ 20% → difficult in LC oscillators.

Drive Capability

- **LO has output swing and drive capability tradeoff, for mixers and dividers as load.**



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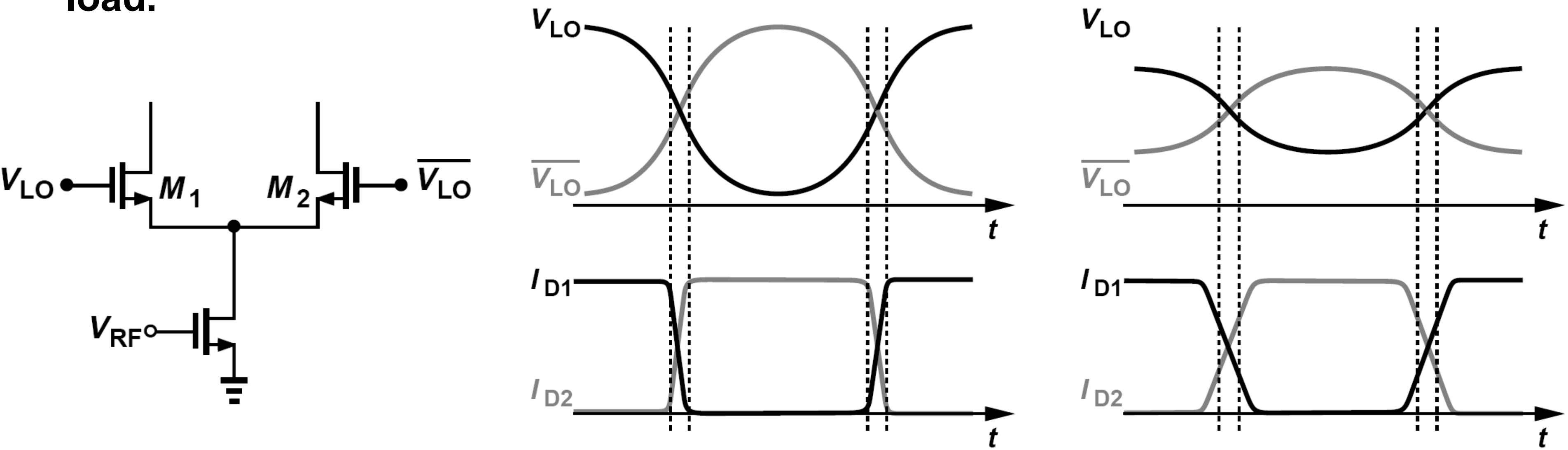
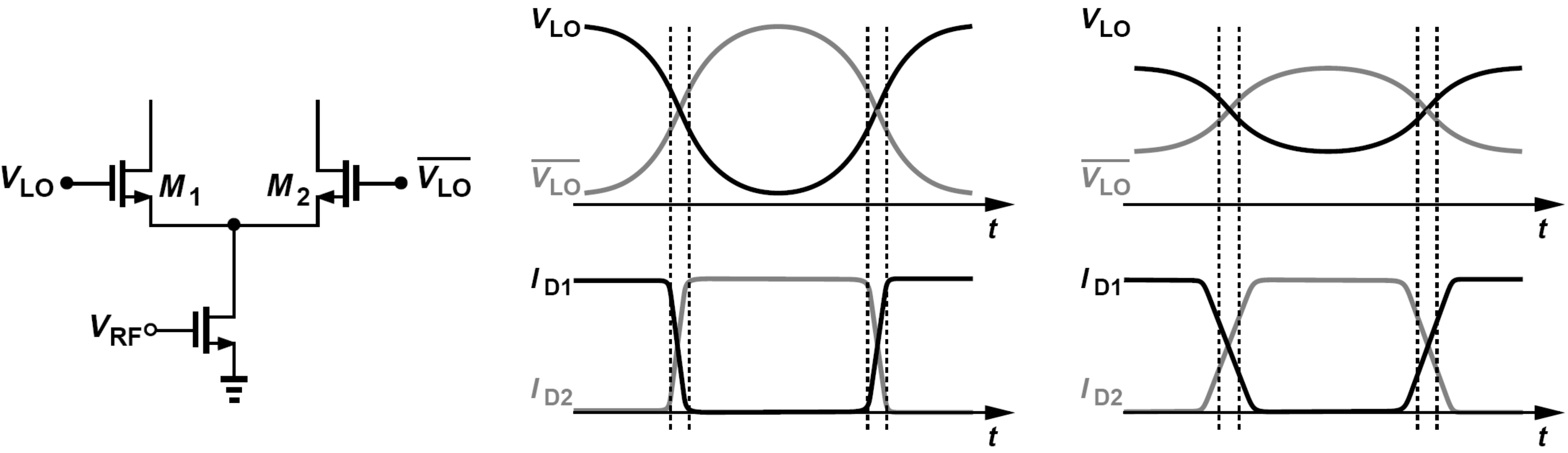
- LO has output swing and drive capability tradeoff, for mixers and dividers as load.



- Select large LO swings so that V_{GS1}-V_{GS2} rapidly reaches a large value, turning off one transistor.
- Or, employ smaller LO swings but wider transistors so that they steer their current with a smaller differential input.
- To alleviate the loading presented by mixers and dividers and perhaps amplify the swings, follow the LO with a buffer.

Ideal Output Waveform

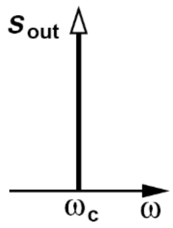


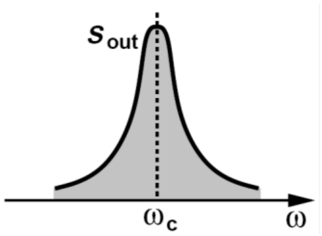
- Sharp, abrupt LO transitions reduce the noise and increase the conversion gain of Mixers.
- Sharp transitions also improve the performance of frequency dividers.
- 50% duty cycle LO to suppress direct feedthrough.
- Ideal LO waveform in most cases is a square wave.

Output Waveform in Practice

- Difficult to generate square LO waveforms in practice.
- Differential LO waveforms for a number of considerations.

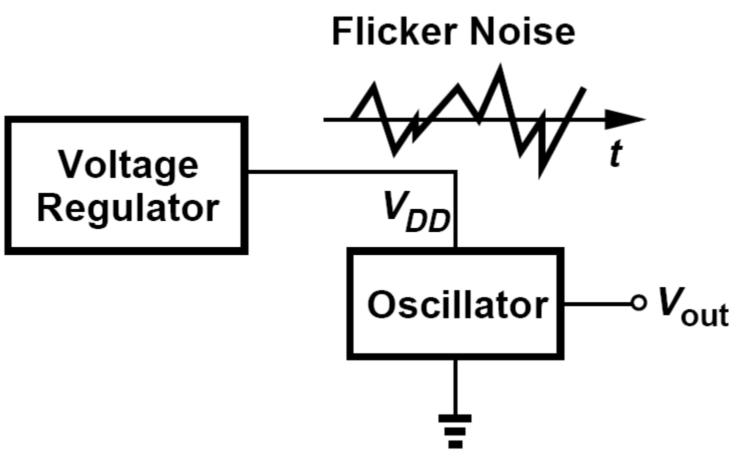
- LO spectrum in practice deviates from an impulse and is "broadened" by the noise of its constituent devices, called "phase noise".
- Phase noise trade-offs with the tuning range and power dissipation
- Very low output swings exacerbate the effect of the internal noise of the oscillator.





Supply Sensitivity

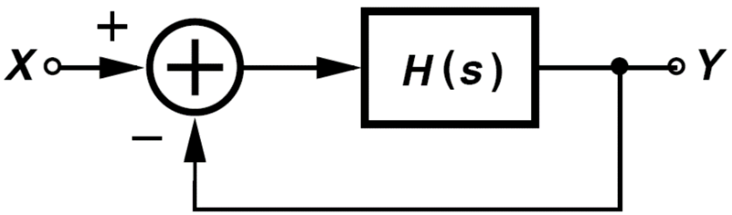
- If LO frequency varies with the supply voltage, it can translate supply noise to frequency (and phase) noise.



Feedback Model of Oscillators

- **An oscillator may be viewed as a "badly-designed" negative-feedback amplifier—so badly designed that it has a zero or negative phase margin.**

$$\frac{Y}{X}(s) = \frac{H(s)}{1+H(s)}$$



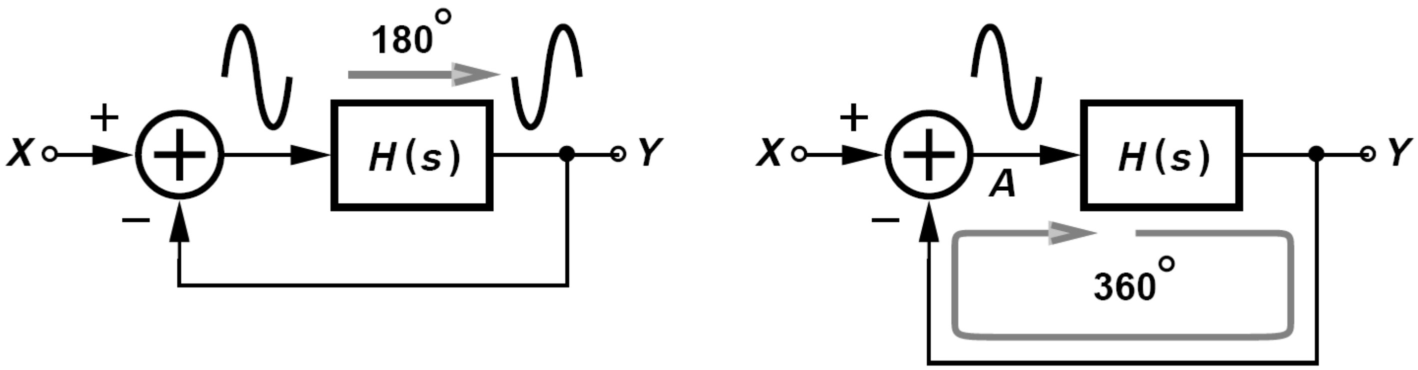
- **When will this system oscillate?**
  - **Barkhausen Criteria**

$$\begin{aligned} |H(s=j\omega_1)| &= 1 \\ \angle H(s=j\omega_1) &= 180^\circ \end{aligned}$$

- **Total phase shift experienced by signal at ω_1 = 360˚.**

Barkhausen's Criteria

$$|H(s = j\omega_1)| = 1$$
$$\angle H(s = j\omega_1) = 180^\circ$$

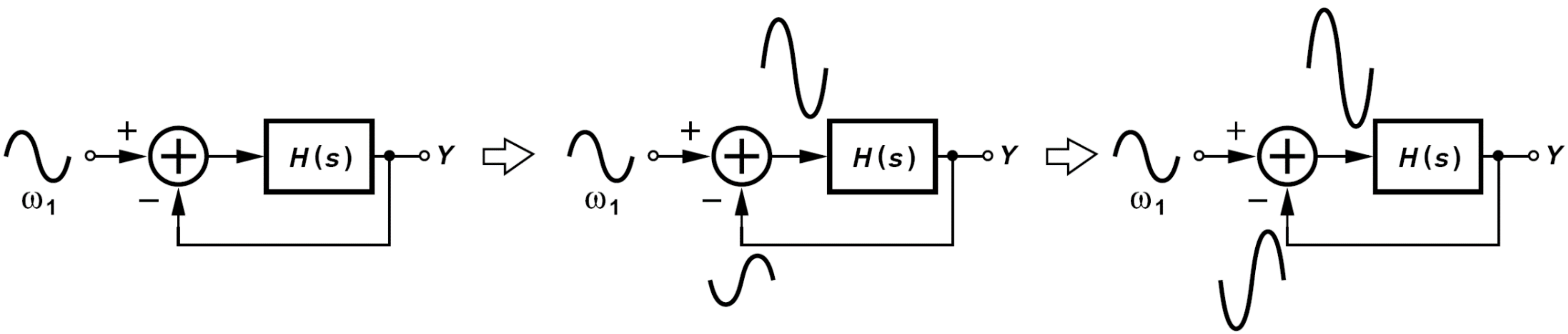


- For the circuit to reach steady state, the signal returning to A must exactly coincide with the signal that started at A.
- 180° phase due to negative feedback
- 180° "frequency-dependent" phase shift due to $\angle H(j\omega_1)$,

  → Changes original negative feedback system to positive feedback at ω_1 !

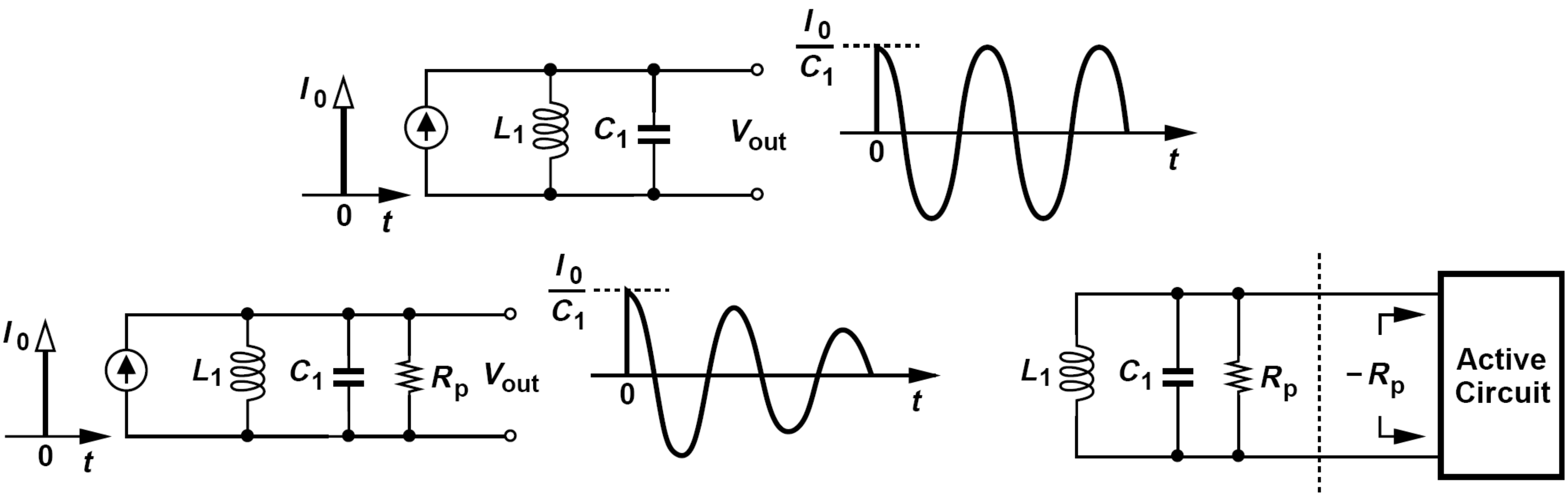
Significance of $|H(j\omega_1)| = 1$

- For a noise component at ω_1 to "build up" as it circulates around the loop with positive feedback, the loop gain must be at least unity.
- $|H(j\omega_1)| = 1$ is called the "startup" condition.



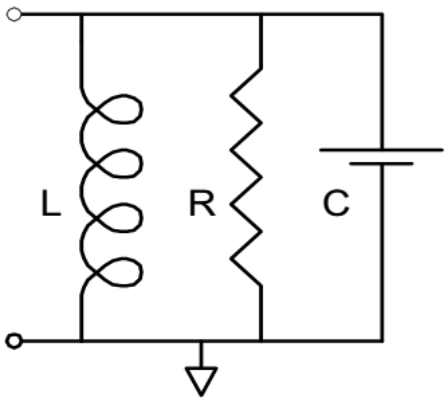
- If $|H(j\omega_1)| > 1$ and $\angle H(j\omega_1) = 180°$, growth occurs at a faster rate because the returning waveform is amplified by the loop.
- Note that the closed-loop poles now lie in the right half plane.

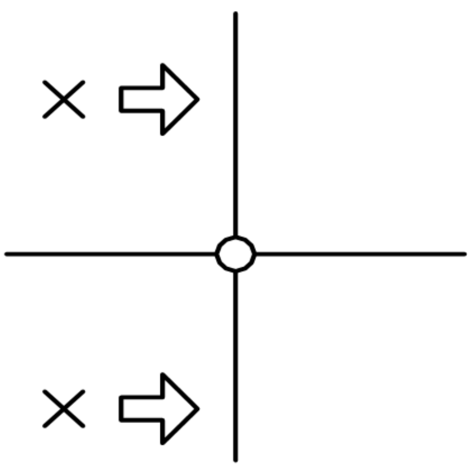
One-Port Model of Oscillators



- **If an active circuit replenishes the energy lost in each period, then the oscillation can be sustained.**

One-Port Model of Oscillators



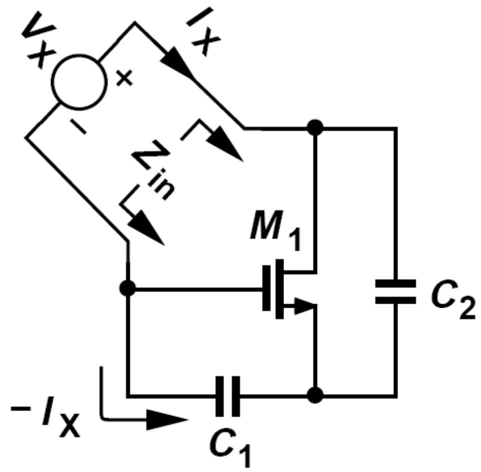


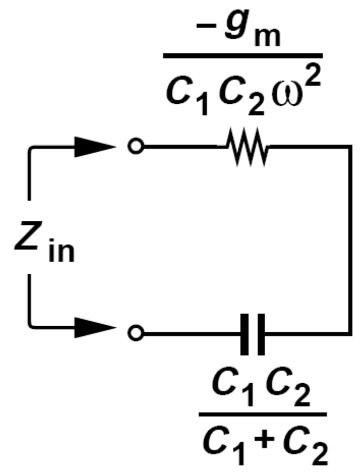
$$Z_{RLC} = \frac{sL}{1 + s^2LC + sGL}$$

$$p_{1,2} = \frac{-GL \pm \sqrt{(GL)^2 - 4LC}}{2LC}$$

$$p_{G\to 0} = \pm j\frac{1}{\sqrt{LC}}$$

Generating –ve Resistance





$$-\frac{I_X}{C_1 s} + V_X = \left(I_X + I_X \frac{g_m}{C_1 s}\right)\frac{1}{C_2 s}$$

$$\frac{V_X}{I_X}(s) = \frac{1}{C_1 s} + \frac{1}{C_2 s} + \frac{g_m}{C_1 C_2 s^2}$$

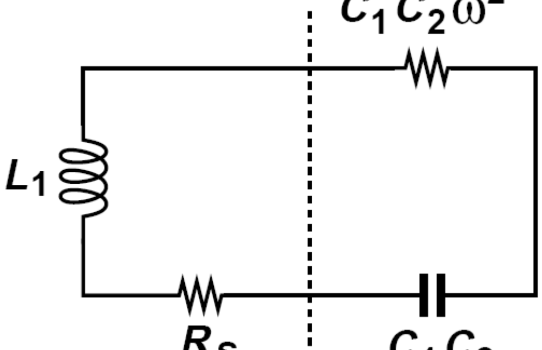
$$\frac{V_X}{I_X}(j\omega) = \frac{1}{jC_1\omega} + \frac{1}{jC_2\omega} - \frac{g_m}{C_1 C_2 \omega^2}$$

- **The negative resistance varies with frequency.**

Connecting Inductor to –ve Res. Ckt

$$R_S = \frac{g_m}{C_1 C_2 \omega^2}$$

$$\omega_{osc} = \frac{1}{\sqrt{L_1 \frac{C_1 C_2}{C_1 + C_2}}}$$



$$R_p = R_s\left(1 + \left(\frac{\omega L_1}{R_s}\right)^2\right) \approx \frac{(\omega L_1)^2}{R_s}$$

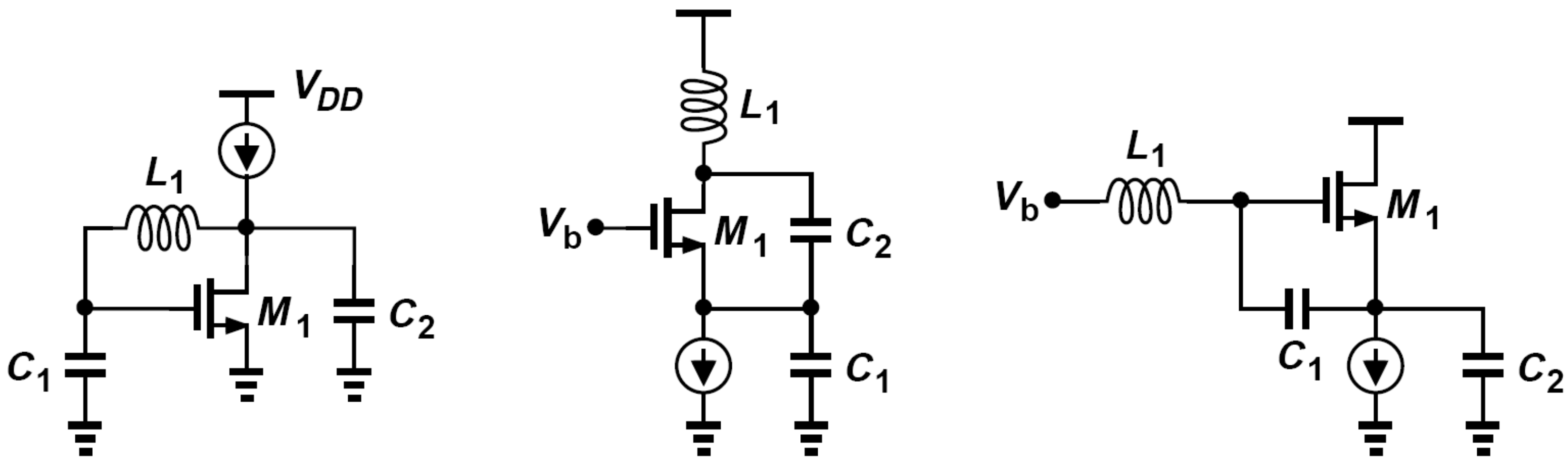
$$\Rightarrow \frac{L_1^2 \omega^2}{R_p} = \frac{g_m}{C_1 C_2 \omega^2}$$

The startup condition:

$$g_m R_p = \frac{(C_1 + C_2)^2}{C_1 C_2} = \frac{C_1}{C_2} + \frac{C_2}{C_1} + 2$$

Three-Point Oscillators

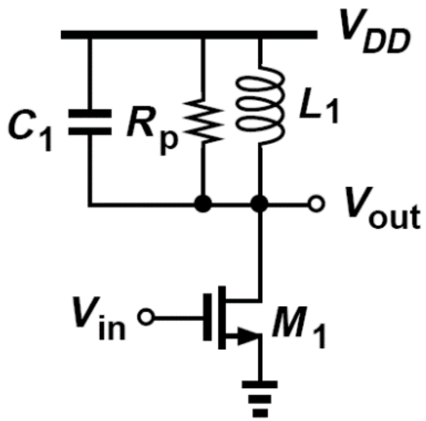
AC ground each terminal → 3 different oscillator topologies.

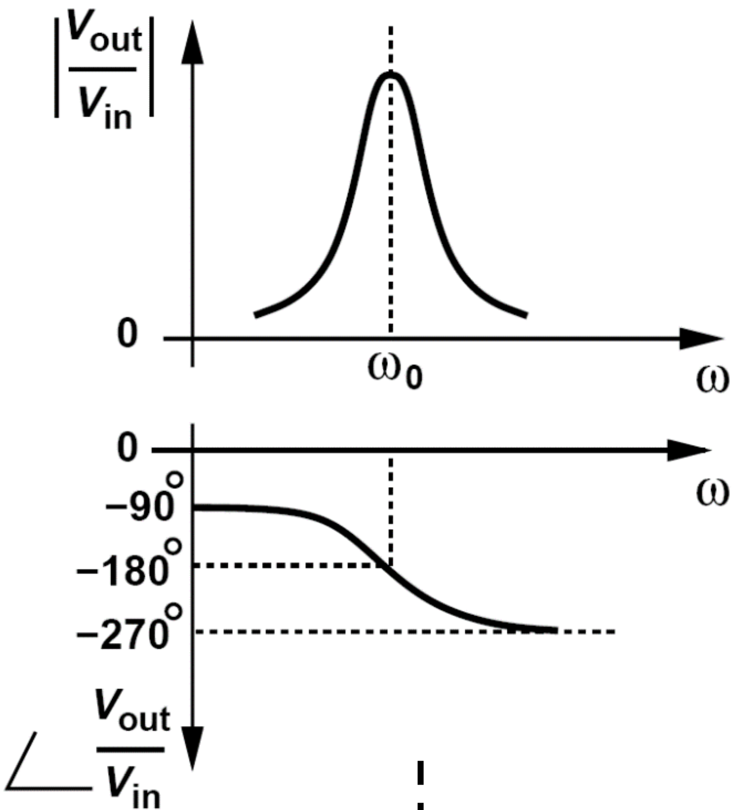


If $C_1 = C_2$, startup condition dictates $g_m R_p \geq 4$

- **Higher power consumption compared to cross-coupled LC VCOs.**

Tuned Amplifier





At very low frequencies

$$\frac{V_{out}}{V_{in}} \approx -g_m L_1 s$$

$|V_{out}/V_{in}|$ → 0

$\angle(V_{out}/V_{in})$ → -90°

At ω_0

$$\frac{V_{out}}{V_{in}} = -g_m R_p$$

$\angle(V_{out}/V_{in})$ = 180°

At very high frequencies

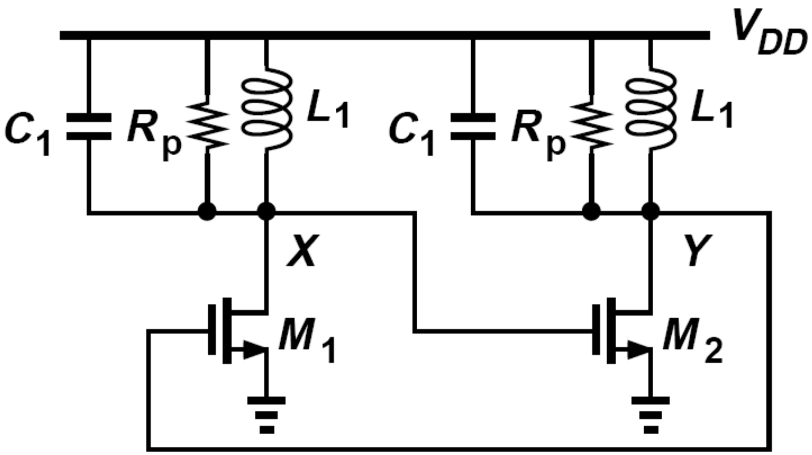
$$\frac{V_{out}}{V_{in}} \approx -g_m \frac{1}{C_1 s}$$

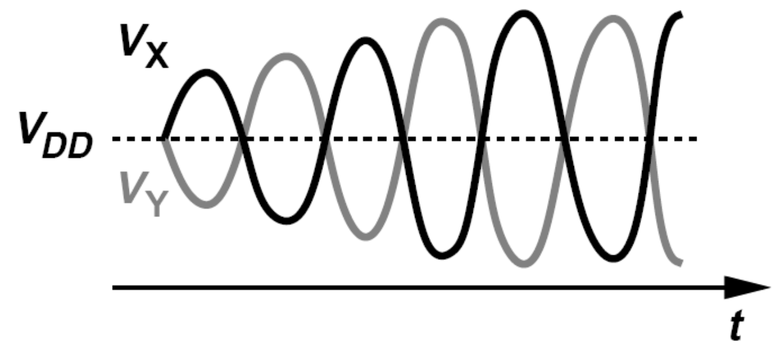
$|V_{out}/V_{in}|$ →0

$\angle(V_{out}/V_{in})$ → +90°

Cascaded Tuned Amp with Feedback

Cascade two phase shifts of 180 ° to get 360 ° around the loop.

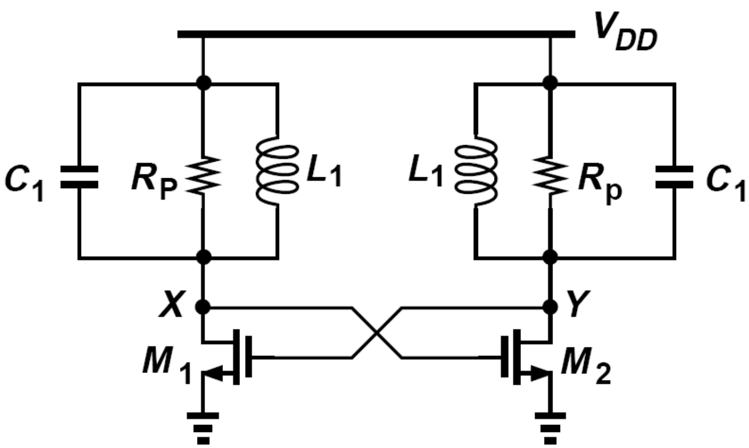


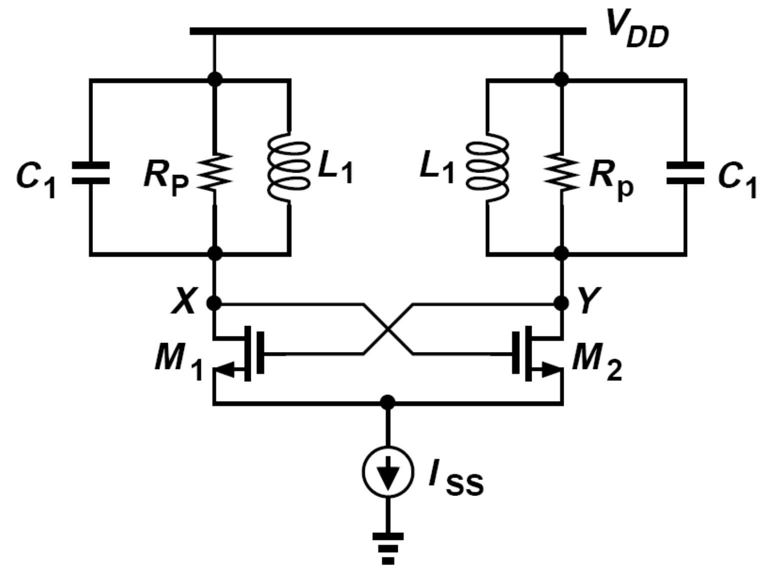


$$(g_m R_p)^2 \geq 1$$

- **Inductive loads → peak voltages above the supply.**
- **The growth of V_X and V_Y ceases when M_1 and M_2 enter the triode region for part of the period, reducing the loop gain.**

Cross-Coupled Oscillator



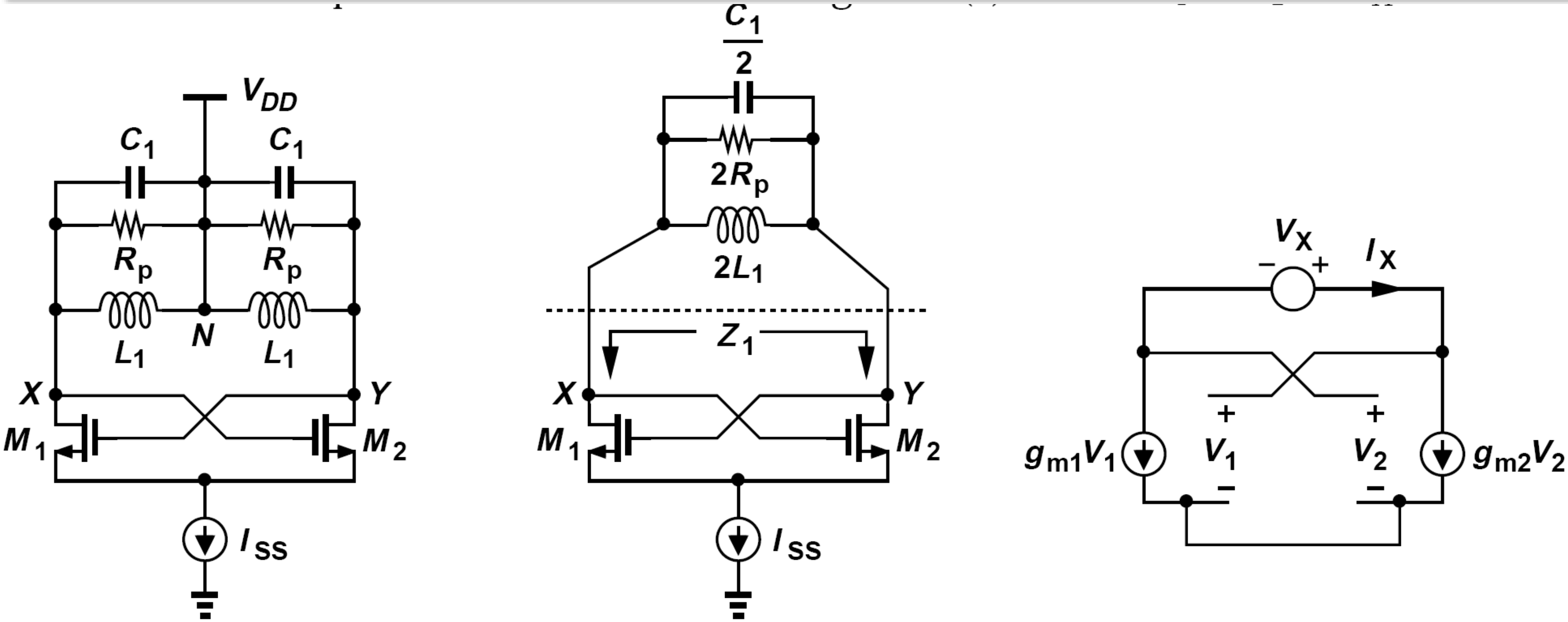


$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_{GS2} + C_{DB1} + 4C_{GD} + C_1)}}$$

Tail current source defines a bias current → more robust and can be viewed as an inductively-loaded differential pair with positive feedback. If M_1 and M_2 experience complete current switching with abrupt edges, peak differential o/p swing

$$V_{XY} \approx \frac{4}{\pi} I_{SS} R_p$$

CC Oscillator: One-Port View



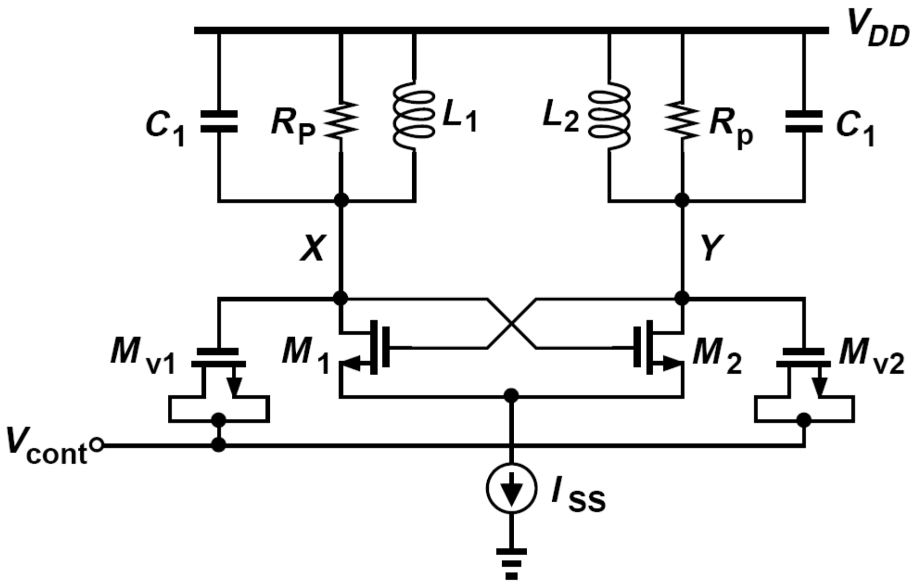
$$I_X = -g_{m1}V_1 = g_{m2}V_2 \quad \Rightarrow \quad \frac{V_X}{I_X} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)$$

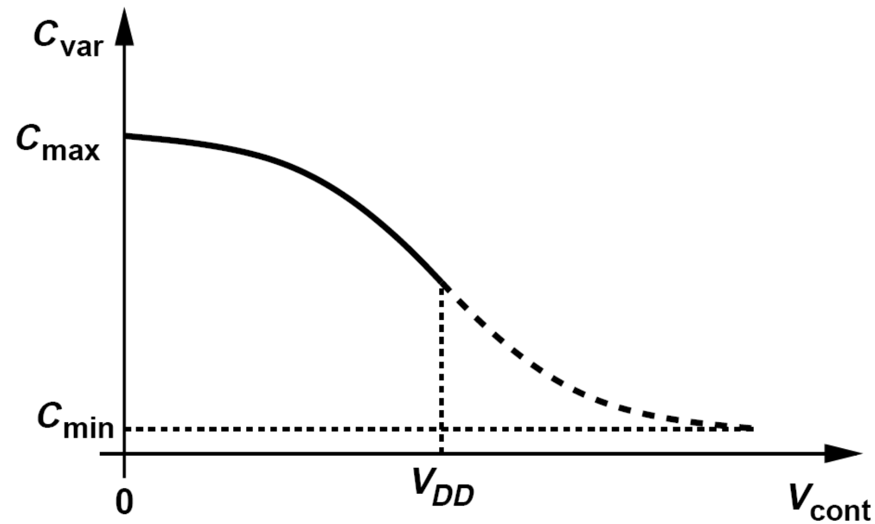
For $g_{m1} = g_{m2} = g_m$ $\quad \dfrac{V_X}{I_X} = -\dfrac{2}{g_m}$

Startup condition: $\quad \dfrac{2}{g_m} \leq 2R_p \quad \Rightarrow \quad g_m R_p \geq 1$

CC-VCO Using MOS Varactors

- Changing cap easier than inductor for VCO
- MOS varactors are more commonly used than *pn* junctions, especially in low-voltage design.



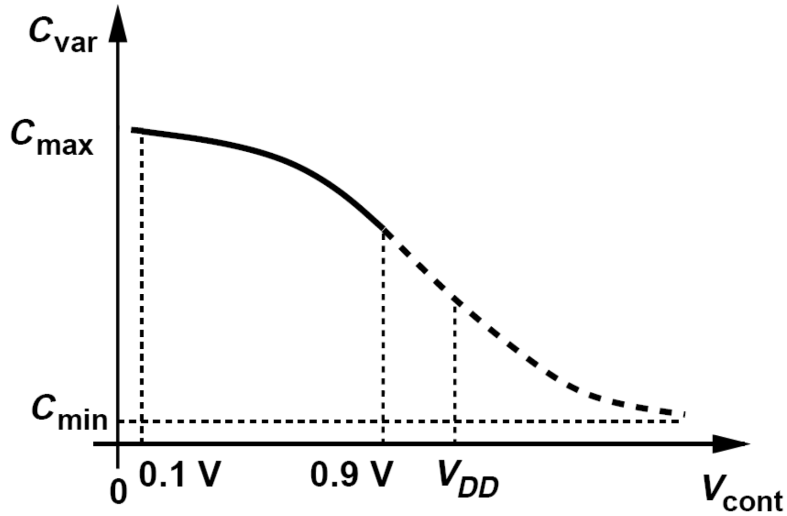


$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{var})}}$$

- Varactors are stressed for part of the period if V_{cont} is near ground and V_X (or V_Y) rises significantly above V_{DD}.
- Only about half of C_{max} - C_{min} is utilized in the tuning.

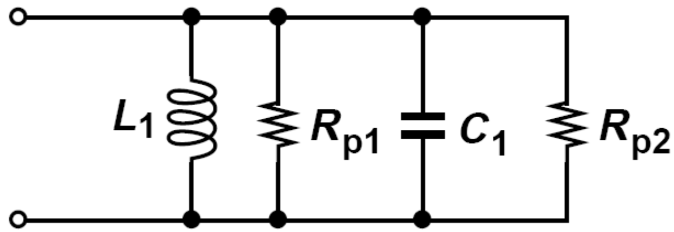
Tuning Range Limitations

- The tuning range trades with the overall tank *Q*.
- Another limitation on C_{var2} - C_{var1} arises from the available range for the control voltage of the oscillator, V_{cont}.



Effect of Varactor's Finite Q:

$$Q_L = \frac{R_{p1}}{L_1\omega}$$
$$Q_C = R_{p2}C_1\omega$$



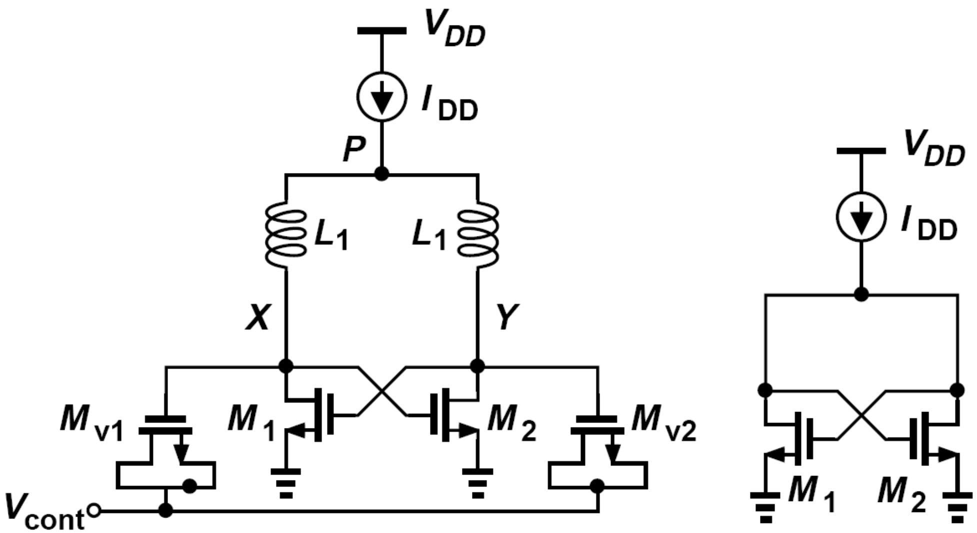
Merging R_{p1} and R_{p2} yields the overall Q:

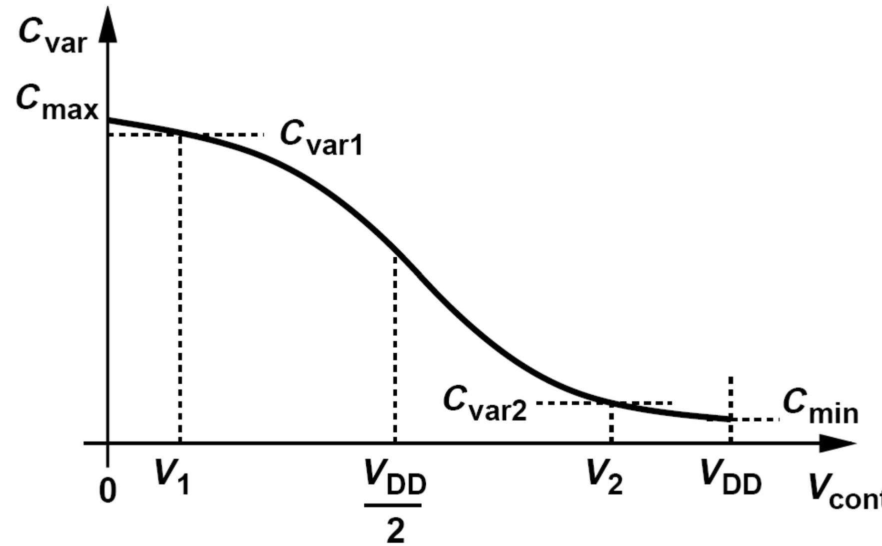
$$\begin{aligned} Q_{tot} &= \frac{R_{p1}R_{p2}}{R_{p1}+R_{p2}} \cdot \frac{1}{L_1\omega} \\ &= \frac{1}{\frac{L_1\omega}{R_{p1}} + \frac{L_1\omega}{R_{p2}}} \\ &= \frac{1}{\frac{L_1\omega}{R_{p1}} + \frac{1}{R_{p2}C_1\omega}}. \end{aligned}$$

$$\Rightarrow \quad \frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

LC VCOs with Wide Tuning Range

- **Allowing both positive and negative (average) voltages across the varactors → utilizing almost the entire range from C_{min} to C_{max}.**



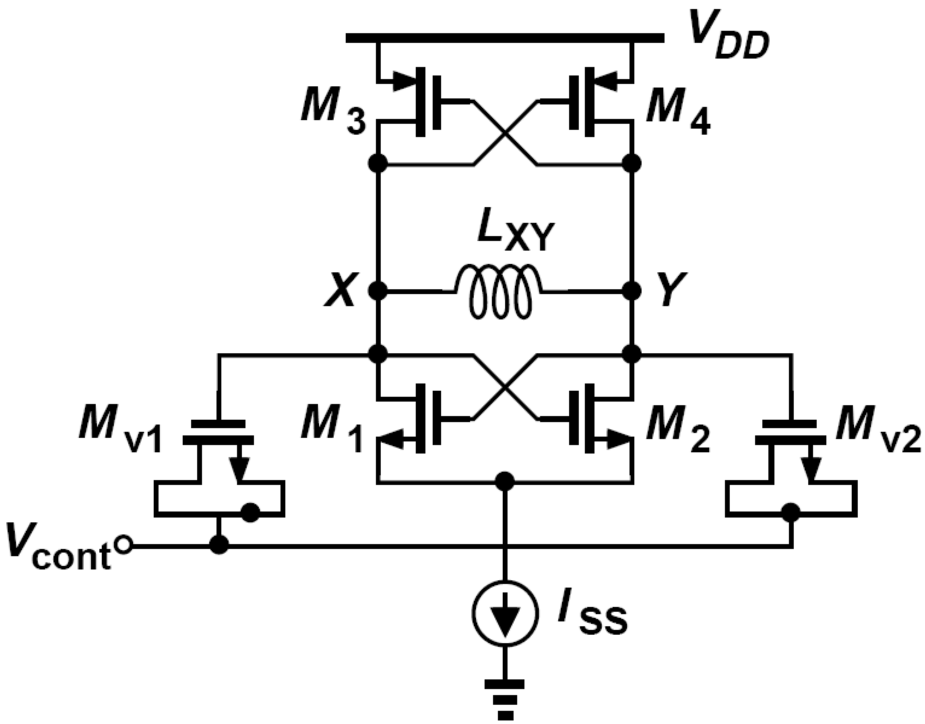


CM = V_{GS} of a diode-connected transistor carrying a current of $I_{DD}/2$.

$$V_{GS1,2} = \sqrt{\frac{I_{DD}}{\mu_n C_{ox}(W/L)}} + V_{TH}$$

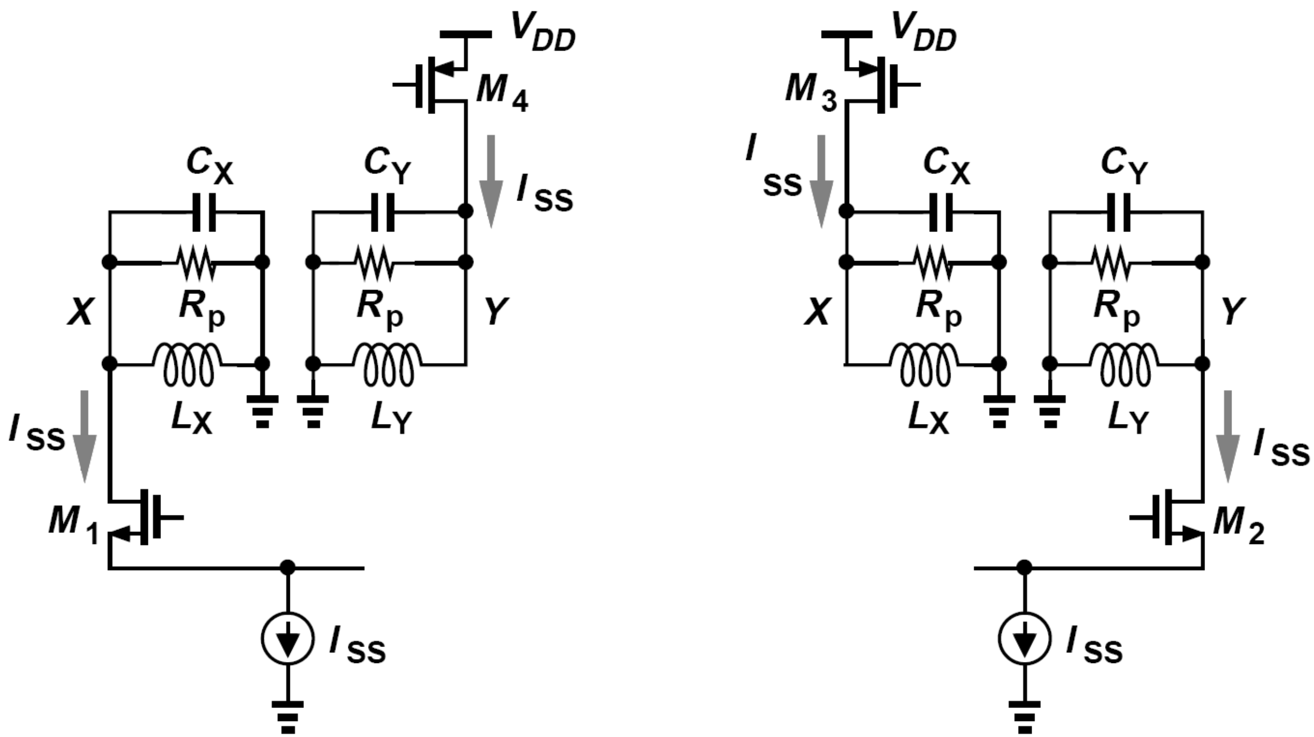
Select W/L for CM = $V_{DD}/2$.
→ As V_{cont} varies from 0 to V_{DD}, $V_{GS,var}$ goes from $+V_{DD}/2$ to $-V_{DD}/2$

Complimentary Cross-Coupled VCO



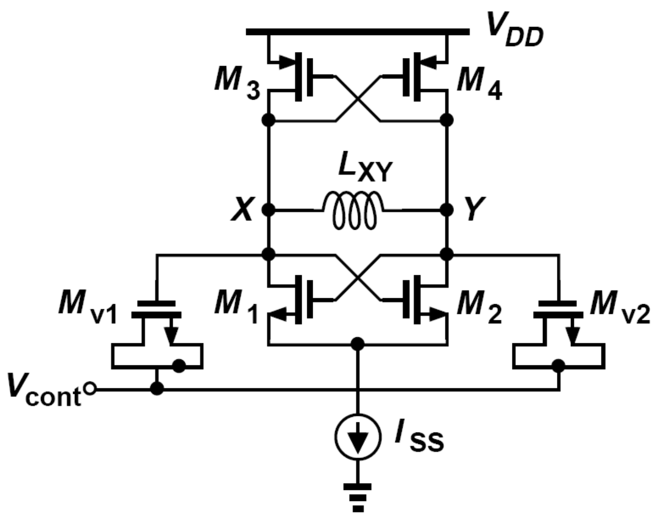
- A cross-coupled NMOS pair and a cross-coupled PMOS pair sharing the same bias current.
- Choose W/L and I_{SS} for CM = V_{DD}/2 at *X* and *Y* → maximizing the tuning range.

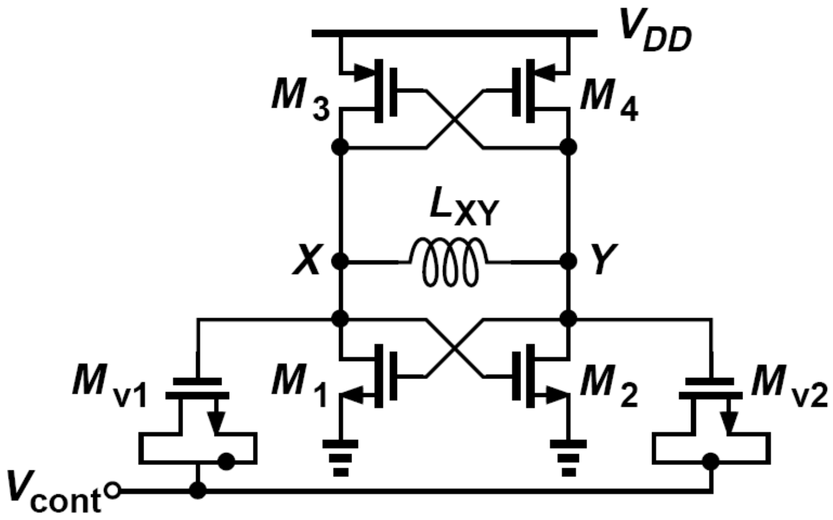
CCC-VCO: Voltage Swing



- The current in each tank swings between $+I_{SS}$ and $-I_{SS}$ whereas in previous topologies it swings between I_{SS} and zero.
- The output voltage swing is therefore doubled.

CCC-VCO: Headroom, Tuning Range



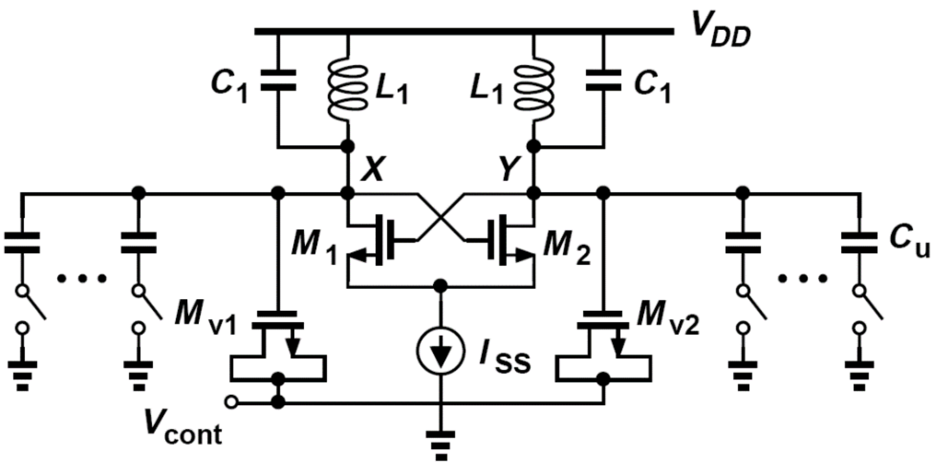


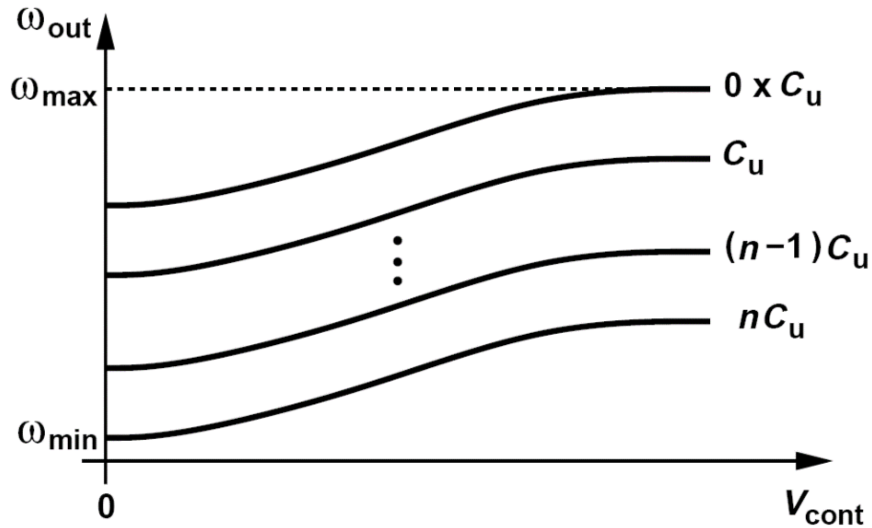
- $|V_{GS3}|+V_{GS1}+V_{ISS} = V_{DD}$ → Wide PMOS, degrading the tuning range.
- Noise of the bias current source modulates the output CM level and hence the capacitance of the varactors, producing frequency and phase noise.
- Remove the tail current source?
  - Supply noise sensitivity increases
  - Bias current varies with PT.

Eg.: A volt. regulator providing V_{DD} may exhibit significant flicker noise, thus modulating the frequency (by modulating the CM level).

Discrete Tuning

- **Add "discrete tuning" to achieve a capacitance range well beyond C_{max}/C_{min} of varactors.**





Lowest frequency : all unit capacitors switched in and max varactor value,

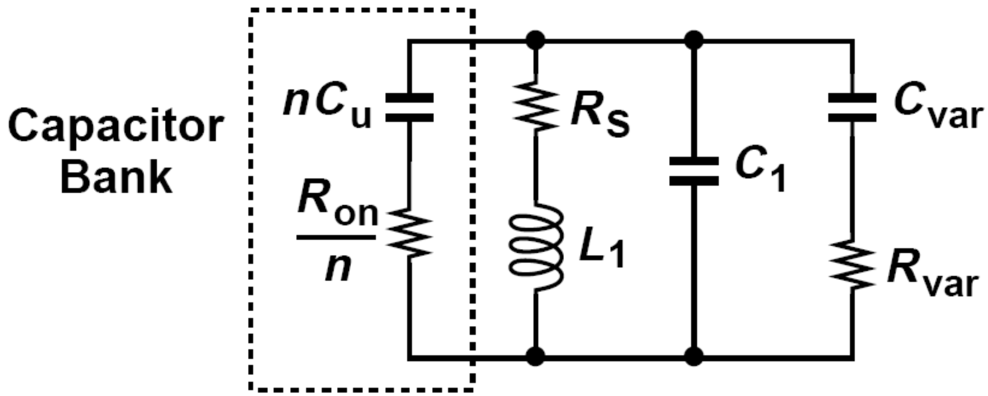
$$\omega_{min} = \frac{1}{\sqrt{L_1(C_1 + C_{max} + nC_u)}}$$

Highest frequency : all unit capacitors switched out and min varactor value,

$$\omega_{max} = \frac{1}{\sqrt{L_1(C_1 + C_{min})}}$$

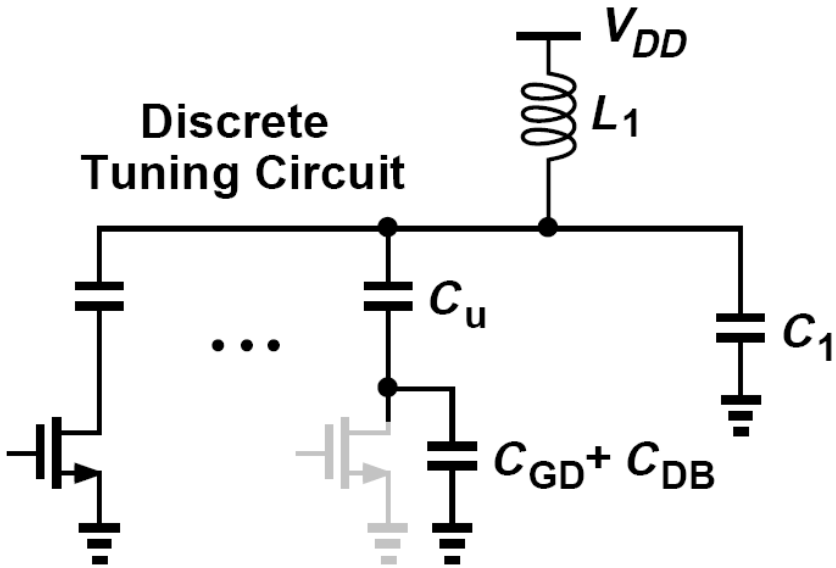
Discrete Tuning: R_{on} degrades Q

- R_{on} of the switches that control the unit caps degrades the tank-Q.



- Increase the width of the switch transistors to minimize R_{on}?

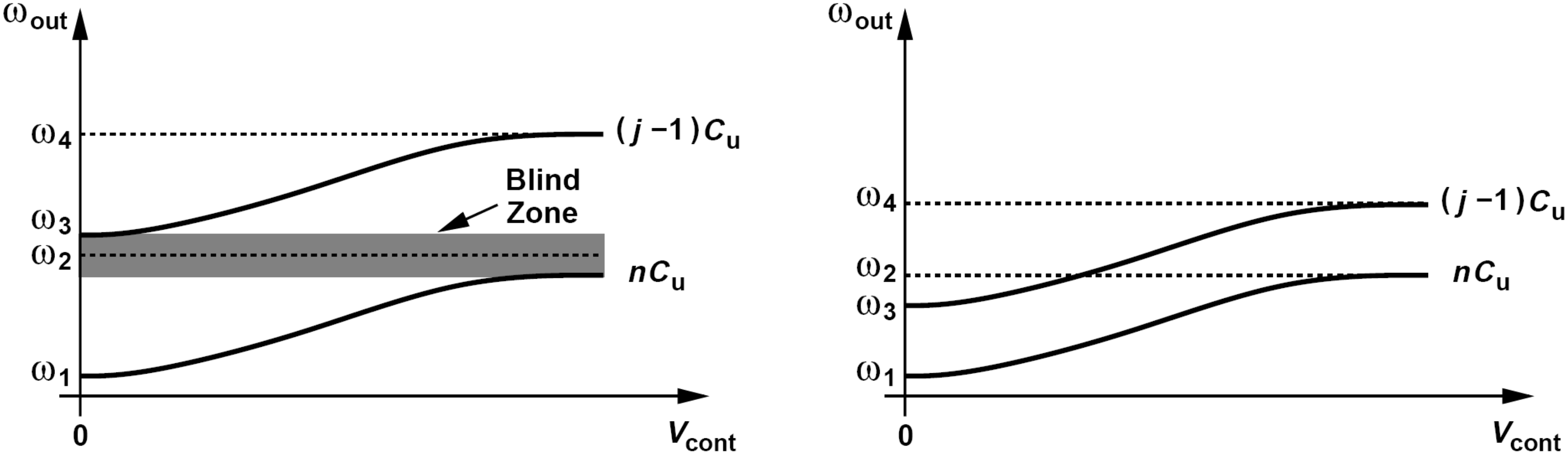
Discrete Tuning: Switch Parasitic Cap



- Wider switches → larger bottom plate cap for the unit capacitors to ground → substantial cap to the tank when the switches are off.
- R_{on}xC_{off} is usually constant for a given technology.
- Trade-off between the *Q* and FTR

F. Cararra et al., "A 2.4-GHz 24-dBm SOI CMOS Power Amplifier With Fully Integrated Reconfigurable Output Matching Network," *Tran. MTT*, Sep. 2009.

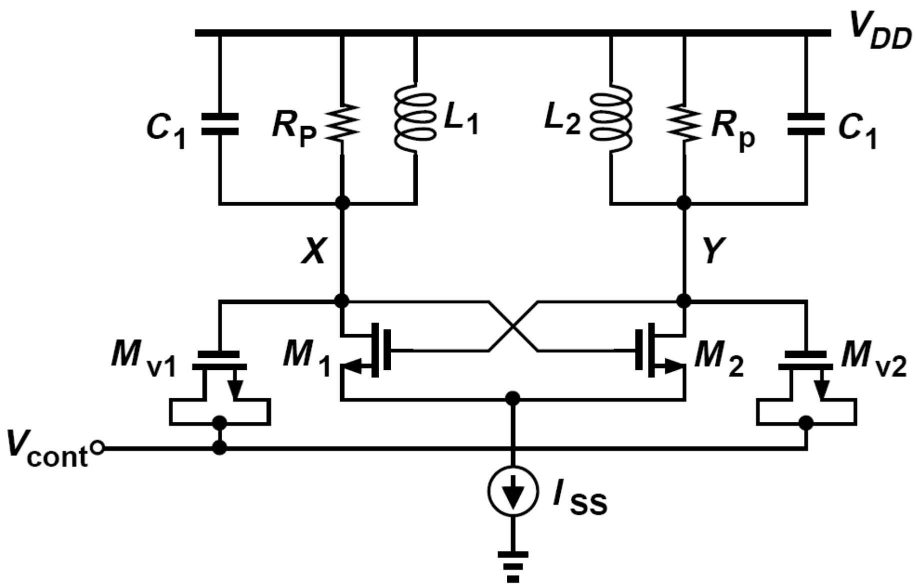
Discrete Tuning: Blind Zone

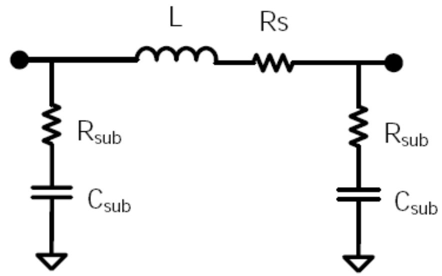


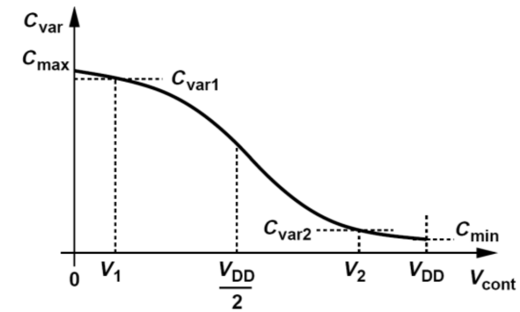
The oscillator fails to cover the range between ω_2 and ω_3 for any combination of fine and coarse controls.

- **To avoid blind zones, each two consecutive tuning characteristics must have some overlap.**
- **→ Smaller C_u and larger *n* → complex layout.**

VCO Design Procedure – I







What are the given constraints? What is desired? Which topology to choose? For a given center frequency ω_0, load capacitance C_L, and

- **FTR, phase noise, minimize power consumption**
- **FTR, power budget, minimize phase noise**
- **power budget, phase noise, maximize FTR**

VCO Design Procedure – II

- Find the inductor with max Q at ω_0. [Select the smallest L that yields a parallel resistance of R_p at ω_0]
- With Q and R_p known, find I_{SS} from the phase noise specification. Or, based on the power budget and hence the maximum allowable I_{SS}, select the R_p so as to obtain the required differential voltage peak swing, $(4/\pi)I_{SS}R_p$.

$$S(\Delta\omega) = \frac{\pi^2}{R_p}\frac{kT}{I_{SS}^2}\left(\frac{3}{8}\gamma + 1\right)\frac{\omega_0^2}{4Q^2\Delta\omega^2}$$

- Assuming a startup factor of 2, calculate the g_m of the cc-transistors.
- From g_m and I_{SS}, determine the dimensions of cc-transistors. Ensure that they experience nearly complete switching with the given voltage swings.
- Calculate $C_{var,max}$, that can be added to reach the lower end of the FTR, ω_{min}

$$\frac{1}{\sqrt{L_0(C_{GS} + 4C_{GD} + C_{DB} + C_p + C_L + C_{var,max})}}$$

- Using proper varactor models, determine $C_{var,min}$, and compute the upper end of the FTR, ω_{max} $\frac{1}{\sqrt{L_0(C_{GS} + 4C_{GD} + C_{DB} + C_p + C_L + C_{var,min})}}$
- If ω_{max} is quite higher than necessary, increase $C_{var,max}$ to center the FTR around ω_0.