Project #1(2)
Due March 4th, 11:30am – **No Exceptions (no late submissions). Upload to Canvas.**

Design, Analysis and Simulation of a CMOS Low Noise Amplifier

This assignment is 30% of your total grade. You will design, analyze and simulate a fully-integrated CMOS LNA with the following design specifications:
Center Frequency, f_C: 5.25GHz,
$|S_{11}| < -10$dB @ f_C and +/-100MHz
$|S_{22}| < -10$dB @ f_C and +/-100MHz
$|S_{12}| < -30$dB @ f_C and +/-100MHz
$|S_{21}| > 15$dB @ f_C and +/-100MHz
NF < 2.2dB and +/-100MHz
IIP3 > -7dBm
Load capacitance (from next stage): 50fF
Minimize the power consumption. VDD = 1.0V
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Notes for the project:
• Reports should be typed. Incorporate figures into the document, not added as appendices. Clearly label all figures with the appropriate axis labels and units and ensure that the plots are clearly visible.
• Use the Single-column Word template supplied on the class website. You do not need to type in equations – you can incorporate a scanned image of hand-calculations, provided they are easily legible.
• Use the 45nm PDK models.
• You are allowed one DC current source and multiple DC voltage sources (for cascode biasing, etc). Otherwise the amplifier must consist of capacitors, resistors, inductors, and transistors.
• The maximum transistor W or L is 700 μm.
• The body of all NMOS transistors should be tied to ground. You have the freedom to tie the body of PMOS transistors anywhere.
• Design for single-ended Rin of 50Ω.
• For IIP3 simulations, use two tones separated by 1MHz. Choose the extrapolation point carefully.
• The induced gate noise has not been modeled and you can ignore it for this project.
• If you fail to meet a particular specification, and give a proper justification, you may still get full marks.

Project grades will be calculated with the following weights:

Meeting Project Specifications	40
Hand Analysis and Calculations	20
Clarity of Report (see deliverables below)	25
Optimization of Power Consumption	15
Total	100

Meeting Project Specifications:
Please include a table listing the specifications and your simulated results.
Project deliverables:
• Complete amplifier schematic on a white background (not the default Cadence black background). [5]
• Table of the operating points of all transistors (gm, W/L, Vds, Vdsat, etc). [5]
• | S11 | | S12 |, |S21| |S22| plots of the amplifier [5]
• Plot showing PIIP3 performance. [5]
• Plot of NF vs. Frequency for LNA [5]
• Any other plots you find useful in demonstrating that your amplifier meets all specifications.
• Cited works.
Hand Analysis and Calculations:
Please include the first pass values of different components and describe how you calculated them. List the assumptions you made.
Optimization of Power Consumption:
Describe how you reduced the power consumption while meeting all the specifications. If you could not meet a certain specification, please justify the final design. Describe different design decisions, tradeoffs, how you optimized your variable, etc.