Project #2(2)
Due April 6th, 10AM – **No Exceptions (no late submissions). Upload to Canvas.**

Design, Analysis and Simulation of a Voltage Controlled Oscillator

This assignment is 30% of your total grade. You will design, analyze and simulate a fully-integrated fully-differential CMOS VCO.

Design specifications:
Center Frequency, f_0: 5.25GHz,
Tuning Range > 10%.
Phase noise: -111dBc/Hz@600kHz offset, -118dBc/Hz@1MHz offset from the nominal center frequency of 5.25GHz.
Minimize the power consumption. VDD = 1.2V
C_L (Constant) > 80fF (representing the load looking into the LO buffer or Mixer)
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Notes for the project:
• Reports should be typed. Incorporate figures into the document, not added as appendices. Clearly label all figures with the appropriate axis labels and units and ensure that the plots are clearly visible.
• Use the Single-column Word template supplied on the class website. You do not need to type in equations – you can incorporate a scanned image of hand-calculations, provided they are easily legible.
• Use the 45nm PDK VDD = 1V transistor models.
• You are allowed one DC current source and multiple DC voltage sources (for cascode biasing, etc).
Otherwise the amplifier must consist of capacitors, resistors, inductors, and transistors.
• The maximum transistor W or L is 700 μm.
• The body of all NMOS transistors should be tied to ground. You have the freedom to tie the body of PMOS transistors anywhere.
• If you fail to meet a particular specification, and give a proper justification, you may still get full marks.

Project grades will be calculated with the following weights:

Meeting Project Specifications	37
Hand Analysis and Calculations	20
Clarity of Report (see deliverables below)	28
Optimization of Power Consumption	15
Total	100

Meeting Project Specifications:
Please include a table listing the specifications and your simulated results.

Project deliverables:

• Complete VCO schematic on a white background (not the default Cadence black background). [4]
• Table of the DC operating points of all transistors (gm, W/L, Vds and Vdsat if applicable, etc), VCO output amplitude, value of R's, C's and L's you have used. [4]
• @5.25GHz, phase-noise plot swept from10kHz to 20MHz. [4]
• Also include a screen capture of the completed PSS noise summary, showing the top 10 contributors to the phase noise at the spot frequency of 1MHz. Be sure to set up the pnoise simulation correctly so that it captures 1/f noise from the devices. [4]
• Plot showing spot phase noise @ 1MHz offset on the y-axis, with frequency of oscillation on the x-axis (f_{0min} , f_0, f_{0max}). Show at least 3 coordinates. [4]
• VCO gain plot: showing frequency of oscillation on the y-axis (f_{0min} to f_{0max}) with the control voltage on the x-axis. Report the VCO gain in V/MHz. Show at least 6 coordinates. [4]
• Plots showing the single-ended and differential output waveforms (transient simulation) @ 5.25GHz. [4]
• Any other plots you find useful in demonstrating that your VCO meets all specifications.
• Cited works.

Hand Analysis and Calculations:

Please include the first pass values of different components and describe how you calculated them. List the assumptions you made.

Optimization of Power Consumption:

Describe how you reduced the power consumption while meeting all the specifications. If you could not meet a certain specification, please justify the final design. Describe different design decisions, tradeoffs, how you optimized a certain variable, etc.