Simulations in Cadence ICFB6

Last updated: 1/23/2018

Sections of this tutorial have icfb5 screenshots. However, the menu options are same in icfb6.

Sudip Shekhar

Originally prepared by Parisa Behnamfar in 2014 for ICFB5

EECE 457/571F RFIC Design Course, University of British Columbia

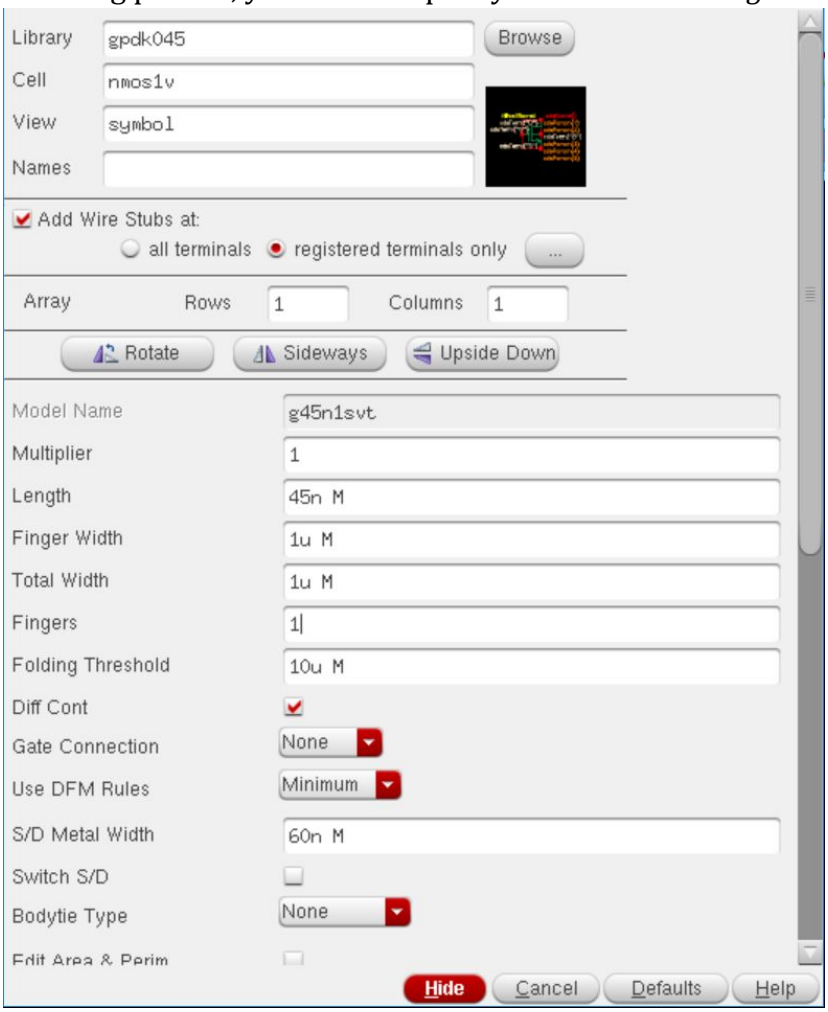
In this tutorial you will learn how to run different simulations in Cadence. This tutorial follows Tutorial 1 where you learnt how to draw a schematic and run an AC simulation.

1. Common-source amplifier schematic

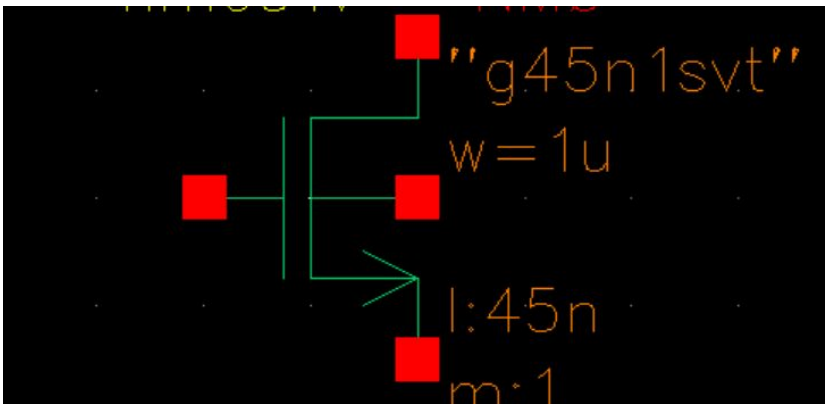
First of all, create another cellview in your project library. We will start by designing a common-source amplifier with a resistive load.

To begin with, you may want to add transistors to the schematic window.

For the CS amplifier, the component you need is *nmos1v* from *gpdk045*. As it highlighted in the following picture, you need to specify the *width* and *length* of the transistor.



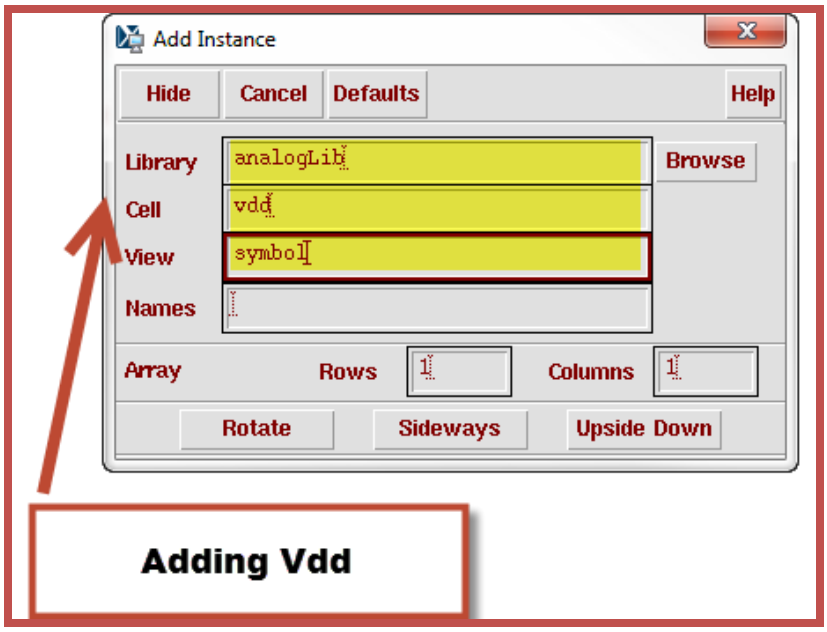
✓ After specifying the above properties then you can put you component in the schematic.



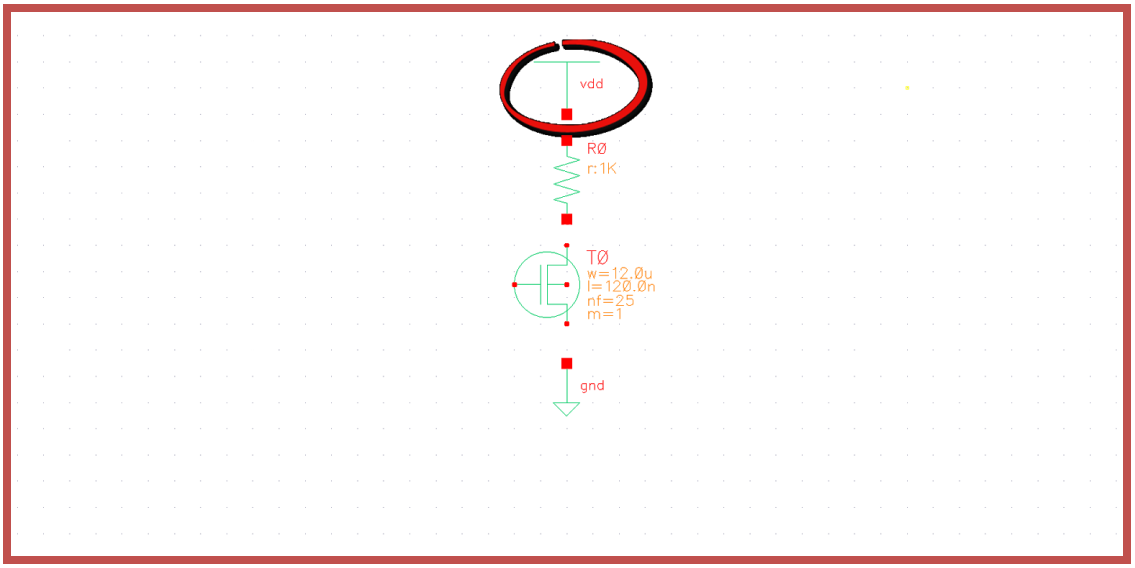
The procedure to instantiate a pmos device is similar to nmos except that you need *pmos_1v* from *gpdk045.*

Next, following the steps of the Tutorial 1, add a resistor (100 Ohms) and connect it to the transistor using a wire. Add gnd to the schematic, and don't forget to connect the bulk of the NMOS to gnd.

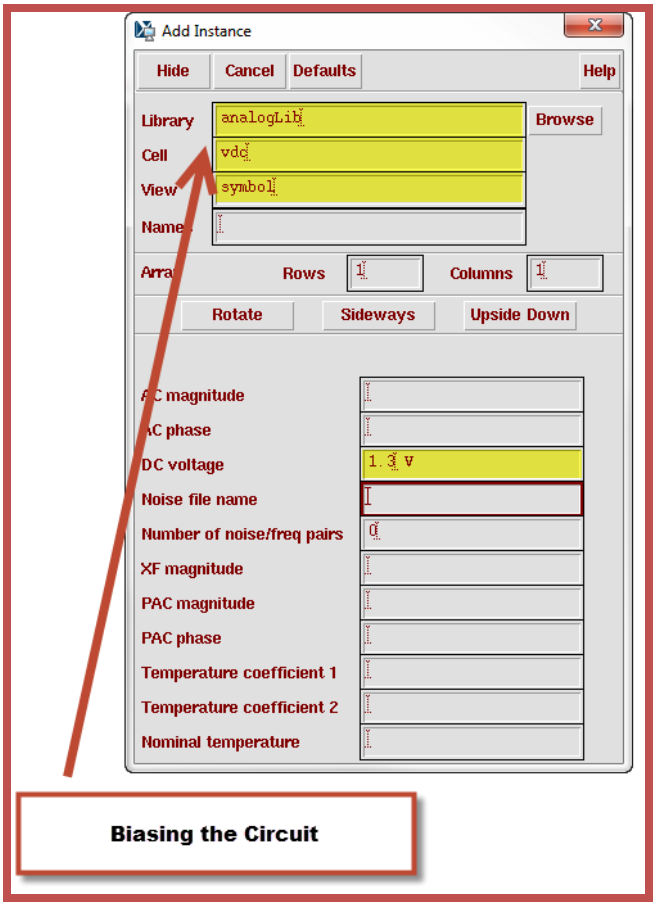
You need to bias your common source and for this purpose we use a component called *vdd* as follow. This component is just a symbolic component and it doesn't have any electrical property; it is used just to make the *vdd* connection easier. This component will give a global name to the net attached to it.



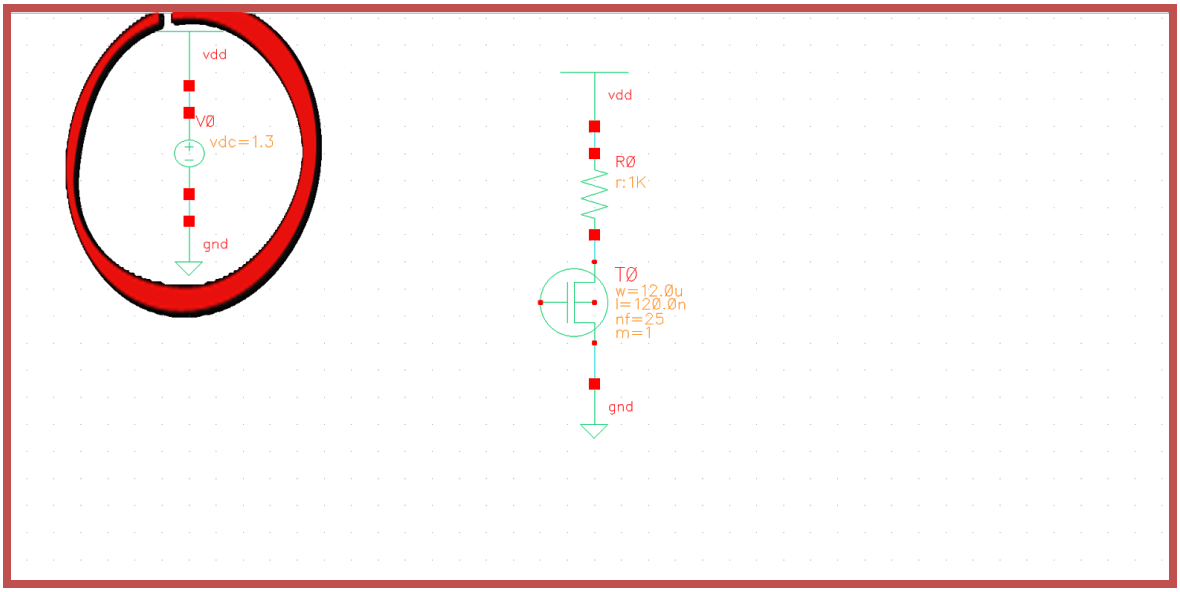
Schematic after adding the vdd symbol:



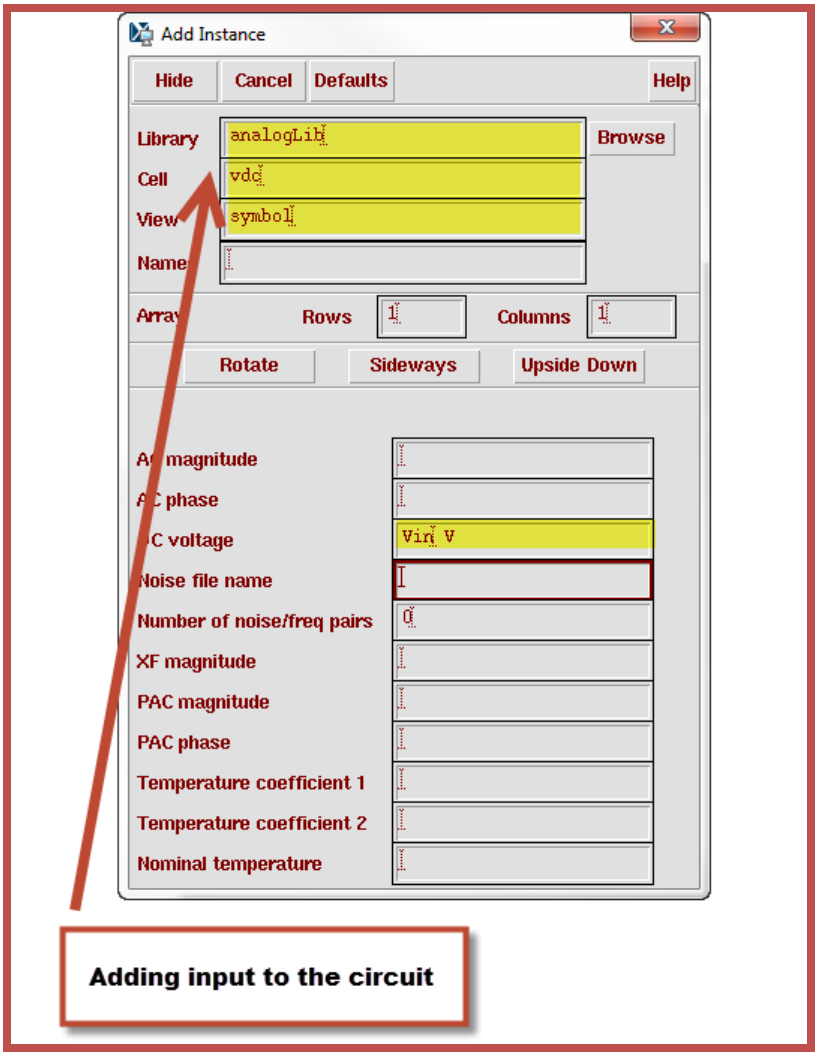
Now you must specify the value of vdd. For this, you will use a dc voltage source (vdc) of 1. 2V.



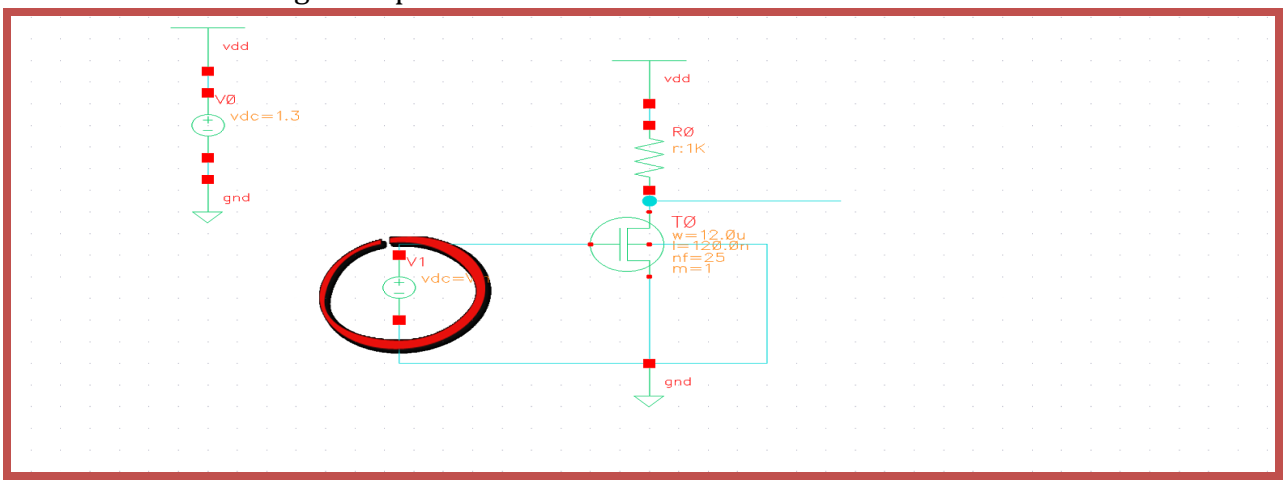
Schematic after adding the final components for biasing:



Now add the input to the circuit; instead of using the exact value for the input, we define it as a variable (Vin), then we can sweep this variable later for our DC analysis or other purposes.



Schematic after adding the input source:



Don’t forget to label the nets that are important for your design because you can find them easily after the simulation in the simulation results.
Don’t forget to check and save your design before any kind of simulation.

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2. Running Simulations

Next, let us see how to run different kinds of simulations:

1. DC Transfer Characteristics
2. DC Operating Points
3. g_m versus Vgs (and how to use the calculator)
4. AC analysis
5. Noise analysis
6. Transient analysis

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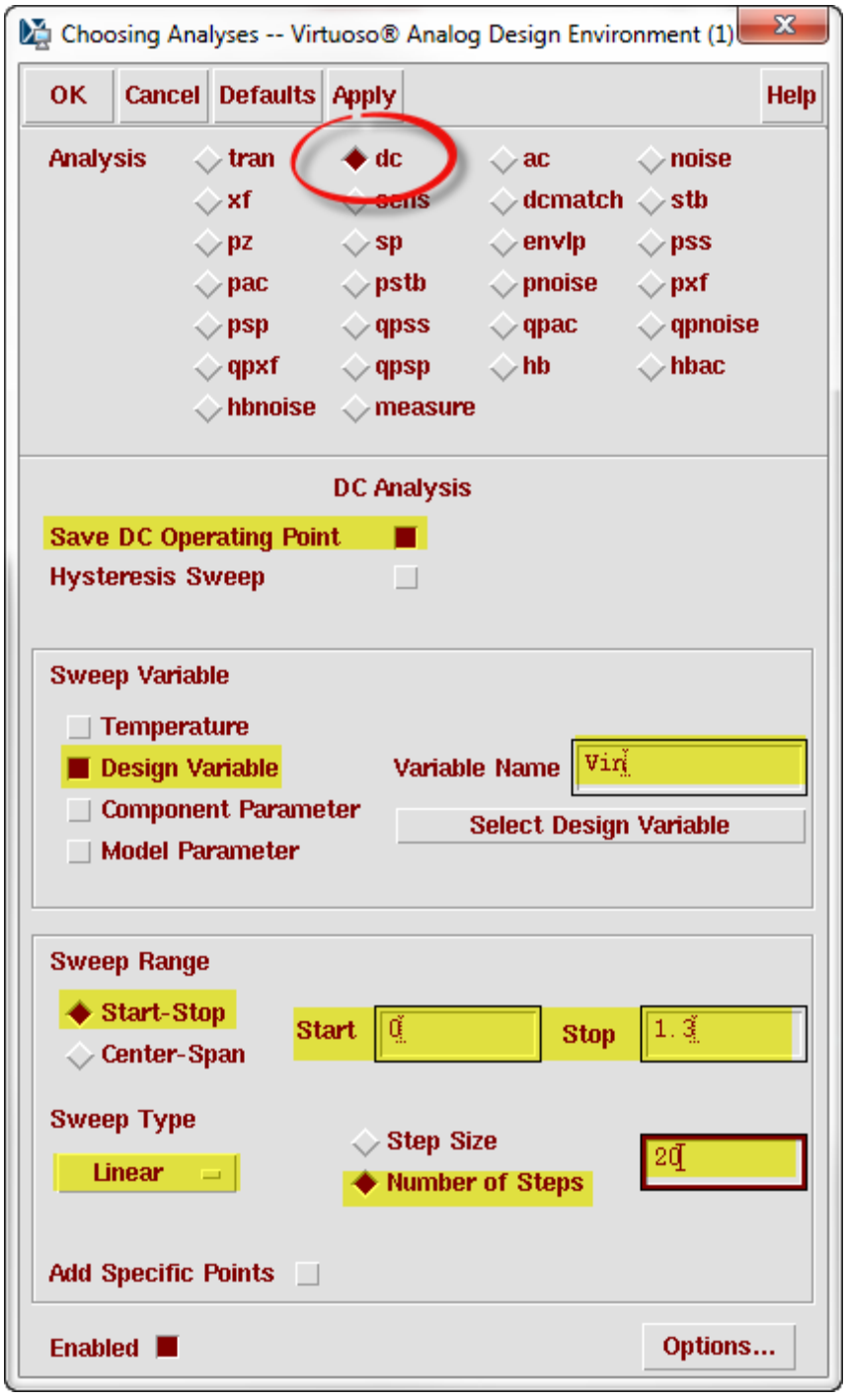
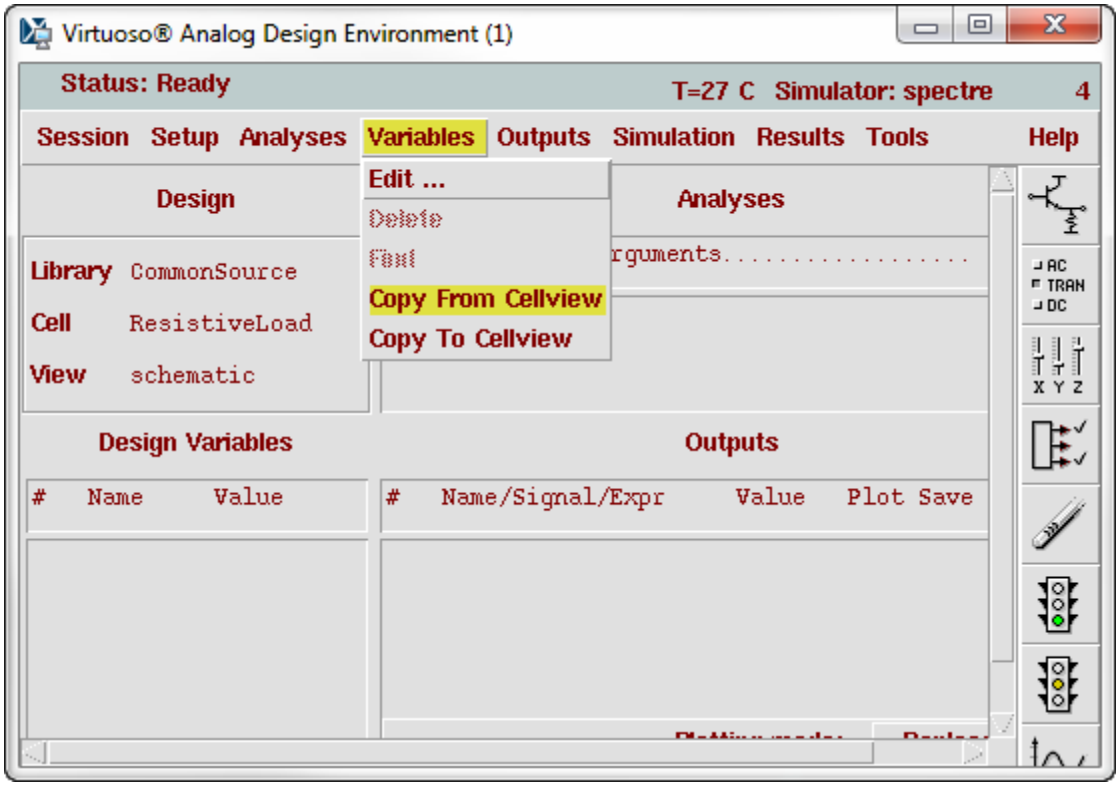
1. DC Transfer Characteristics:

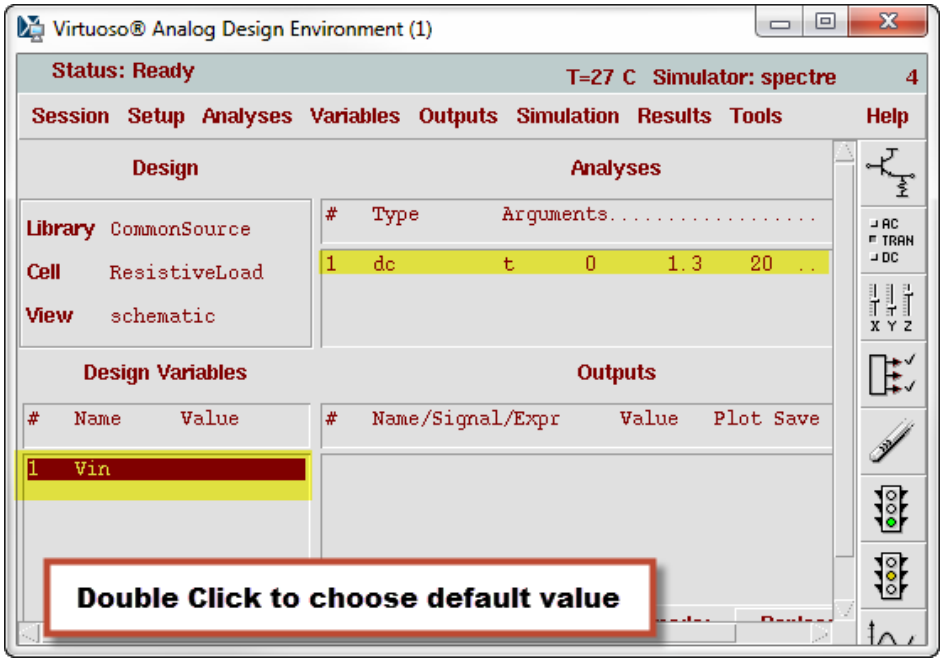
Running the DC sweep to get the DC characteristics of the Common Source amplifier.



Before doing the simulation all the variables should be copied to ADE from the schematic of Cellview; in our case it is just one variable that is “Vin”. To do this, follow the image below:

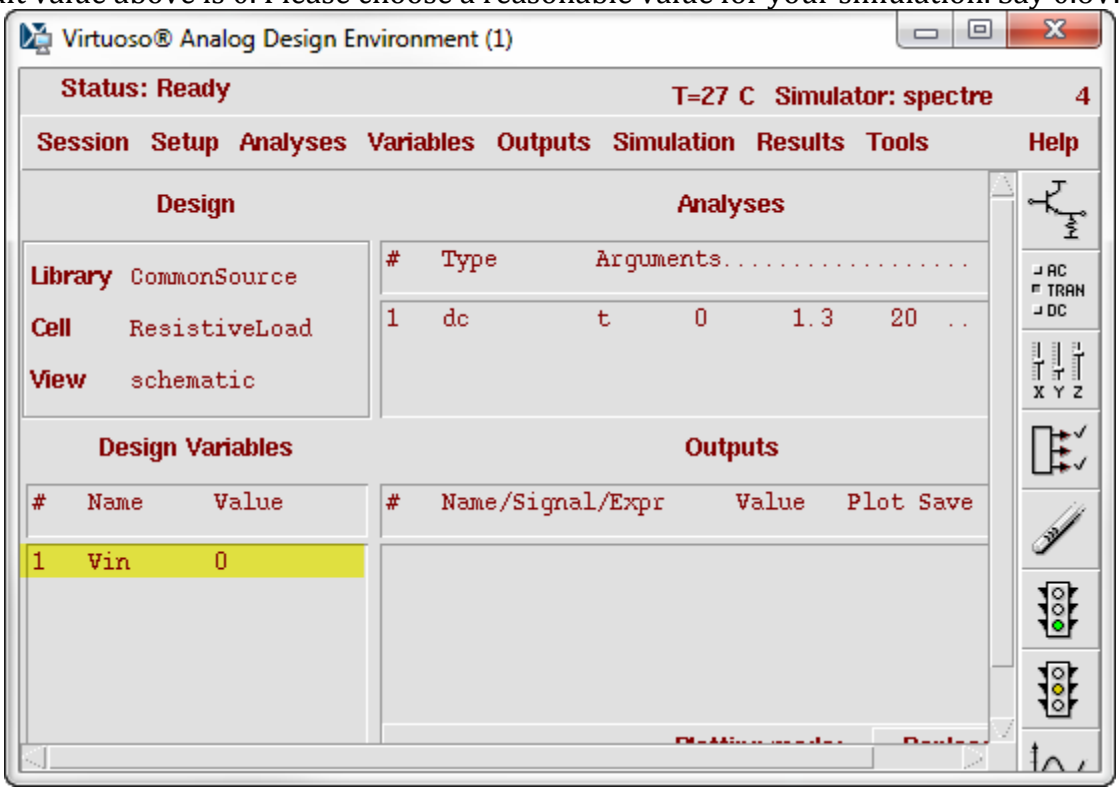


Every variable you copy from the Cellview should have a default value before doing the simulation:

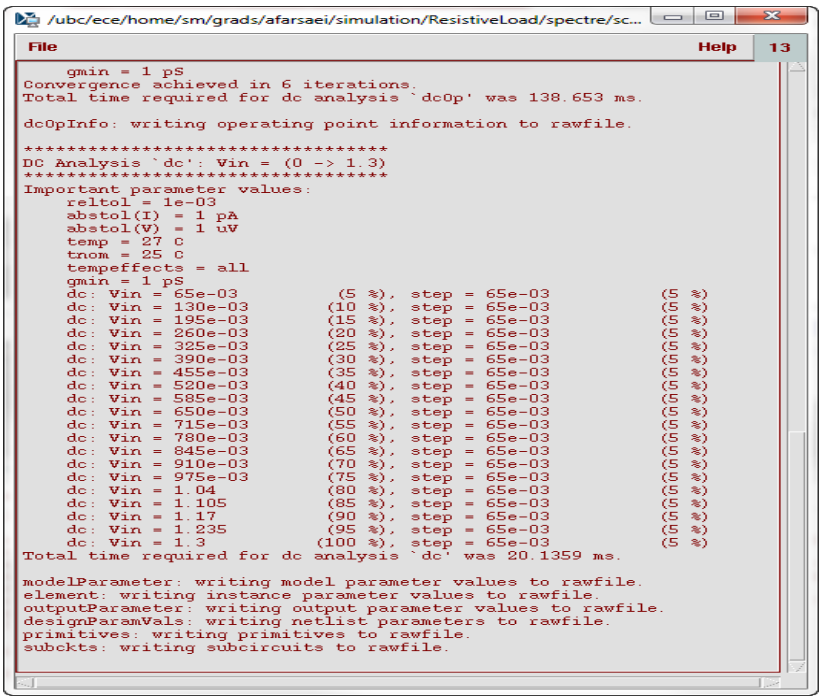


Specify the default value for the Variable “Vin”

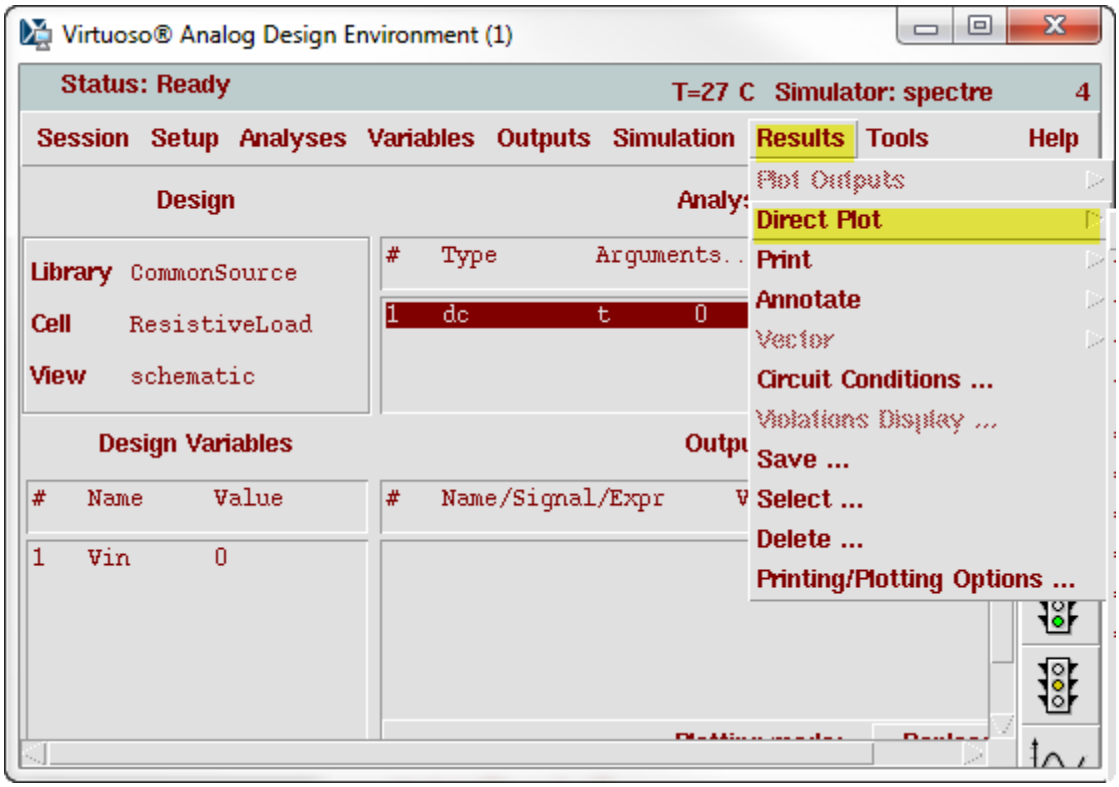
The ADE GUI after setting the default value for variable “Vin”
The default value above is 0. Please choose a reasonable value for your simulation. Say 0.6V.



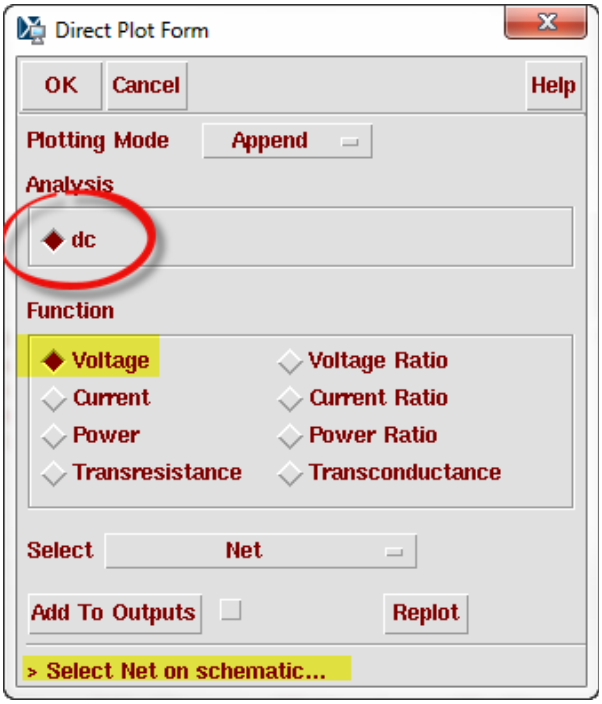
Run the simulation using the “Simulation -> Run”;
Check whether the simulation has been done successfully.



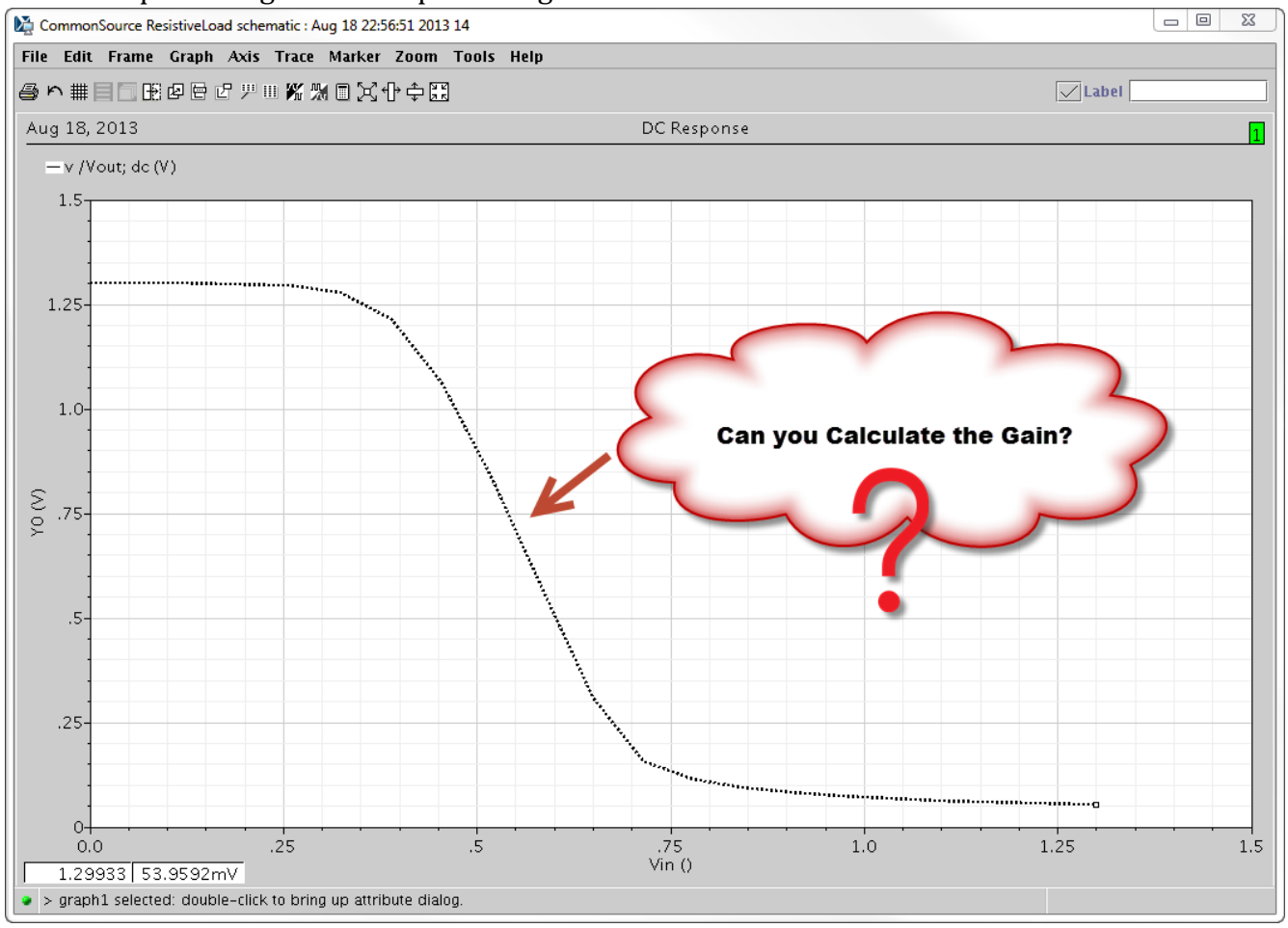
Plot the simulation results (Results -> Direct Plot -> Main Form):



Choose the results you want to see:

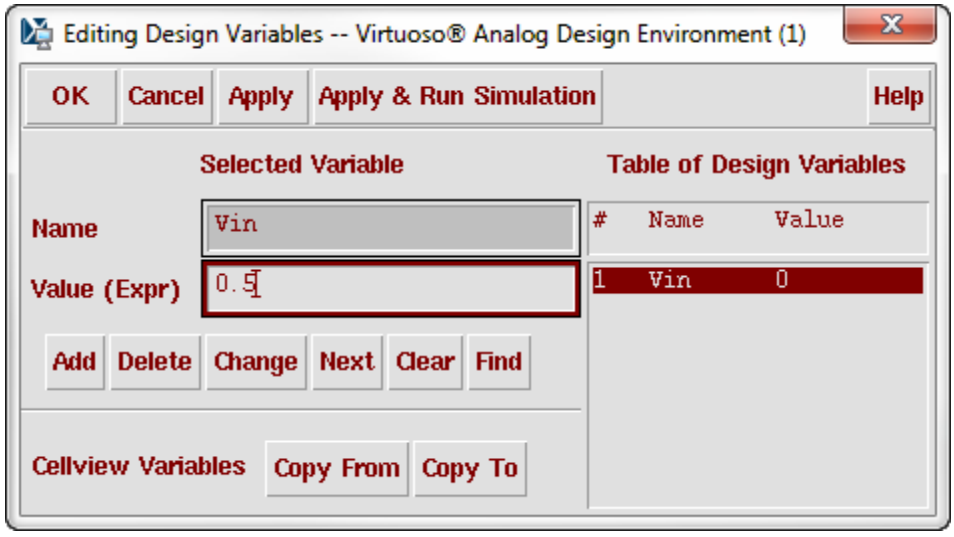


Plot of Output Voltage versus Input Voltage:

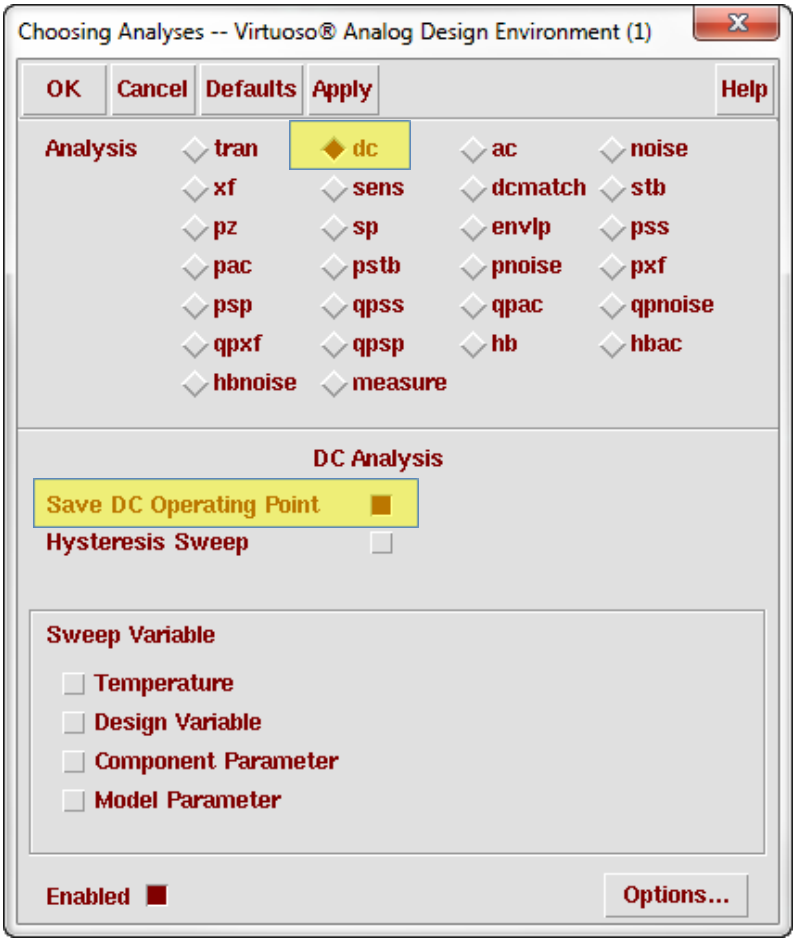


2. DC Operating Points

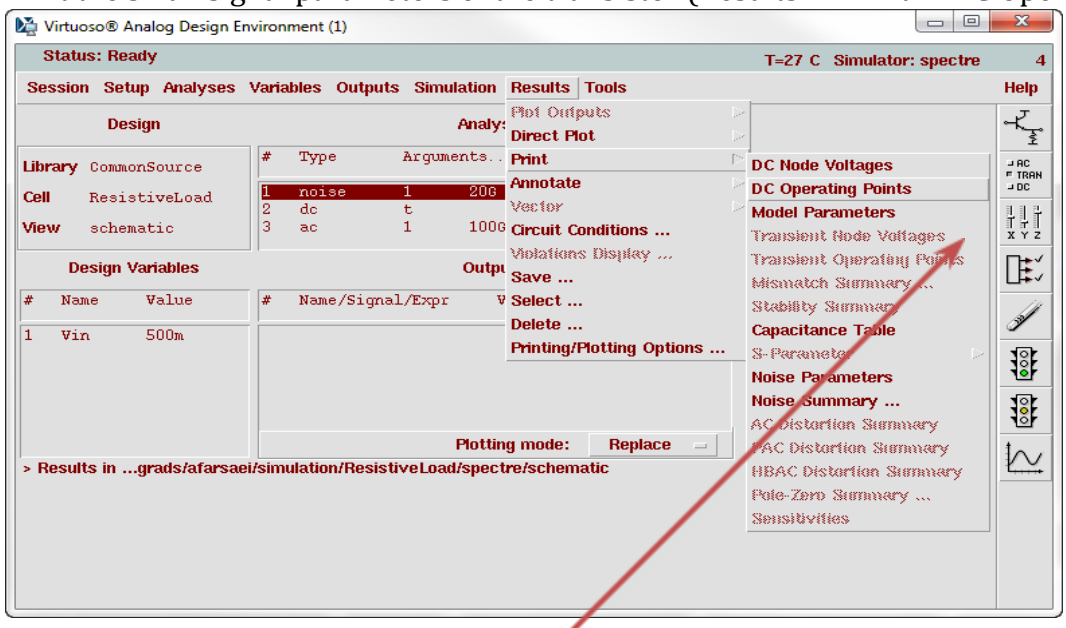
Setup analysis to extract small signal parameters of the transistor. First of all you should specify the DC voltage where you want to extract small signal parameters of the transistor.



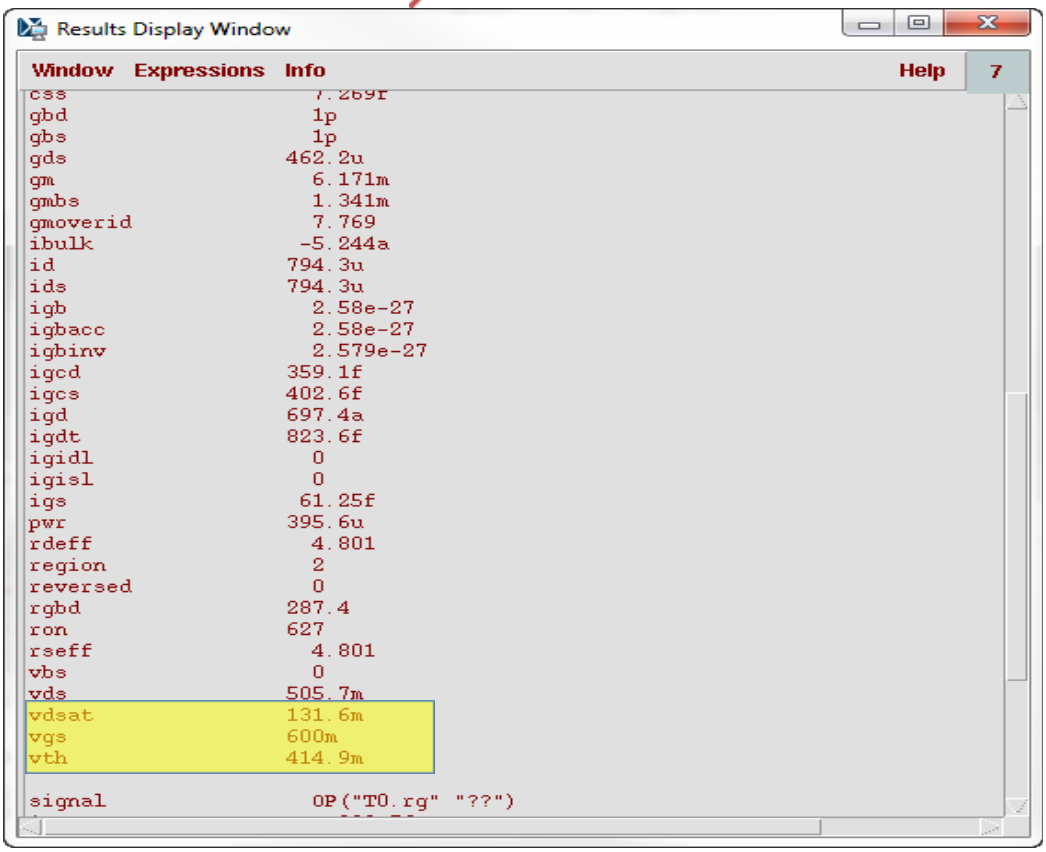
Choose DC analysis as the analysis you want to run (Don't forget to check "Save DC Operating Point"):



Print the small signal parameters of the transistor (Results -> Print -> DC Operating Points):



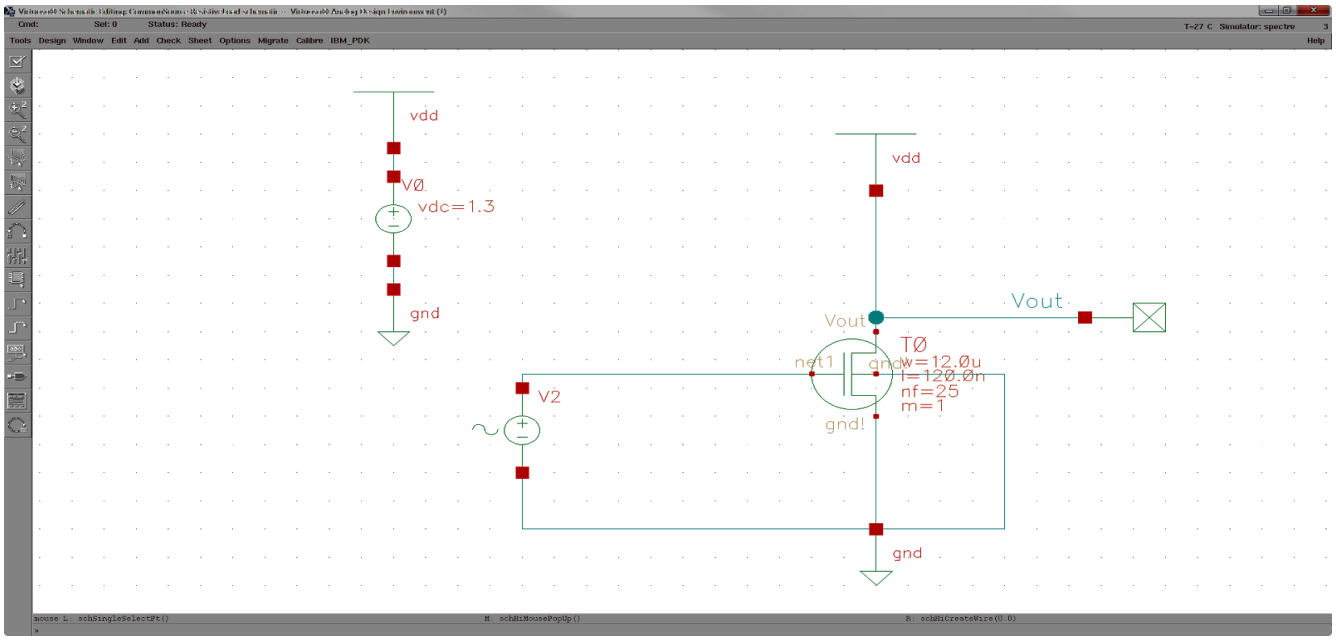
Click the component you want to see the DC operating point for. As an example, for the NMOS,



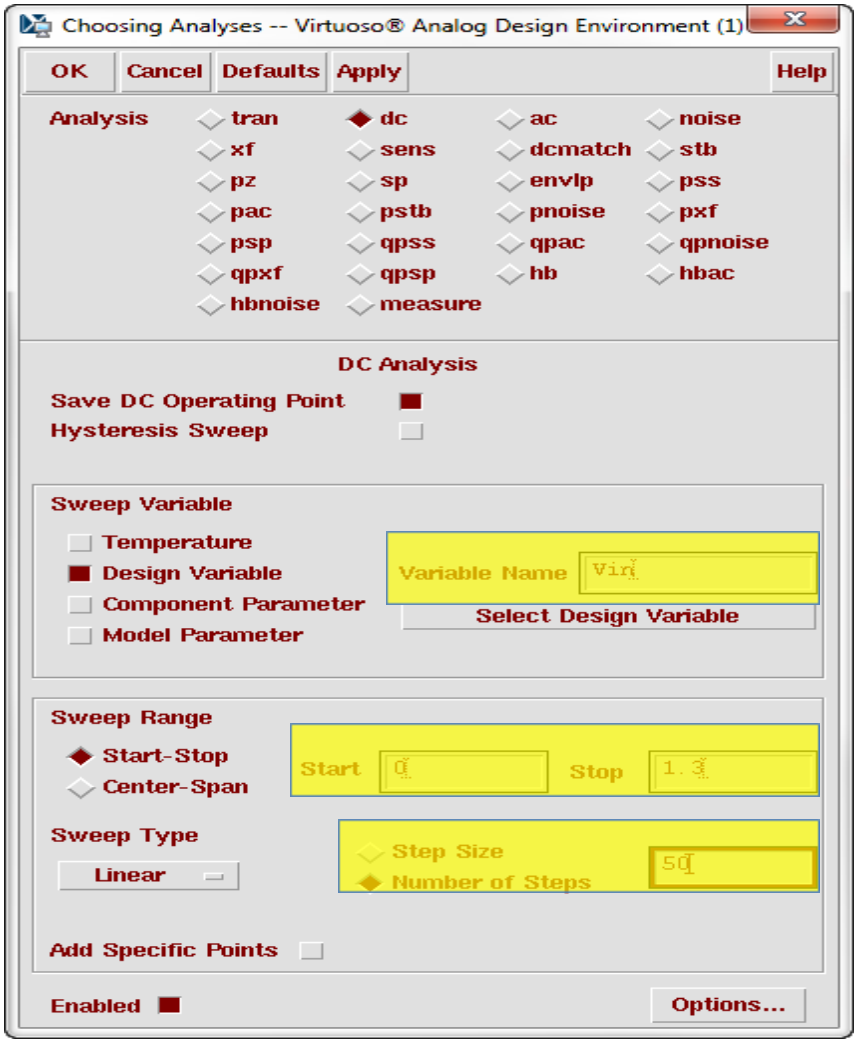
You can also Print DC Node Voltages and they will show up in the schematic window.

3. Plot gm versus Vgs

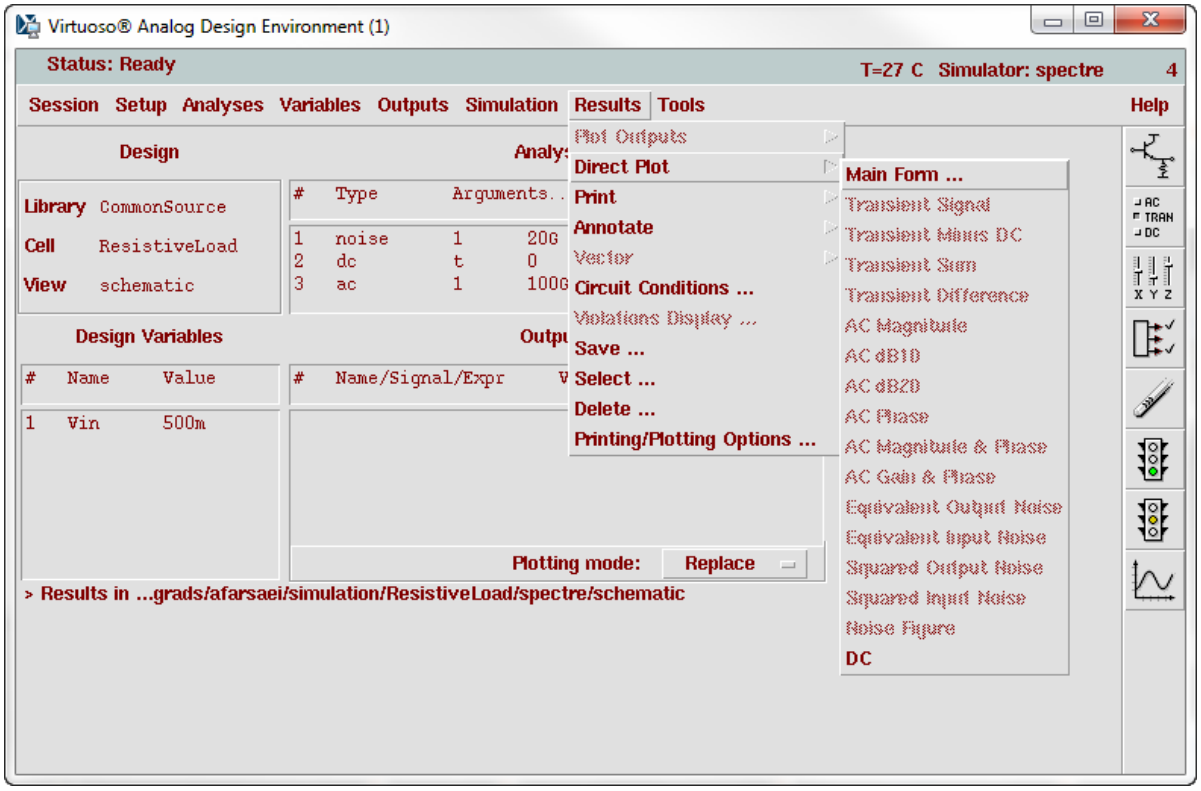
(Change the schematic to be similar to the following schematic):

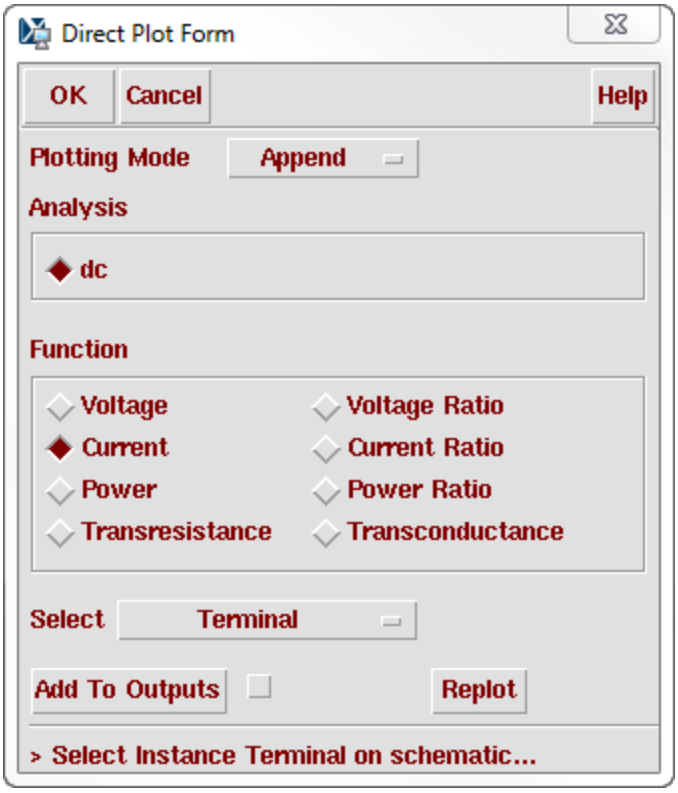


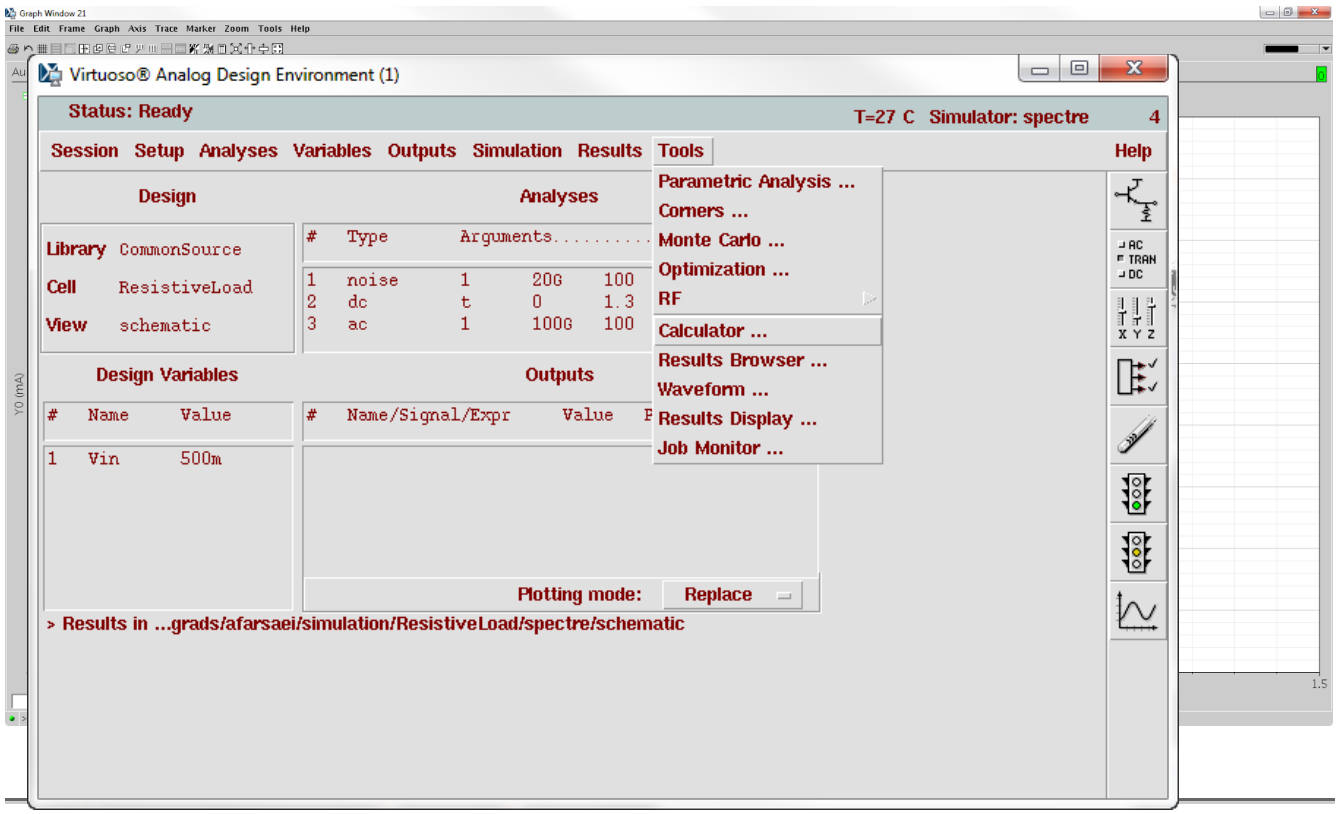
Specify the Analysis:



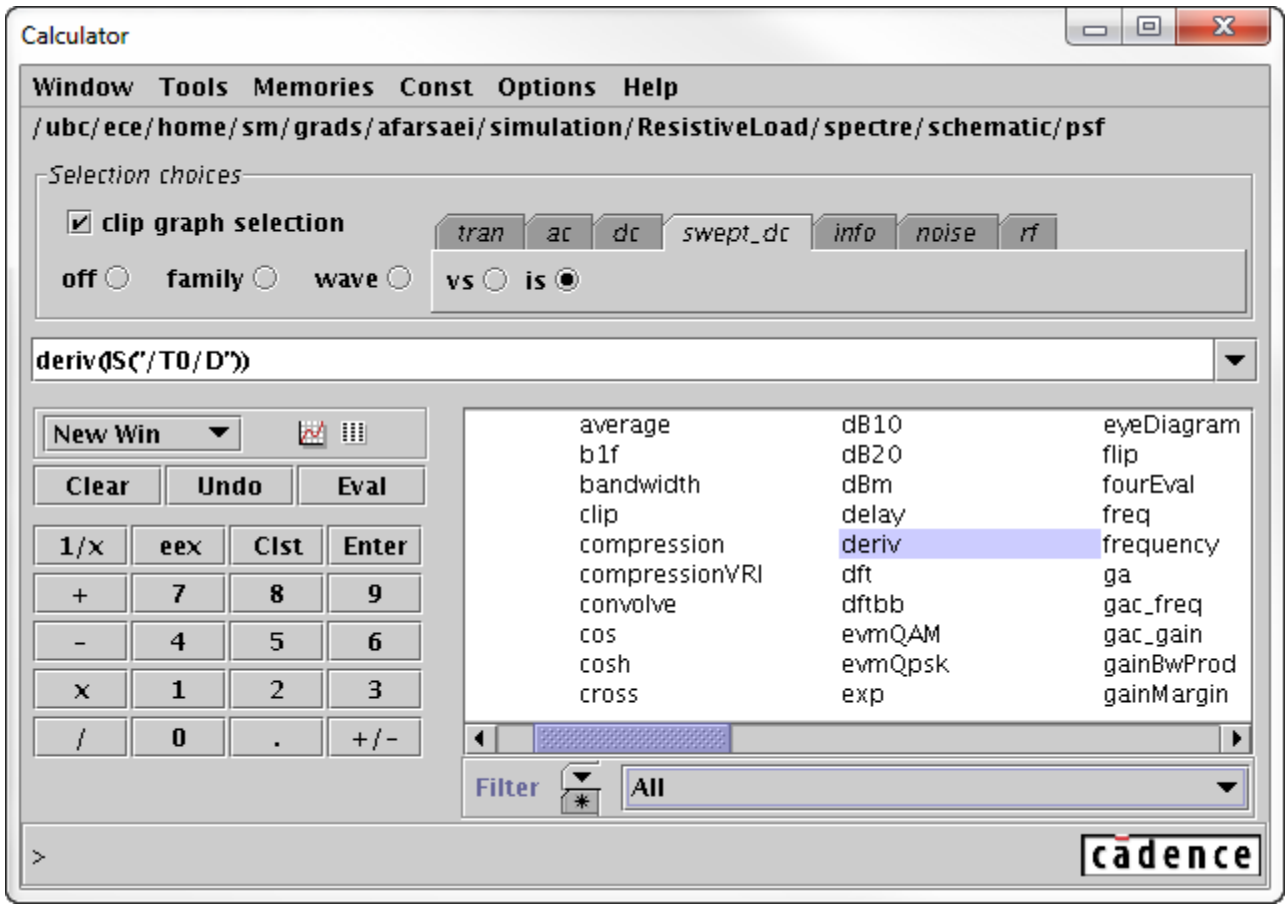
Run the simulation and plot the ID versus Vgs (which is Vin in our design):

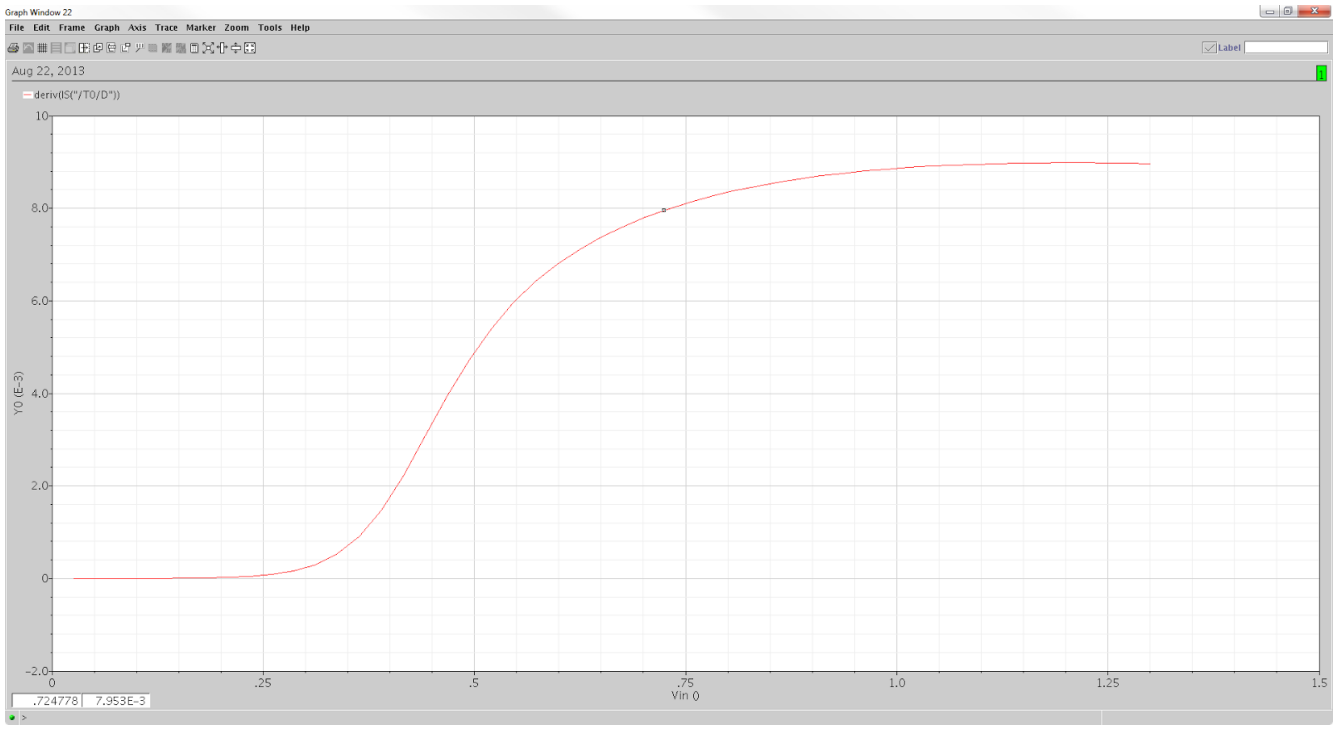

Virtuoso® Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 4
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library CommonSource
Cell ResistiveLoad
View schematic
Type Arguments..
1 noise 1 20G
2 dc t 0
3 ac 1 100G
Design Variables
Name Value
1 Vin 500m
Name/Signal/Expr
Plotting mode: Replace
> Results in ...grads/afarsaei/simulation/ResistiveLoad/spectre/schematic
Plot Outputs
Direct Plot
Print
Annotate
Vector
Circuit Conditions ...
Violations Display ...
Save ...
Select ...
Delete ...
Printing/Plotting Options ...
Main Form ...
Transient Signal
Transient Minus DC
Transient Sum
Transient Difference
AC Magnitude
AC dB10
AC dB20
AC Phase
AC Magnitude & Phase
AC Gain & Phase
Equivalent Output Noise
Equivalent Input Noise
Squared Output Noise
Squared Input Noise
Noise Figure
DC


Direct Plot Form
OK Cancel Help
Plotting Mode Append
Analysis
dc
Function
Voltage
Current
Power
Transresistance
Voltage Ratio
Current Ratio
Power Ratio
Transconductance
Select Terminal
Add To Outputs
Replot
> Select Instance Terminal on schematic...



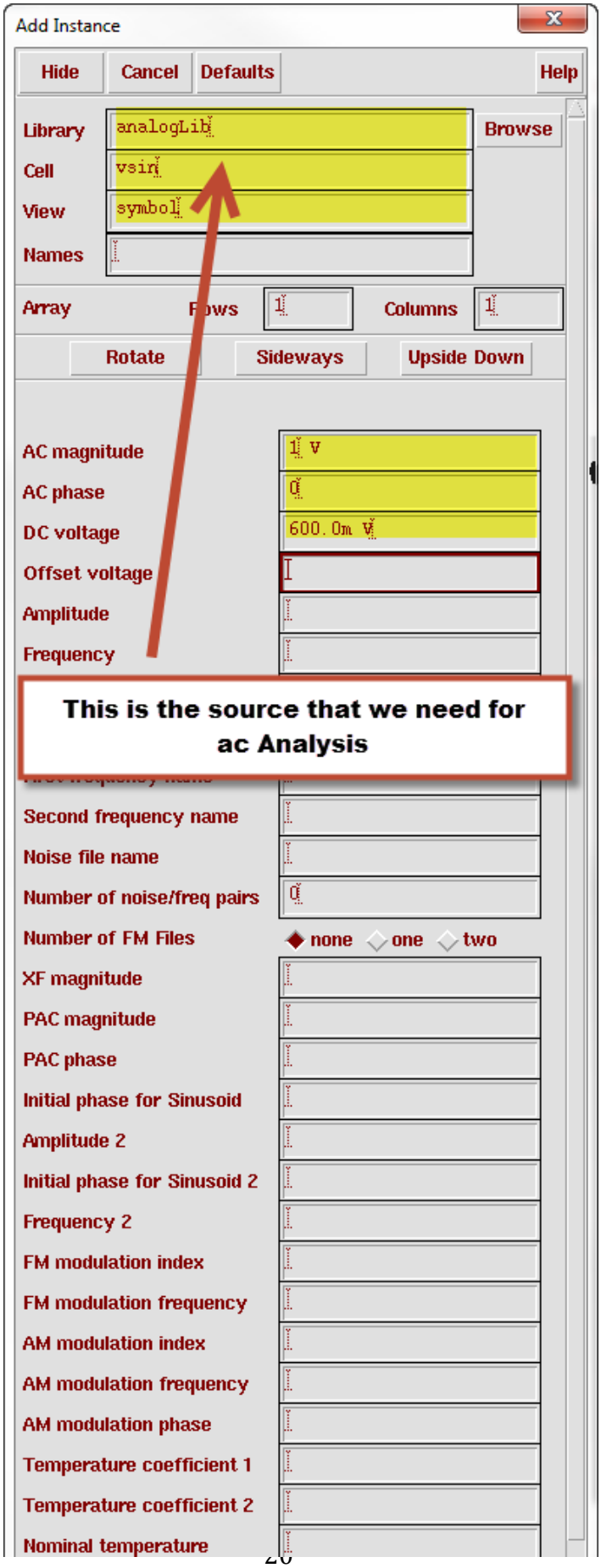
Use calculator (Tools -> Calculator) to calculate the derivate of the above figure, which will be gm:


Calculator
Window Tools Memories Const Options Help
/ubc/ece/home/sm/grads/afarsaei/simulation/ResistiveLoad/spectre/schematic/psf
Selection choices
clip graph selection
off family wave
tran ac dc swept_dc info noise rf
vs is
deriv(IS("/T0/D"))
New Win
Clear Undo Eval
1/x eex Clst Enter
+ 7 8 9
- 4 5 6
x 1 2 3
/ 0 . +/-
average dB10 eyeDiagram
b1f dB20 flip
bandwidth dBm fourEval
clip delay freq
compression deriv frequency
compressionVRI dft ga
convolve dftbb gac_freq
cos evmQAM gac_gain
cosh evmQpsk gainBwProd
cross exp gainMargin
Filter
All
>
cadence

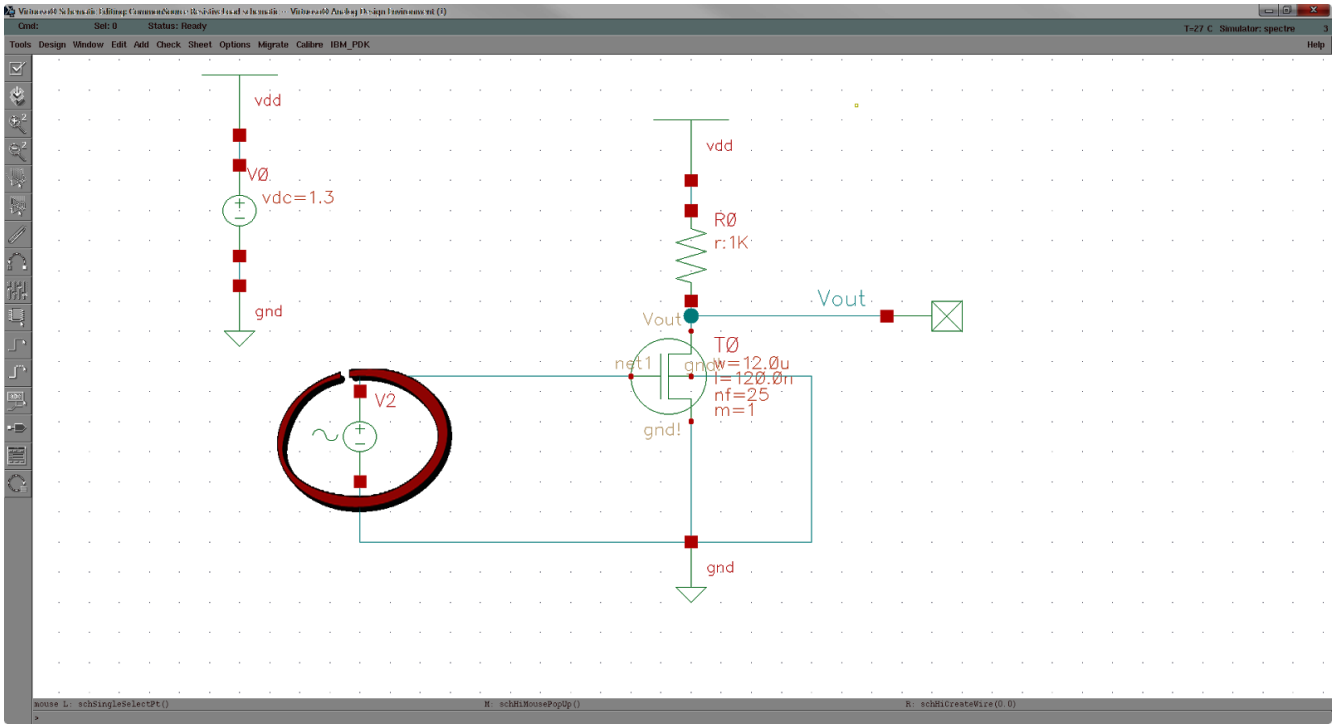

Graph Window 22
File Edit Frame Graph Axis Trace Marker Zoom Tools Help
Aug 22, 2013
deriv(IS("/T0/D"))
10
8.0
6.0
4.0
2.0
0
-2.0
Y0 (E-3)
0
.25
.5
.75
1.0
1.25
1.5
Vin 0
.724778
7.953E-3

4. AC Analysis:

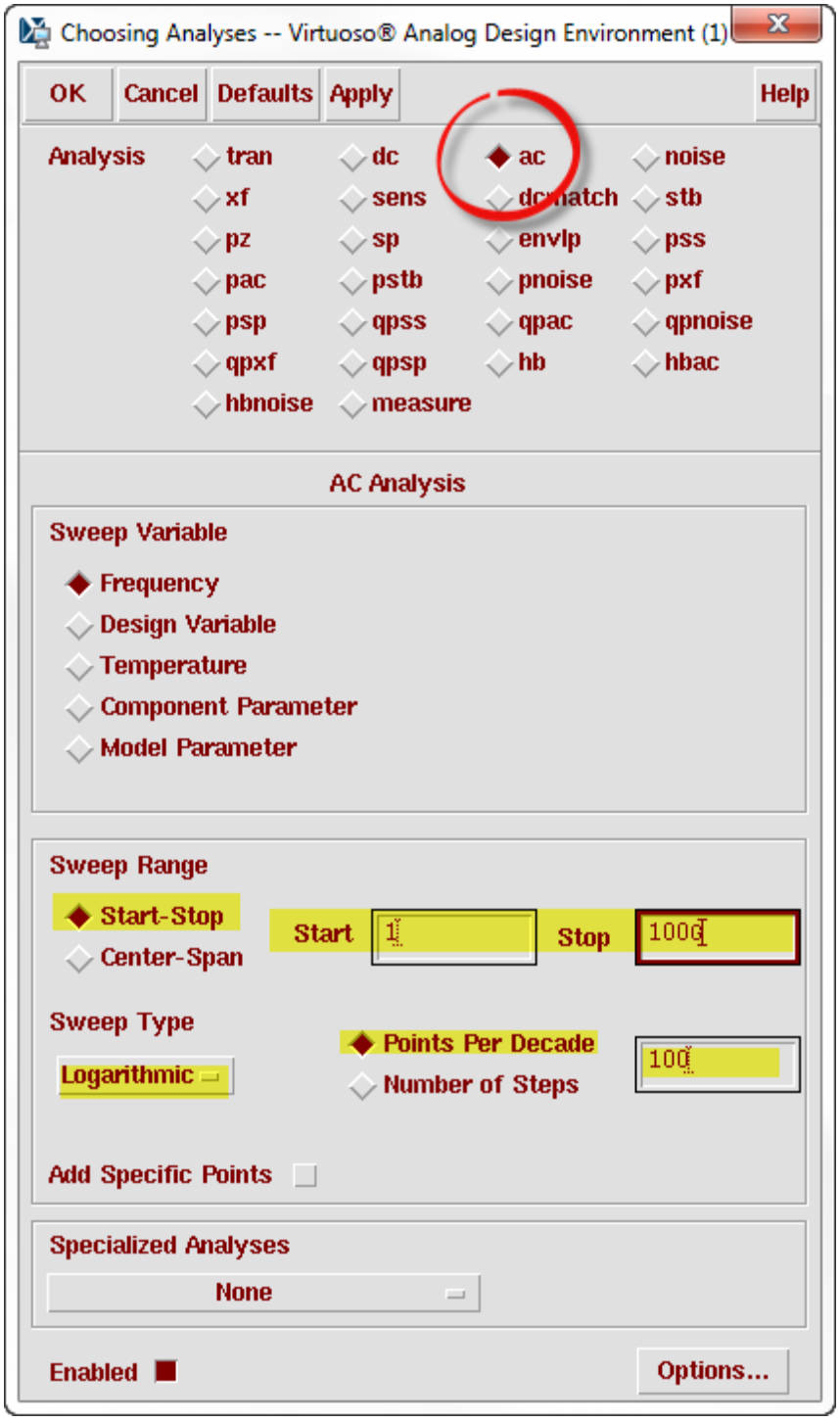
Set up AC analysis by changing the type of input source to “Vsin” as shown on the next page. Please keep in mind that in this simulation the nonlinear circuit will be linearized around its DC operating point (which is 0.6 V); therefore the amplitude of the AC signal in the following figure (1V) will not break the condition for small signal analysis. It has been chosen just to make the interpretation of the simulation results easier.


Add Instance
Hide
Cancel
Defaults
Help
Library
analogLib
Browse
Cell
vsin
View
symbol
Names
Array
Rows
1
Columns
1
Rotate
Sideways
Upside Down
AC magnitude
1 V
AC phase
0
DC voltage
600.0m V
Offset voltage
Amplitude
Frequency
This is the source that we need for ac Analysis
Second frequency name
Noise file name
Number of noise/freq pairs
0
Number of FM Files
none
one
two
XF magnitude
PAC magnitude
PAC phase
Initial phase for Sinusoid
Amplitude 2
Initial phase for Sinusoid 2
Frequency 2
FM modulation index
FM modulation frequency
AM modulation index
AM modulation frequency
AM modulation phase
Temperature coefficient 1
Temperature coefficient 2
Nominal temperature

The schematic after changing the type of input voltage source:

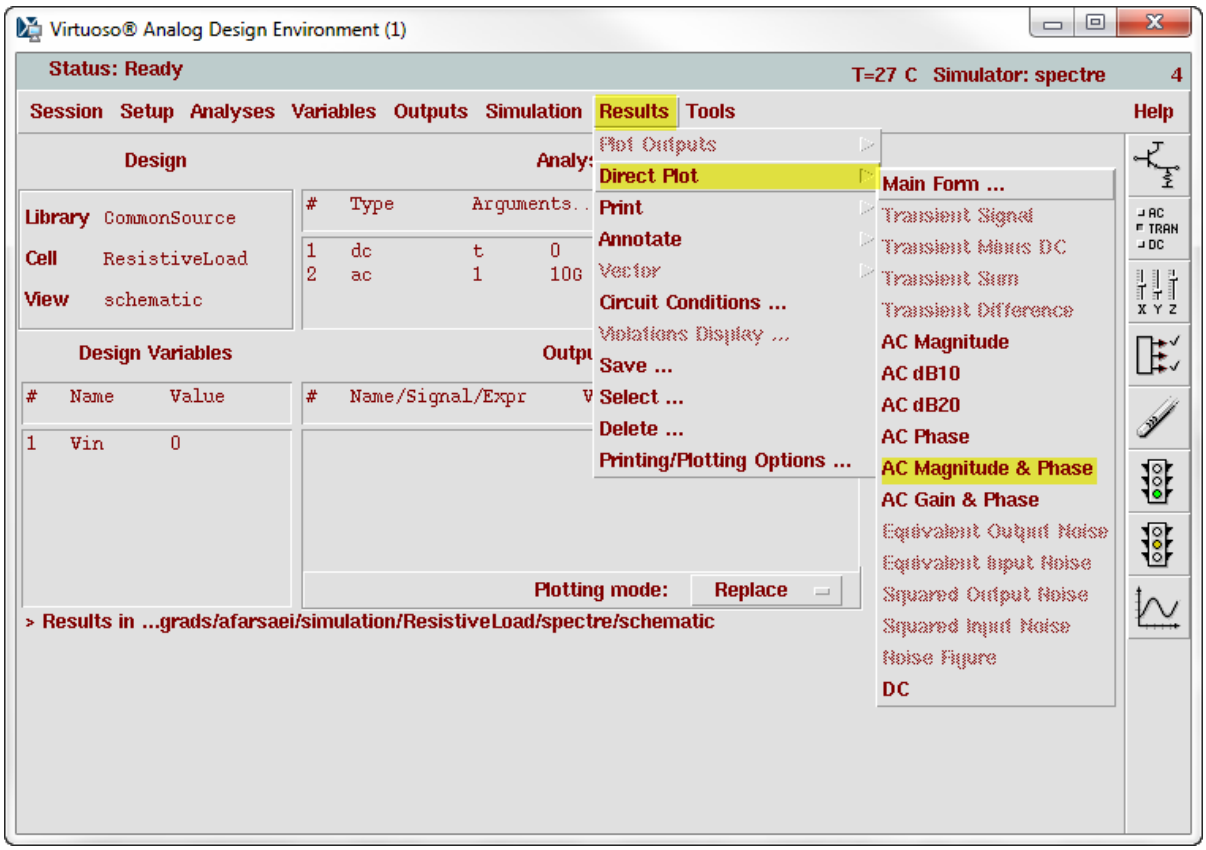


Final step to set up the AC analysis:

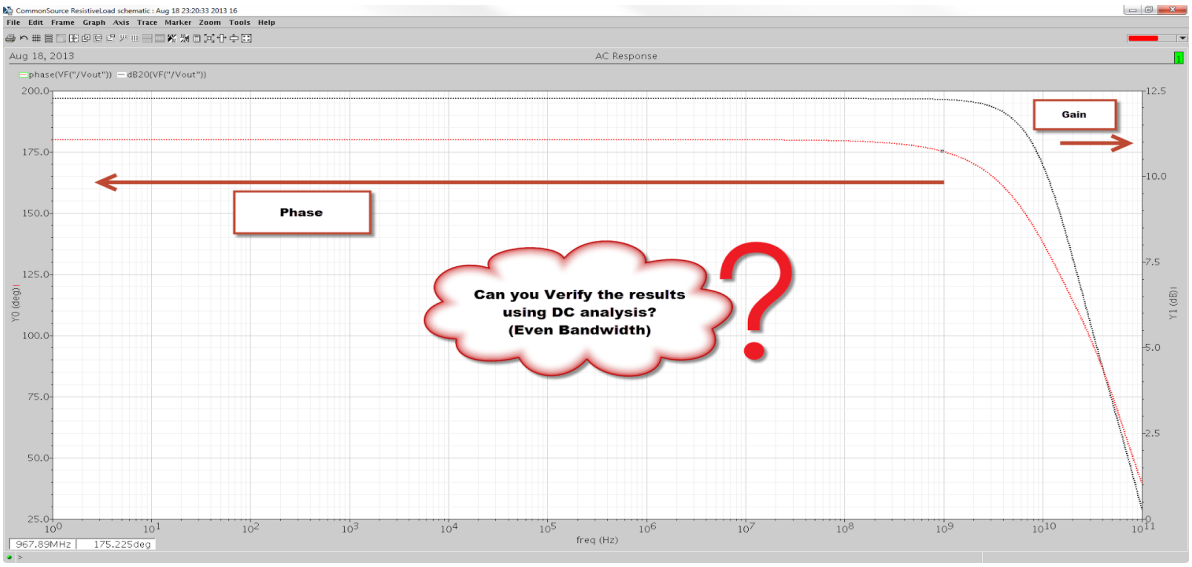


You may of course choose a different frequency sweep range if you are interested in a narrower frequency range.

Plot Simulation results as follow for the Output voltage:



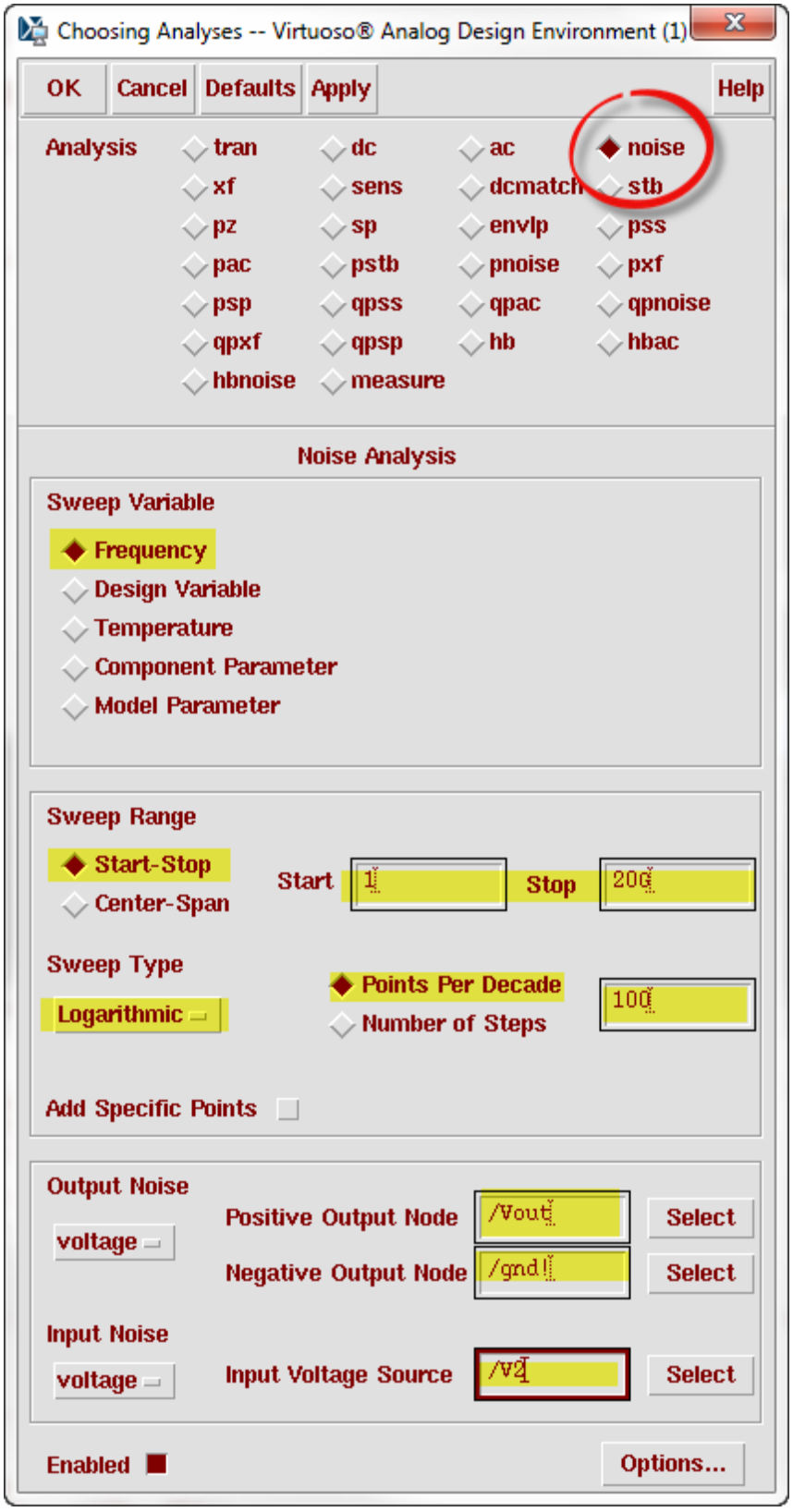
Simulation Results for the Output voltage (These are complex values because they are phasors):



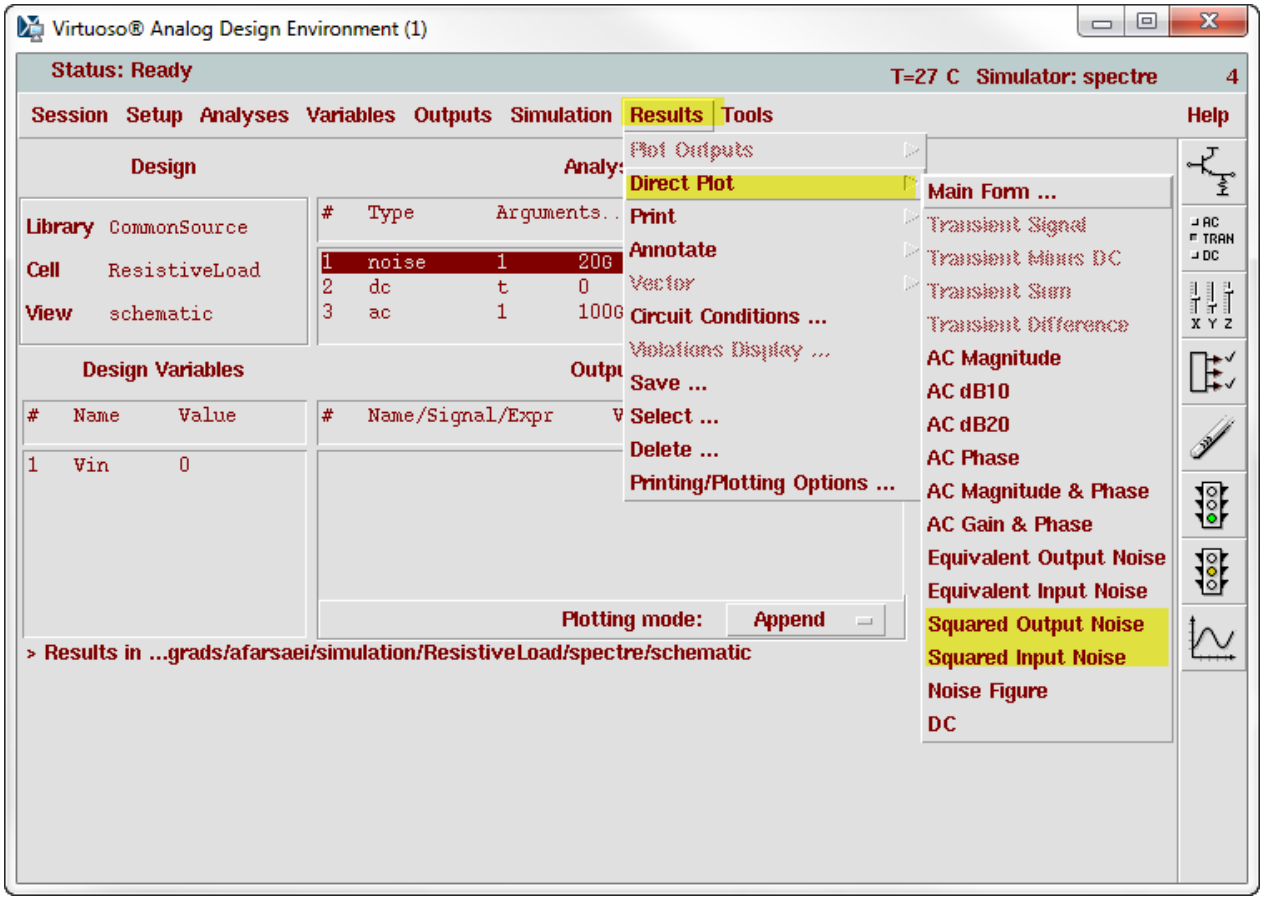
Use the zoom button on the waveform window to highlight the frequency of interest. You may also choose to plot only AC magnitude, AC dB20 (for voltage gain), AC phase, etc.

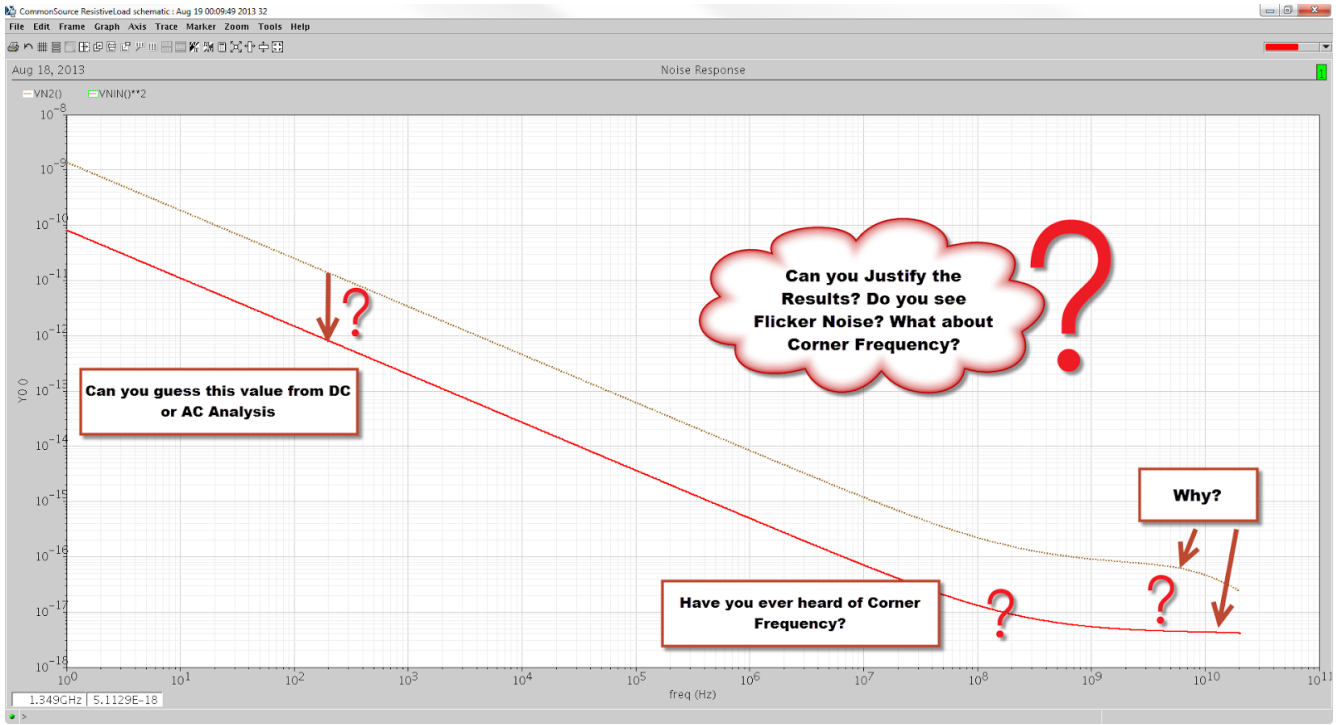
5. Noise Analysis:

Setting up the noise analysis:



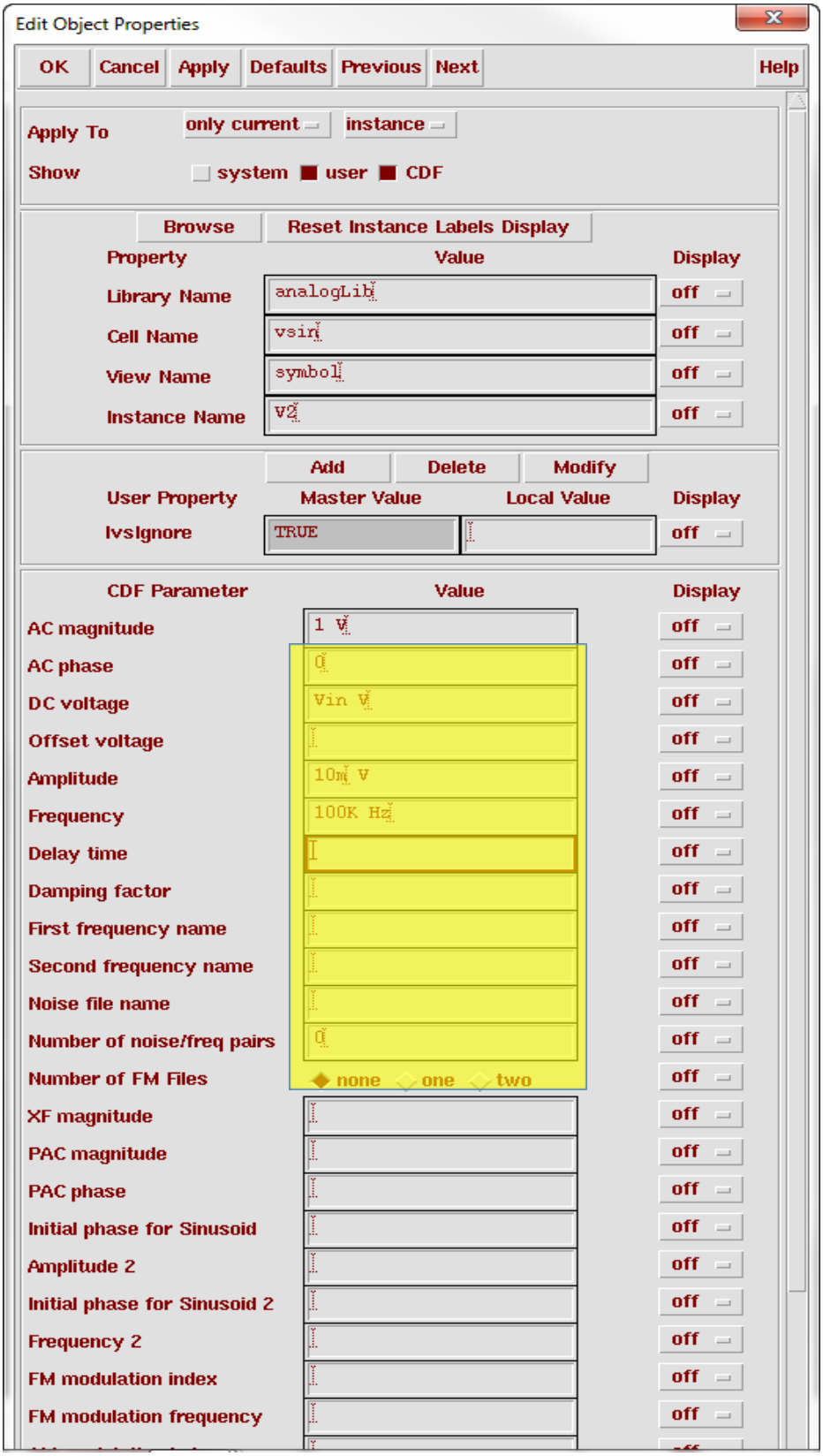
Plot the simulation results:


Virtuoso® Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 4
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library CommonSource
Cell ResistiveLoad
View schematic
Type Arguments..
1 noise 1 20G
2 dc t 0
3 ac 1 100G
Design Variables
Name Value
1 Vin 0
Name/Signal/Expr
Plotting mode: Append
> Results in ...grads/afarsaei/simulation/ResistiveLoad/spectre/schematic
Plot Outputs
Direct Plot
Print
Annotate
Vector
Circuit Conditions ...
Violations Display ...
Save ...
Select ...
Delete ...
Printing/Plotting Options ...
Main Form ...
Transient Signal
Transient Minus DC
Transient Sum
Transient Difference
AC Magnitude
AC dB10
AC dB20
AC Phase
AC Magnitude & Phase
AC Gain & Phase
Equivalent Output Noise
Equivalent Input Noise
Squared Output Noise
Squared Input Noise
Noise Figure
DC

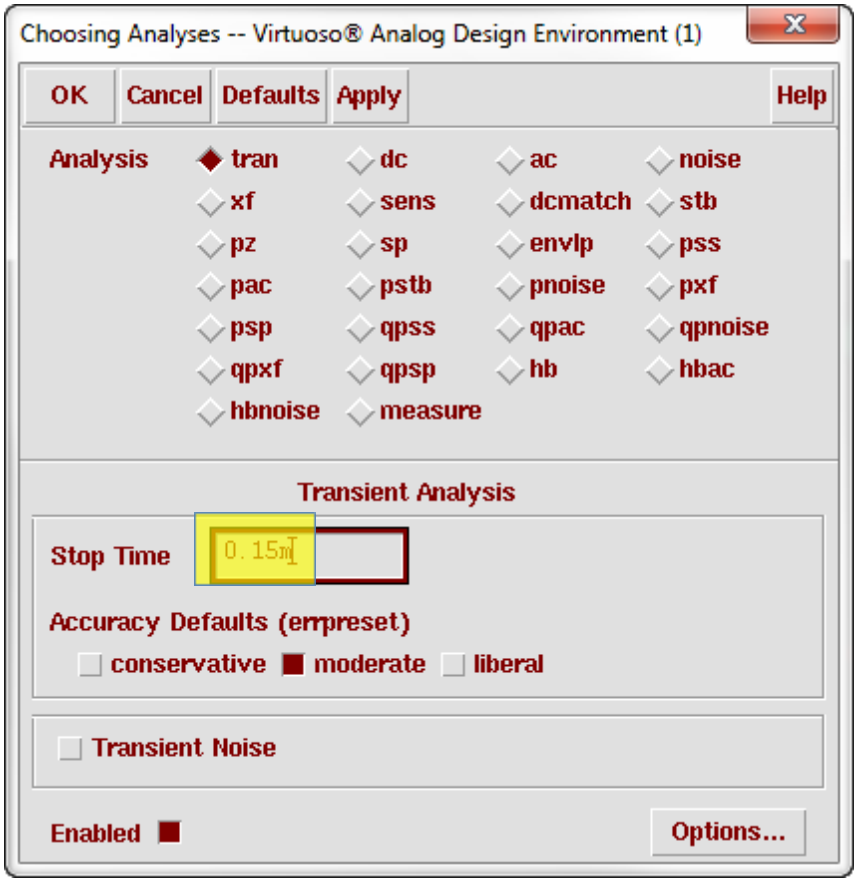

Noise Response
VN2()
VNIN()**2
Can you Justify the Results? Do you see Flicker Noise? What about Corner Frequency?
Can you guess this value from DC or AC Analysis
Why?
Have you ever heard of Corner Frequency?
freq (Hz)

6. Transient Analysis:

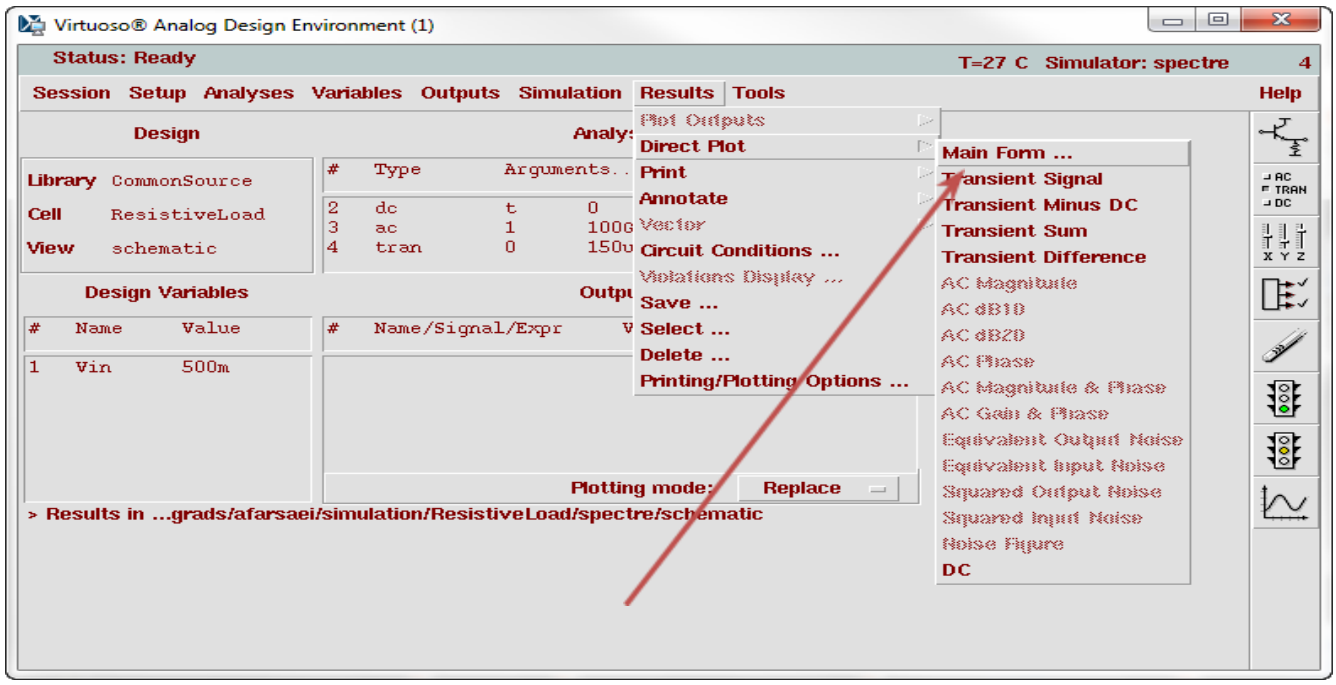
Change parameters of the Input source for transient analysis:

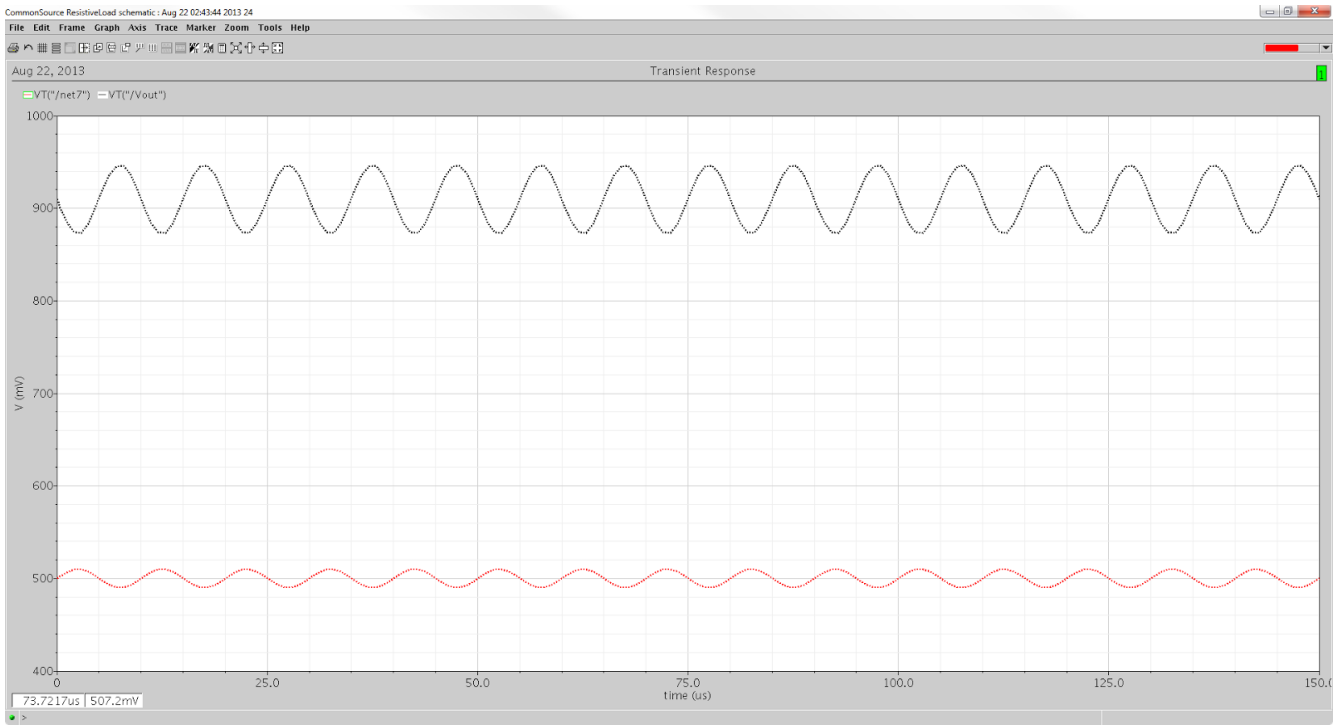

Edit Object Properties
OK
Cancel
Apply
Defaults
Previous
Next
Help
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
analogLib
off
Cell Name
vsin
off
View Name
symbol
off
Instance Name
V2
off
Add
Delete
Modify
User Property
Master Value
Local Value
Display
lvsIgnore
TRUE
off
CDF Parameter
Value
Display
AC magnitude
1 V
off
AC phase
0
off
DC voltage
Vin V
off
Offset voltage
off
Amplitude
10m V
off
Frequency
100K Hz
off
Delay time
off
Damping factor
off
First frequency name
off
Second frequency name
off
Noise file name
off
Number of noise/freq pairs
0
off
Number of FM Files
none
one
two
off
XF magnitude
off
PAC magnitude
off
PAC phase
off
Initial phase for Sinusoid
off
Amplitude 2
off
Initial phase for Sinusoid 2
off
Frequency 2
off
FM modulation index
off
FM modulation frequency
off

Setup Transient Analysis:



Run the simulation and Plot the results you want (Results -> Transient Signal):


Virtuoso® Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 4
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library CommonSource
Cell ResistiveLoad
View schematic
Type Arguments..
2 dc t 0
3 ac 1 100G
4 tran 0 150u
Design Variables
Name Value
1 Vin 500m
Name/Signal/Expr
Plot Outputs
Direct Plot
Print
Annotate
Vector
Circuit Conditions ...
Violations Display ...
Save ...
Select ...
Delete ...
Printing/Plotting Options ...
Main Form ...
Transient Signal
Transient Minus DC
Transient Sum
Transient Difference
AC Magnitude
AC dB10
AC dB20
AC Phase
AC Magnitude & Phase
AC Gain & Phase
Equivalent Output Noise
Equivalent Input Noise
Squared Output Noise
Squared Input Noise
Noise Figure
DC
Plotting mode: Replace
> Results in ...grads/afarsaei/simulation/ResistiveLoad/spectre/schematic


CommonSource ResistiveLoad schematic : Aug 22 02:43:44 2013 24
File Edit Frame Graph Axis Trace Marker Zoom Tools Help
Aug 22, 2013
Transient Response
VT("/net7") VT("/Vout")
1000
900
800
700
600
500
400
V (mV)
0
25.0
50.0
75.0
100.0
125.0
150.0
time (us)
73.7217us 507.2mV