LNA Simulation in Cadence ICFB6

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Sections of this tutorial have icfb5 screenshots. However, the menu options are same in icfb6.

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I. Introduction

In this tutorial, we will cover the simulation and different parameter measurements of a given common-source low noise amplifier (LNA). We will run ac and sp analysis to characterize the LNA behavior. Then, we will setup the pss analysis to measure the 1-dB compression point and pac or qpss analysis to plot the IPN curves.

The pre-requisites for this tutorial are being familiar with 1) Cadence schematic and components libraries, 2) Analog Design Environment (ADE) features, such as setting up the model libraries, defining the outputs to be saved/plotted, using the calculator, setting up the dc and ac analysis, annotating and printing the dc operating points and node voltages, and being able to check the results in the results → direct plot menu.

Previous tutorials of this course have already covered the above-mentioned pre-requisite materials. You may refer to those tutorials for further information.

II. LNA Schematic in Cadence

Question:

The LNA of figure 1 is designed using a common-source configuration. Target specifications are:

- f_0=900MHz

- Voltage gain >10dB

- Power consumption <5mW

- S_{11}<-10dB

- Input impedance matching to 50Ω

- The circuit has an output capacitance of C_L=10pF. The nmos transistor's W and L are: W=50um/L=0.13um. V_{dd} is 1.2V, V_s=200mV and R_s=50Ω.

The load inductance has series parasitic resistance of R_d.

Draw the circuit in Cadence schematic and verify the specifications and measure the s-parameters, 1-dB compression point and IIP3 of the circuit.

Solution:

We have selected a circuit configuration as shown in figure 1. As it is shown in this figure, the inductor L_d is non-ideal, having a series resistance R_d. R_T is used for matching purposes and C_{in} is a decoupling capacitor.

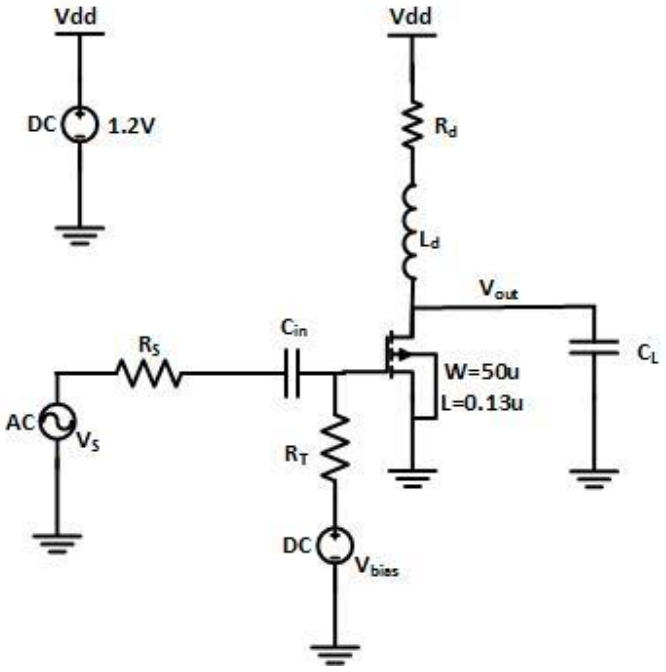

Fig. 1: LNA schematic

To draw the circuit schematic in cadence, we start from the non-ideal inductor and make a symbol view for it. To do that, start with a new schematic and call it ind_res. Draw an inductor with a series resistor. Attach two ports, called ind1 and ind2 to the two ends, as shown in figure 2. Make sure the ports directions are defined as "InputOutput". Then, from the menus, go to design->Create cellview-> From Cellview.

In the window that appears, click ok, and proceed to the next pop-up window (figure 3), where you define the placement of your non-ideal inductor input/outputs. Click ok, and your inductor's symbol which is nothing but a rectangle and two ports will open up in a new schematic window. You can edit the shape if you like. Close this window after you apply your edits.

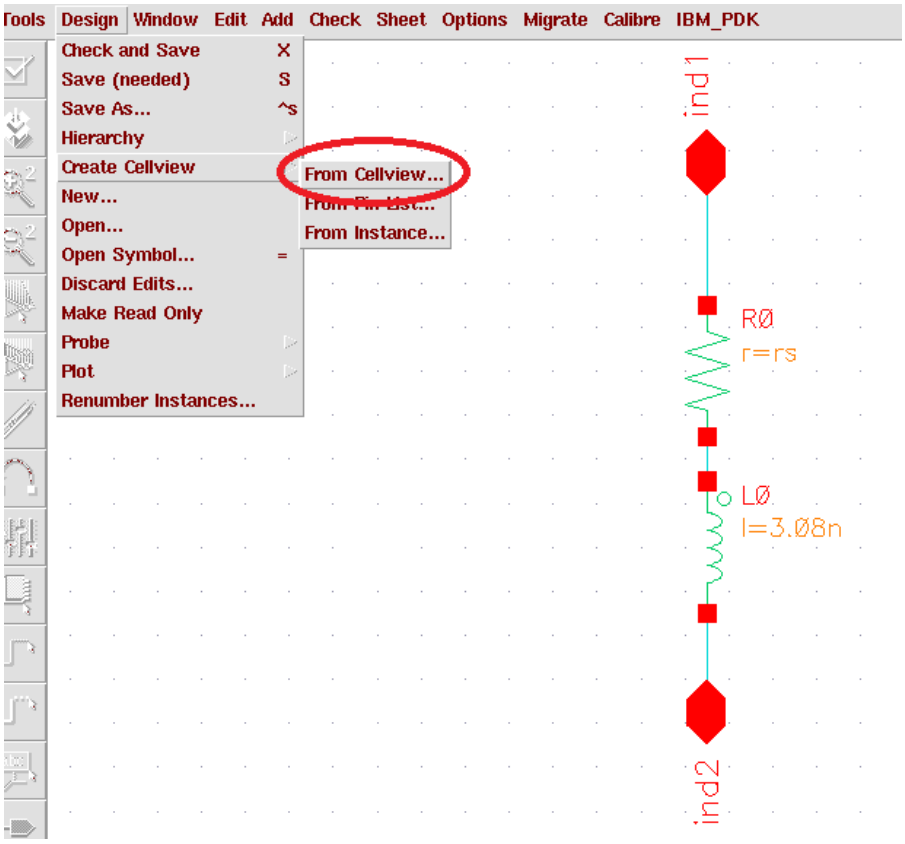

Fig. 2: Non-ideal inductor and how to make a symbol

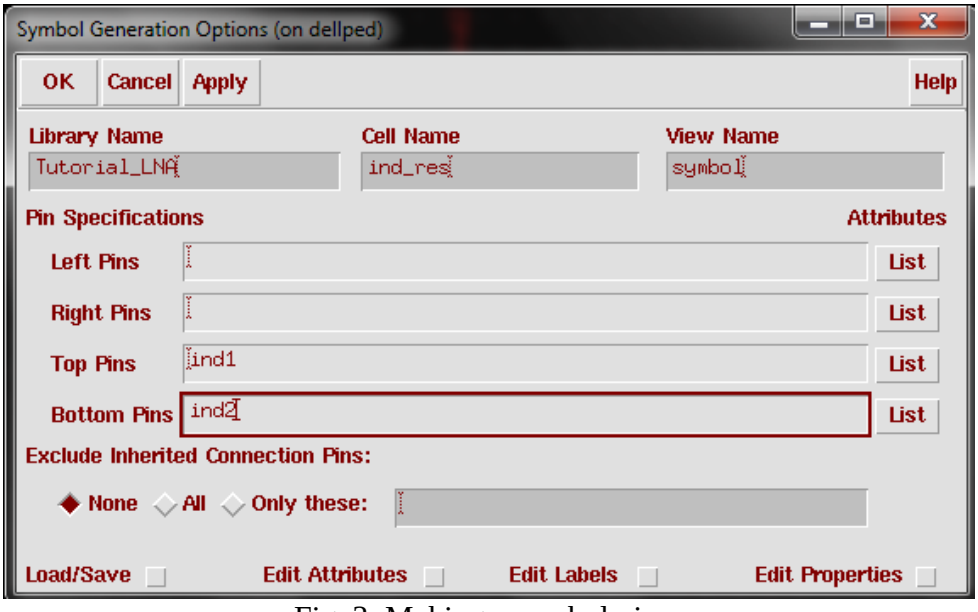

Fig. 3: Making a symbol view

Open a new schematic cellview and draw your circuit like figure 4. You may call this schematic LNA_schematic. For the non-ideal inductor model, use your own symbol from your design library.

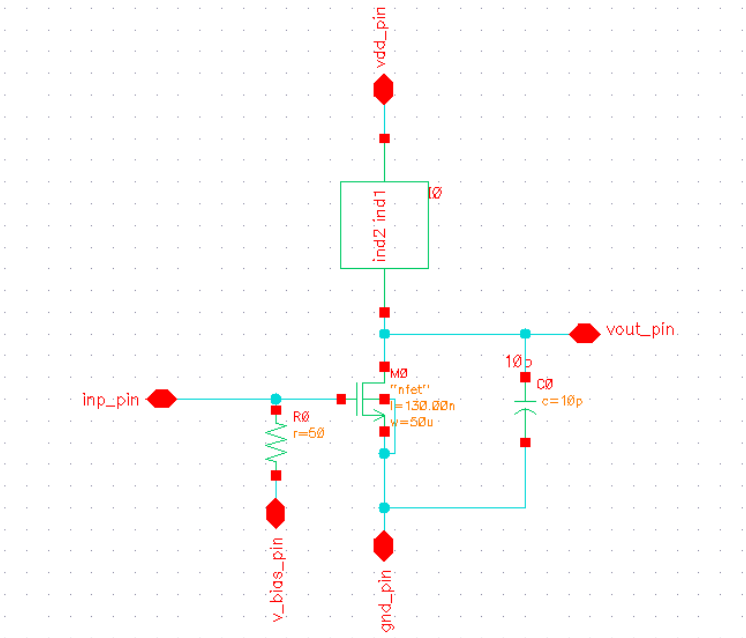

Fig. 4: LNA schematic

We are again making a symbol view of this circuit, so make sure you put inputoutput ports for all your inputs and outputs of the circuit as shown in figure 4. Using the instructions of figures 2 and 3, make a symbol view of this circuit and define the port placements, in a reasonable way (Look at figure 5 for inspiration).

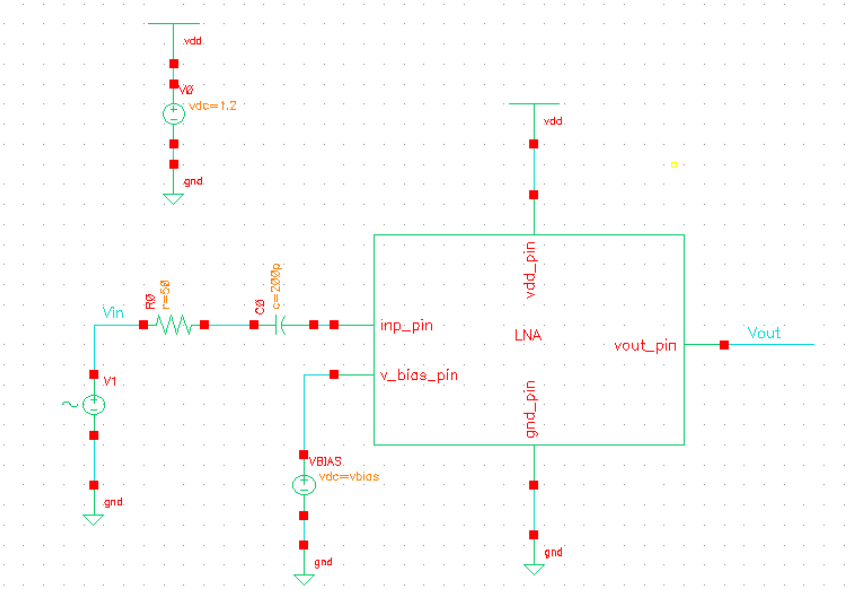

Fig. 5: LNA Test Bench

Then, make another schematic, call it LNA_tb (tb stands for test_bench). Using your LNA_schematic symbol view, draw the circuit of figure 5.

III. LNA Characterization and Measurements

➢ DC and AC analysis

Run DC and AC analysis based on the instructions in previous tutorials.

Check your DC operating points. What is the DC current? How about the power consumption?

Check the gain and resonance frequency (figure 6). Make sure they meet the specifications.

Question: play with the value of the inductor's parasitic resistance. How does the gain and resonance frequency change? Do you see the importance of the careful layout?

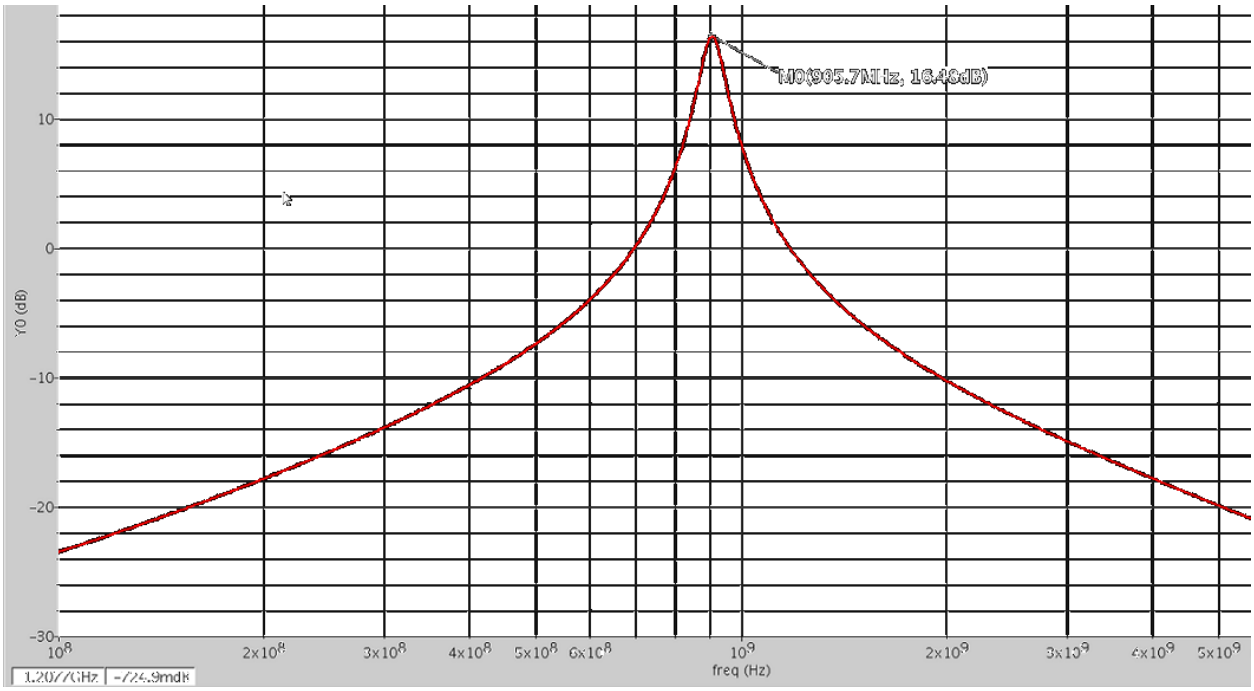

Fig. 6: Voltage gain

➢ SP analysis

Now, we are going to check the s and z parameters of the circuit, as well as the noise figure using the sp analysis. To run sp analysis, you need to have "ports" at the circuit input and/or output.

Take out the V_s and R_s in the LNA_tb schematic and replace them with a port from analogLib library. Also, put another port at the output. The schematic is now similar to figure 7.

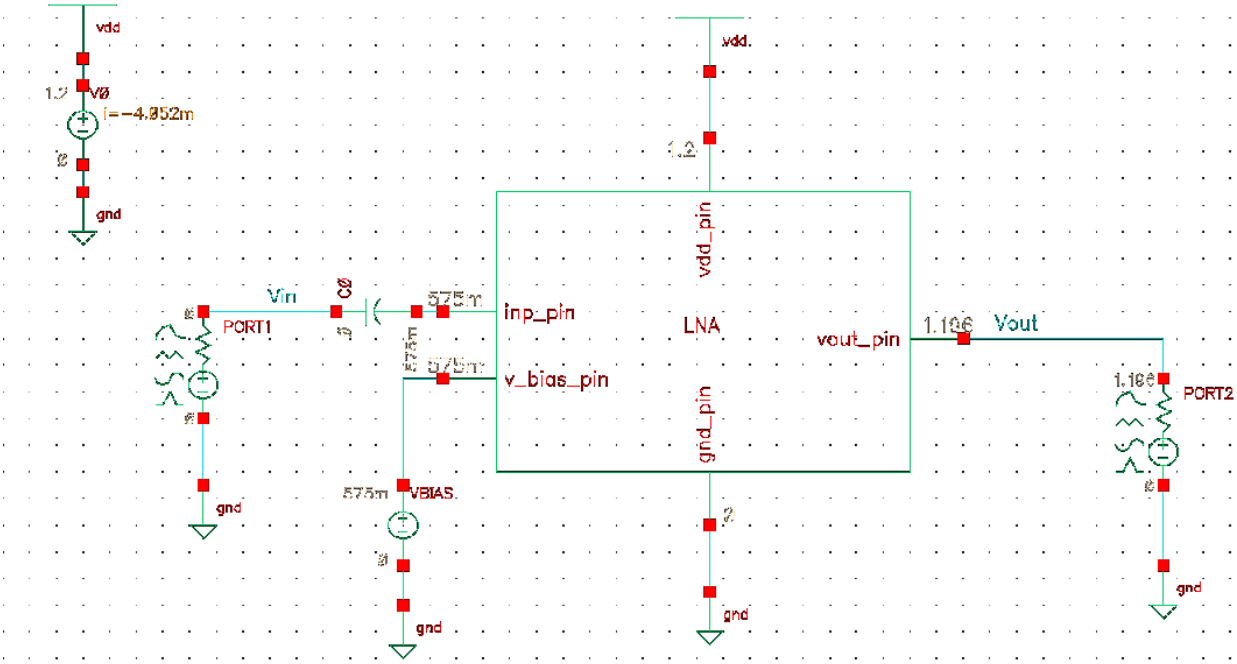

Fig. 7: Circuit schematic with input and output ports

For the input port, set 50Ω for resistance, and define a sinusoidal input of 900MHz as in figure 8. For the output port, set 10MΩ for resistance to represent an "open". Do not set the values for the source in this port.

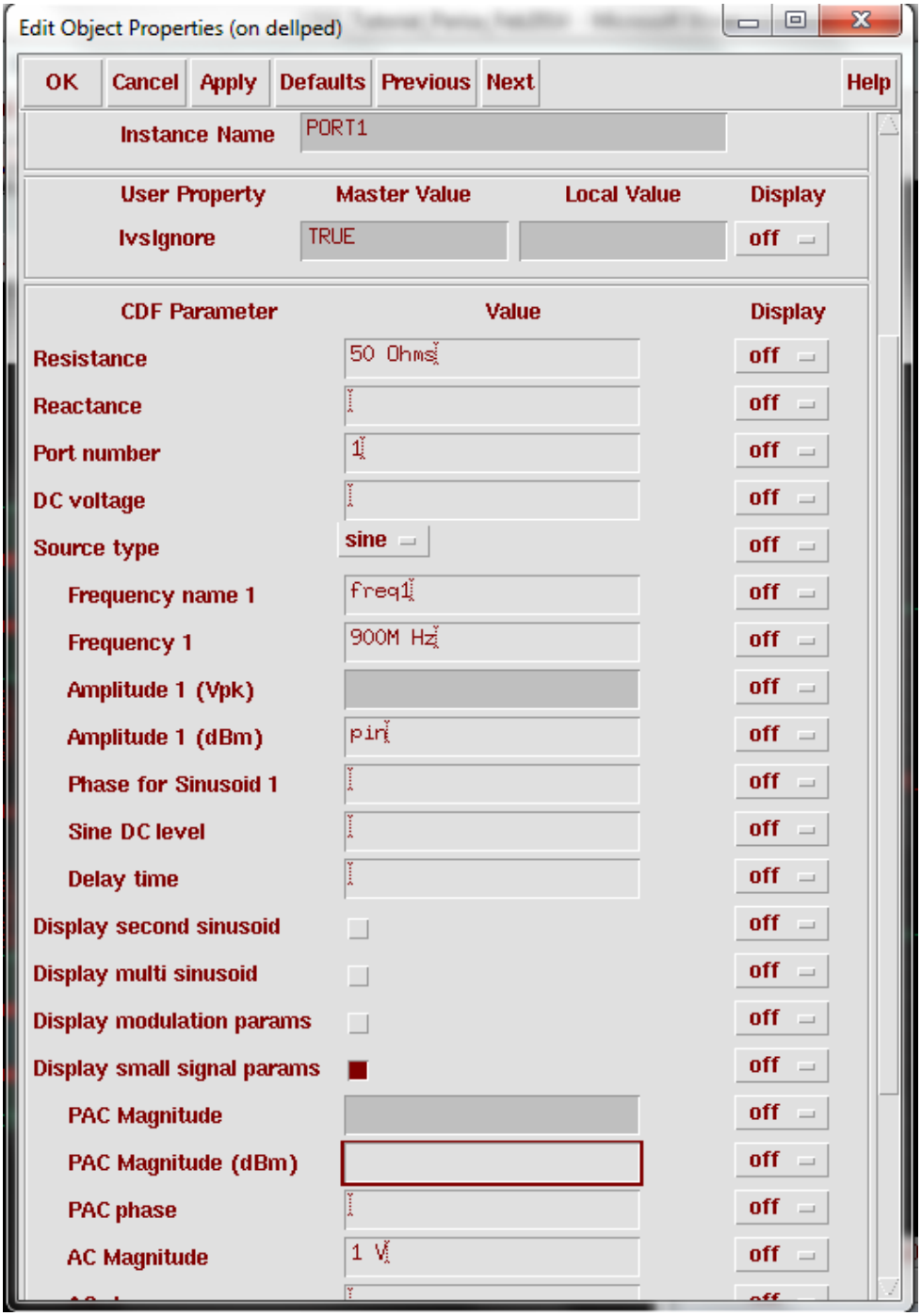

Fig. 8: Input port setup

Check and save this schematic. In the analog design environment, make sure to give a value (for example -30) to p_{in} variable, which is the input port's power. Choose the "sp" analysis to run s-parameter analysis. Setup the analysis as in figure 9. Make sure your ports are in the right order (input port first in the "ports" section). Click ok and run the simulation.

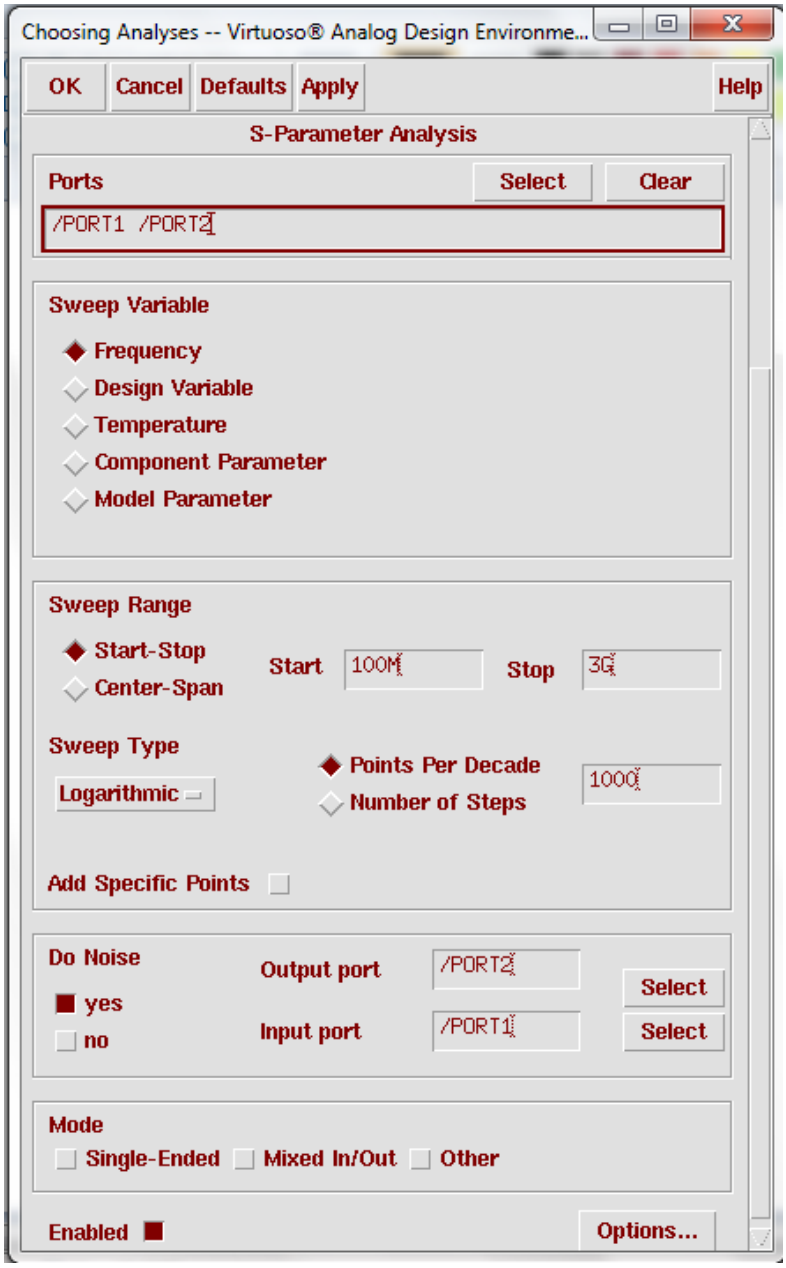

Fig. 9: sp analysis

After finishing the simulation, go to results->direct plot->main form (figure 10):

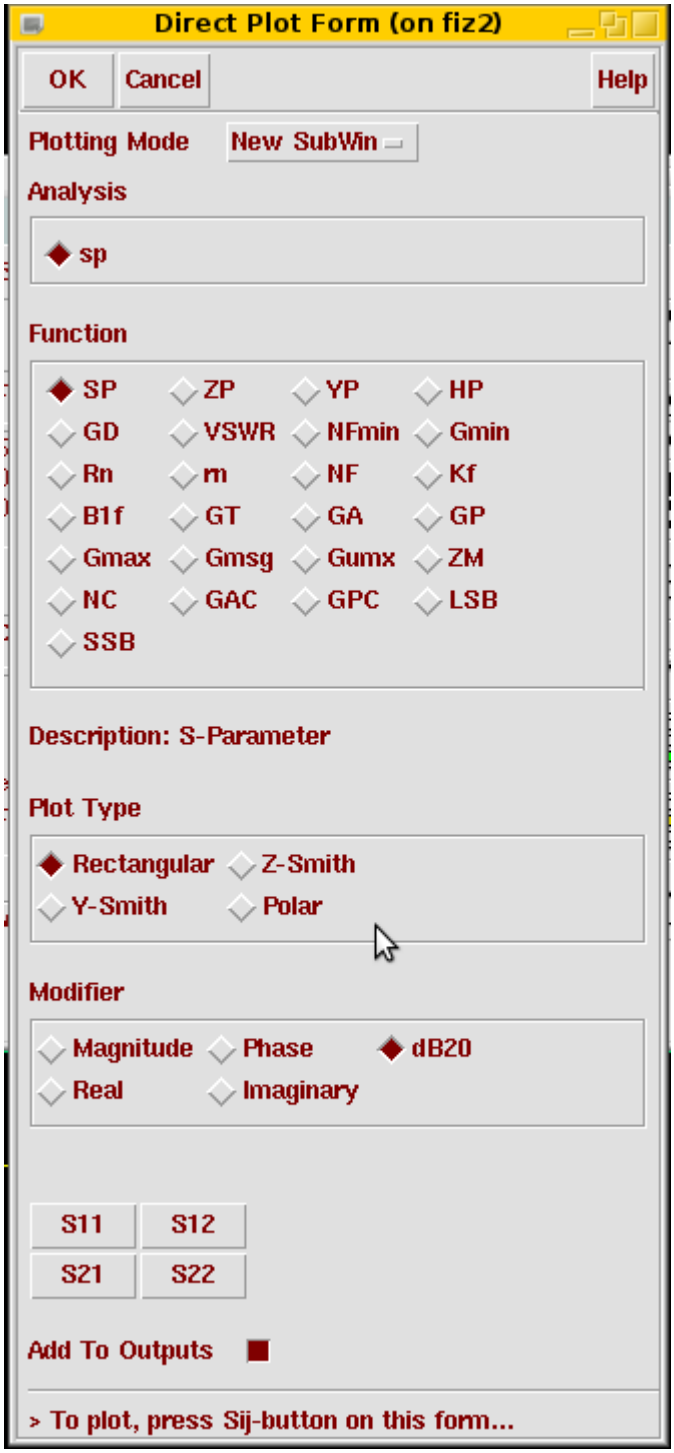

Fig. 10: sp analysis direct plot form

Choose “new subwin” for plotting mode. If you have multiple analysis, choose “sp”. Under “function”, choose “SP”. Select “rectangular” for plot type and “dB20” for modifier.

Try plotting S_{11} and S_{21} (figure 11). What does the S_{11} plot tell you? How is the input matching?

What about S_{21}? Does it match the gain plot? (Should it match at all?)

Are you expecting output matching as well? Check your output matching by plotting S_{22}.

Also, check your S_{12}. What does that tell you about "isolation"?

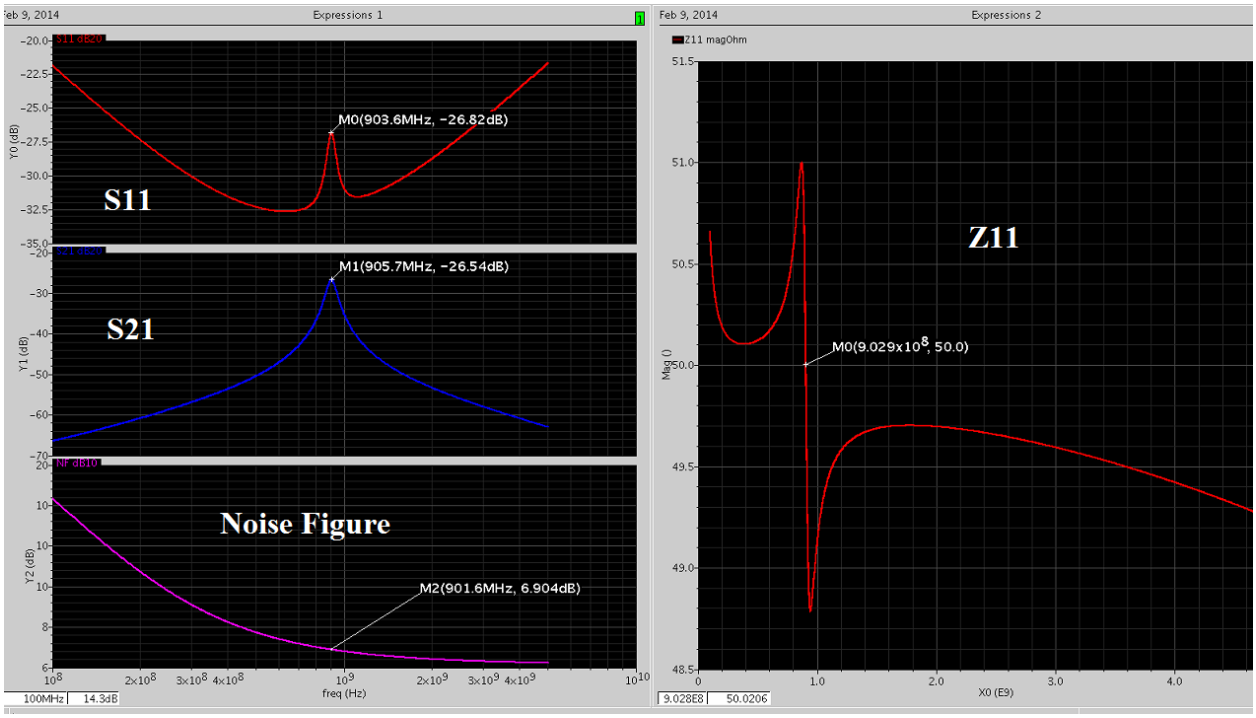

Fig. 11: Plots for S_{11}, S_{21}, NF and Z_{11}

To check the noise figure, in the above form, click on NF, and plot the noise figure (figure 11). How much is the noise figure at the resonance frequency? How could you make it better?

Click on zp, and plot Z_{11} (figure 11). What do you see? Does it match your expectation? How about Z_{22}?

➢ PSS and PAC analysis

- **1-dB compression point**

Now, to measure the 1-dB compression point, setup a pss analysis as in figure 12.

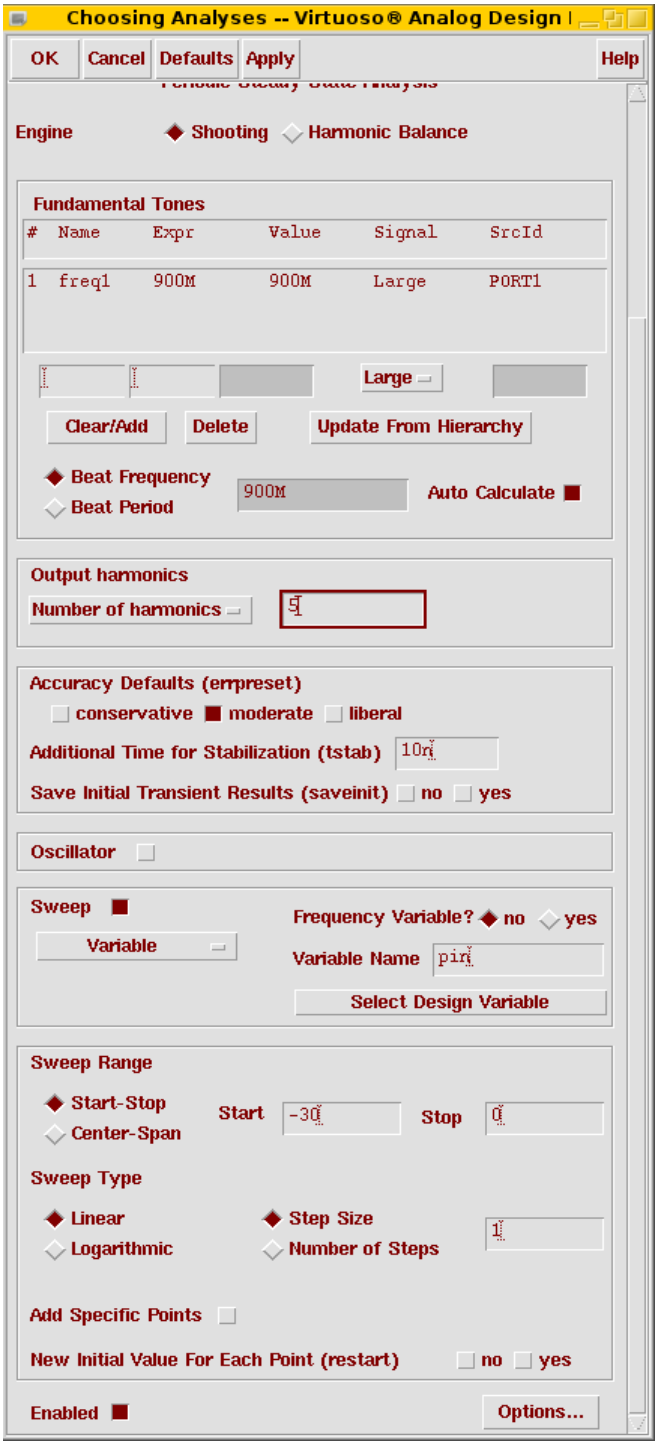

Fig. 12: Setting up a pss analysis for 1-dB compression point measurement

After running the simulation, go to results->direct plot->main form. Select pss analysis, under function, select "compression point", then Port (fixed R(port)), then "output power" and enter "1" for "gain compression". Enter -30 for p_{in}. Select "input referred 1dB compression" and then select the first order harmonic of the circuit (900MHz). Select the output port on the schematic and click "replot" to see the compression point graph. Your plot should look similar to figure 13.

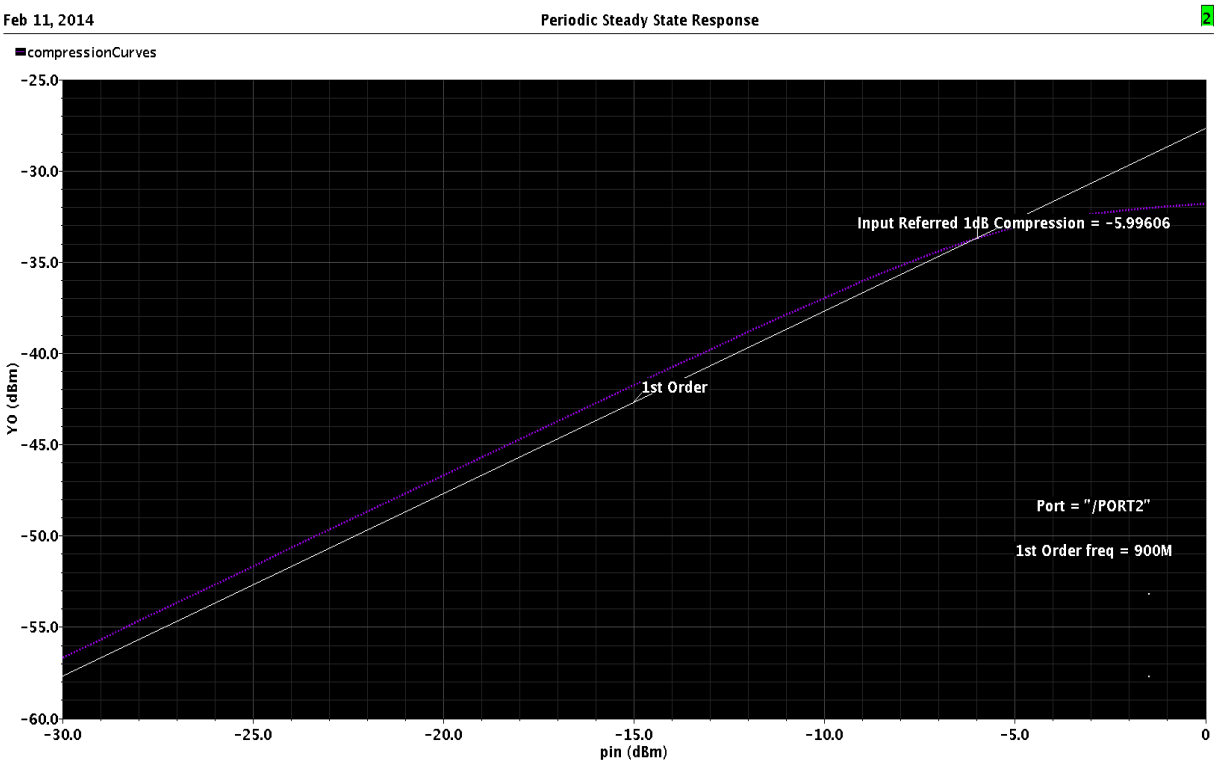

Fig. 13: A typical 1-dB compression point analysis result

Go back to pss analysis setup. Change the "number of harmonics" to 1 and see the simulation results. Do this for 3 harmonics as well. Do you see any difference? Refer to the definition of 1-dB compression point measurement, and think if the number of harmonics should change the output results.

- **IPN curves**

To plot the IPN (in our case IP3) curves, pss analysis following by a pac analysis is performed.

Refer to the definition of the intermodulation and third intercept point (IP_3) (for example in RF Microelectronics (second edition) by Behzad Razavi, pages 21-29) to see why two tones with same amplitude are needed for IP3 measurements.

In the schematic test bench, modify the input port as in figure 14. Make sure you enter variable "pin" for "PAC magnitude (dBm)". Your ω_1 is 900MHz.

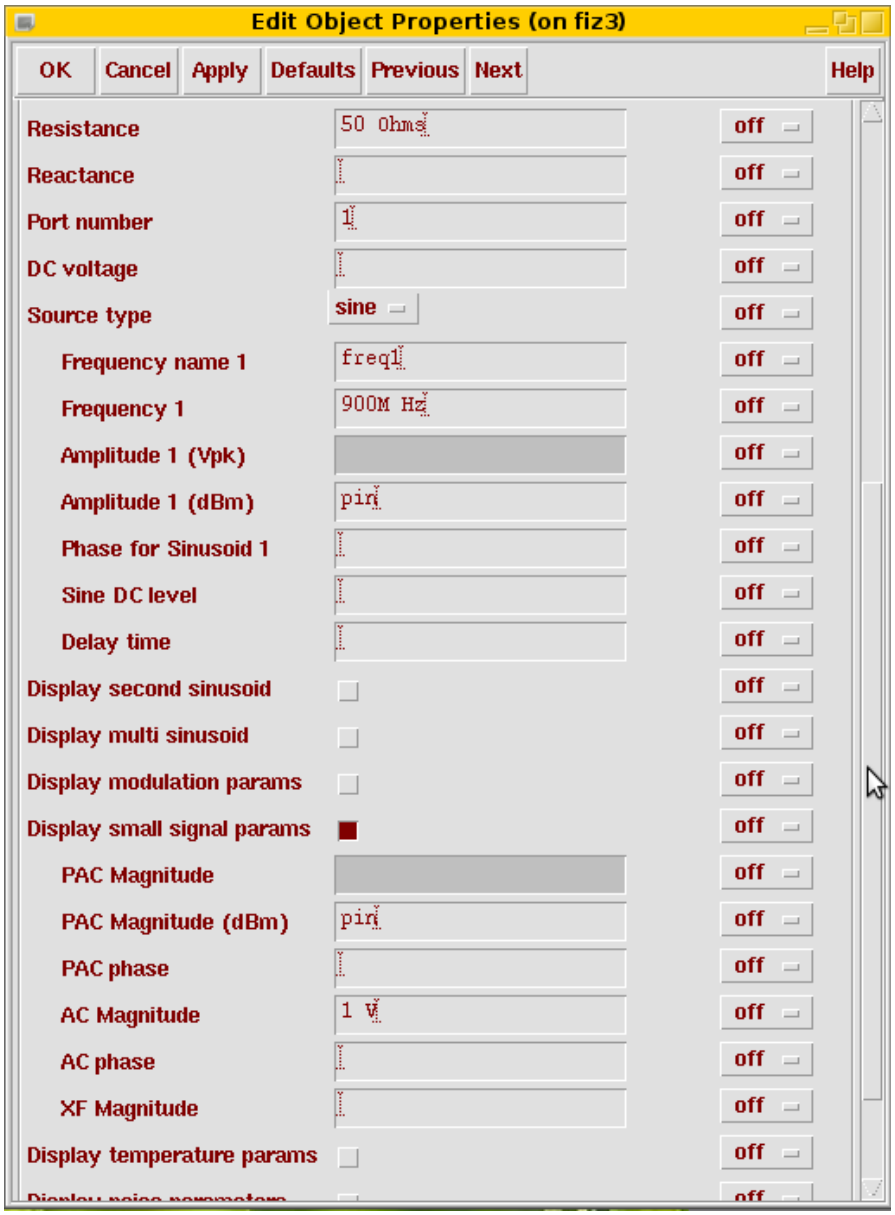

Fig. 14: Modifying the input port for pss+pac analysis

Check and save the schematic. In ADE, set up a pss analysis the same as the setup for 1-dB compression point in figure 12. Select "enabled" and click ok to exit this setup and choose pac analysis from the list. Set up the pac analysis as shown in figure 15. Define a second tone (ω_2) close to the first tone of 900MHz. In here 901MHz is chosen for the second tone.

For maximum sideband, choose 2 to cover 3rd harmonic. Select "enabled" and click ok.

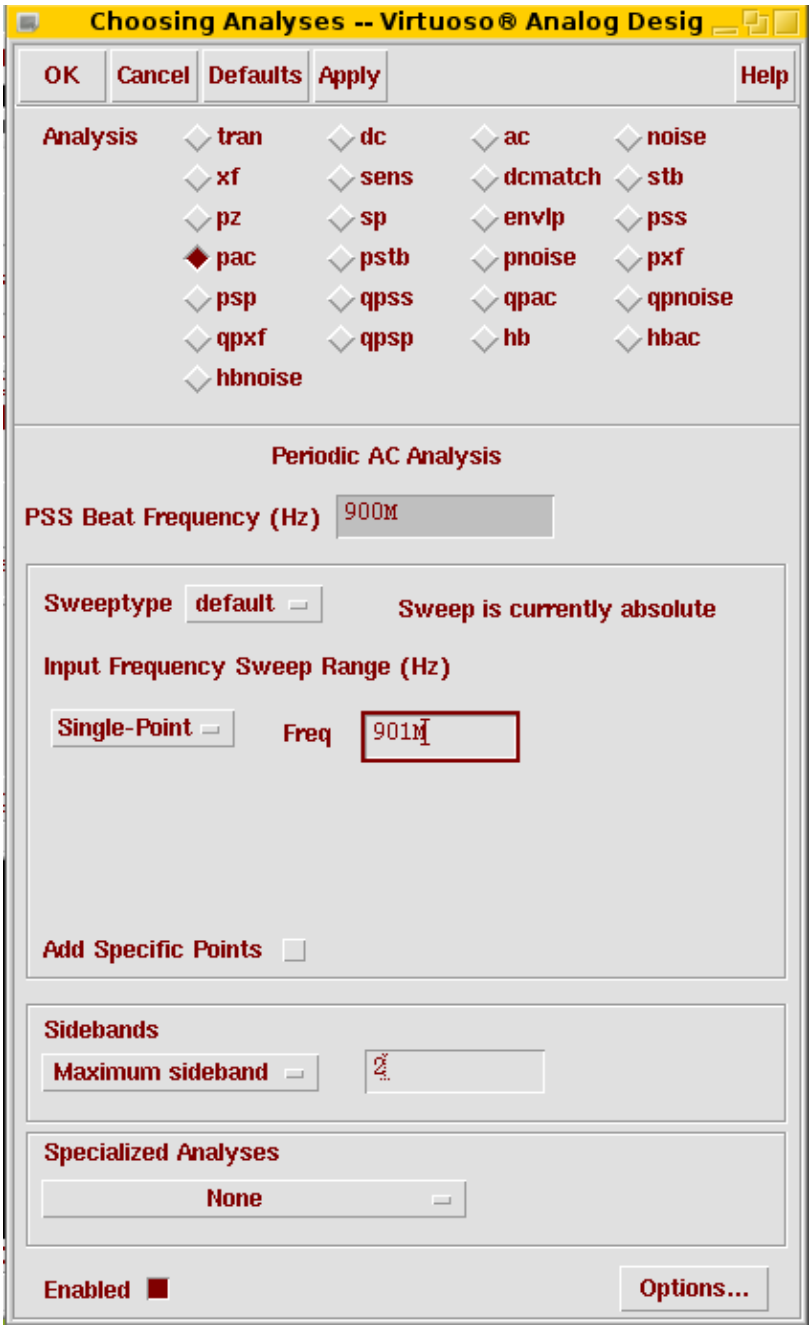

Fig. 15: PAC analysis setup for IP_3 measurement

Run the simulation, and go to results →direct plot→main form (figure 16).

Under analysis, select "pac". Under function, select "IPN curves". Select "Port (fixed R(port)) and for circuit input power, select "variable sweep". Enter an extrapolation point close to the sweep range starting point. To see IIP_3, select "input referred IP3", and to see OIP3, select "output referred IP3". Select "3rd" for order. Select the third order harmonic to be equal to $2\omega_1-\omega_2$. Select the 1st order harmonic to be equal to your ω_2. Select output port by clicking on it to see the IIP_3 curves as in figure 17.

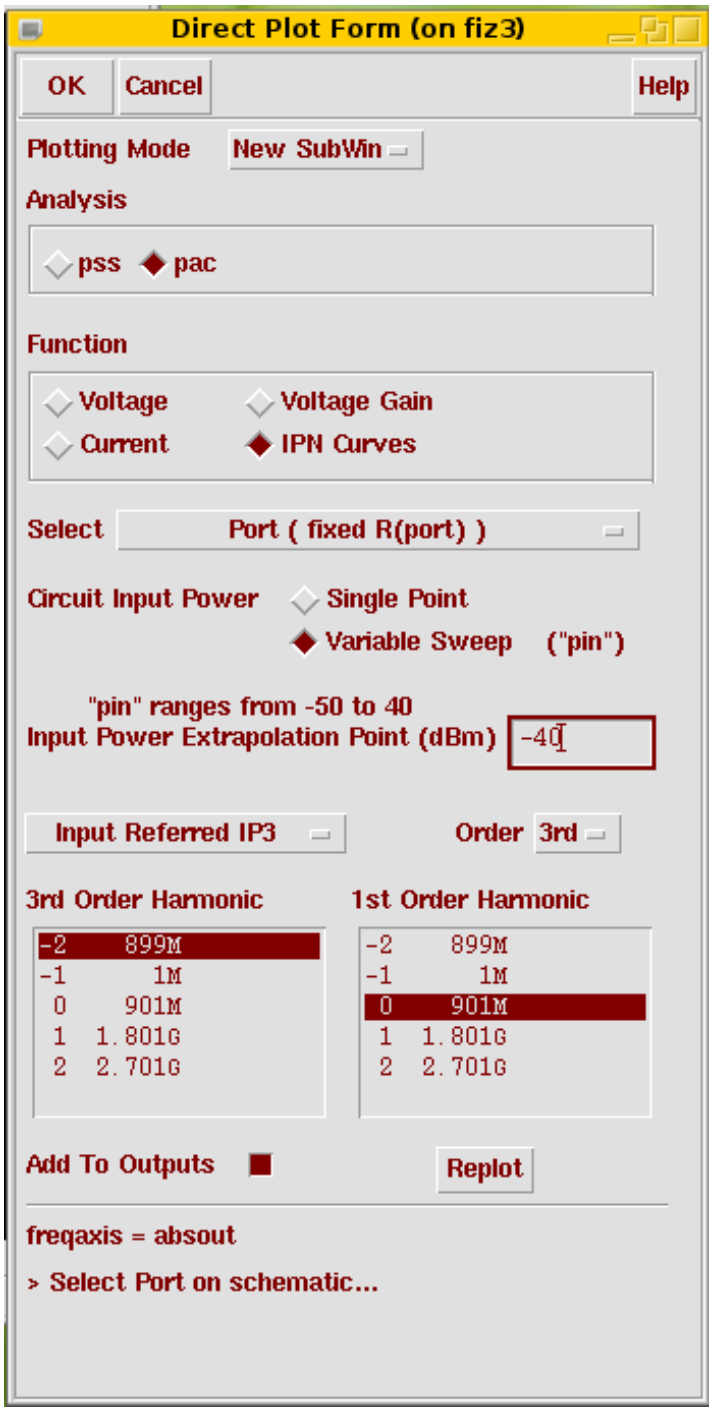

Fig. 16: PAC direct plot form

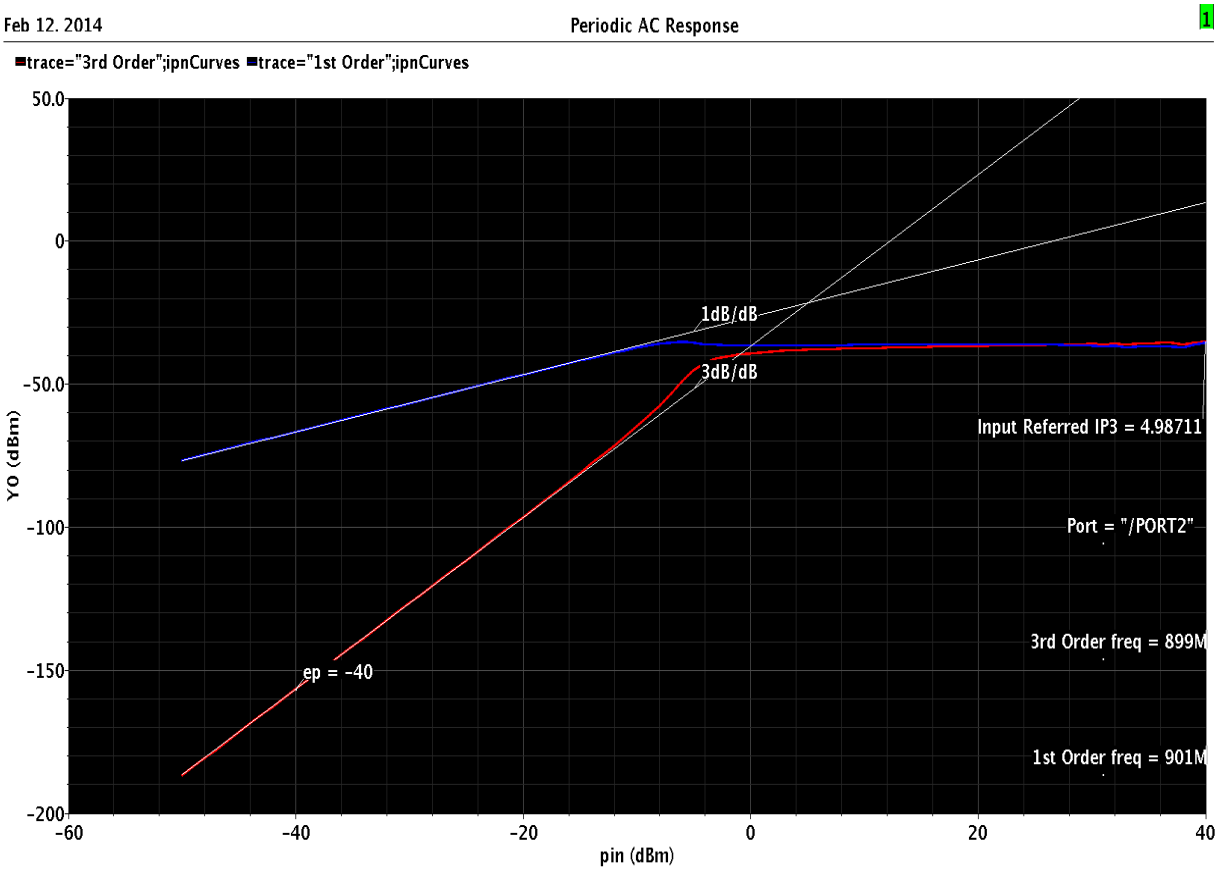

Fig. 17: IIP_3 curves

➢ QPSS analysis

• IPN curves

The second method to plot the IPN curves and measure the third intercept point is the qpss analysis.

To run this analysis, you need to enter the two tones in the input port (in schematic), as shown in figure 18.

Check and save the schematic. Go to analog design environment, and setup the qpss analysis as shown in figure 19. Make sure the second tone is defined to have "moderate" level.

Select "enabled", click ok and run the simulation.

After finishing the simulation, go to results→direct plot→main form, as shown in figure 20.

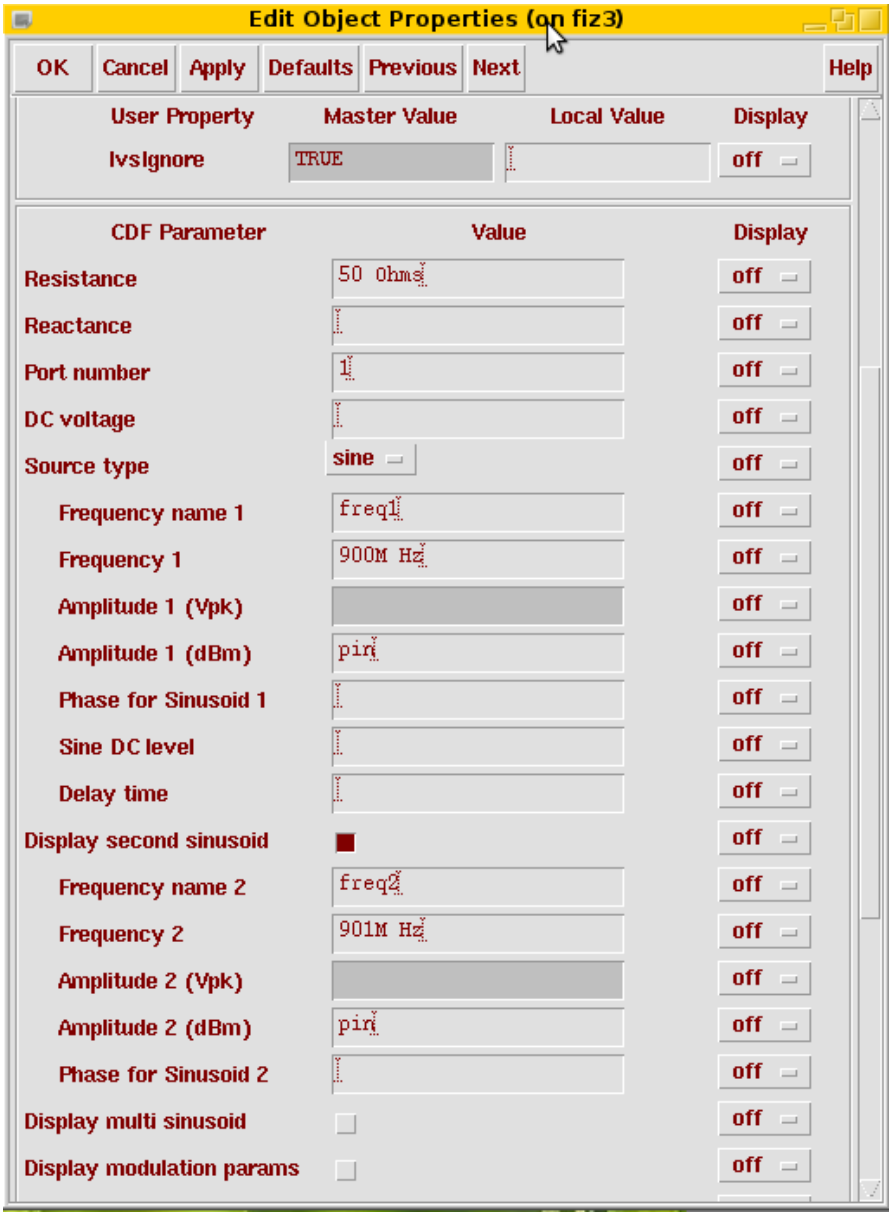

Fig. 18: Setting up the input port for IPN measurements in qpss analysis

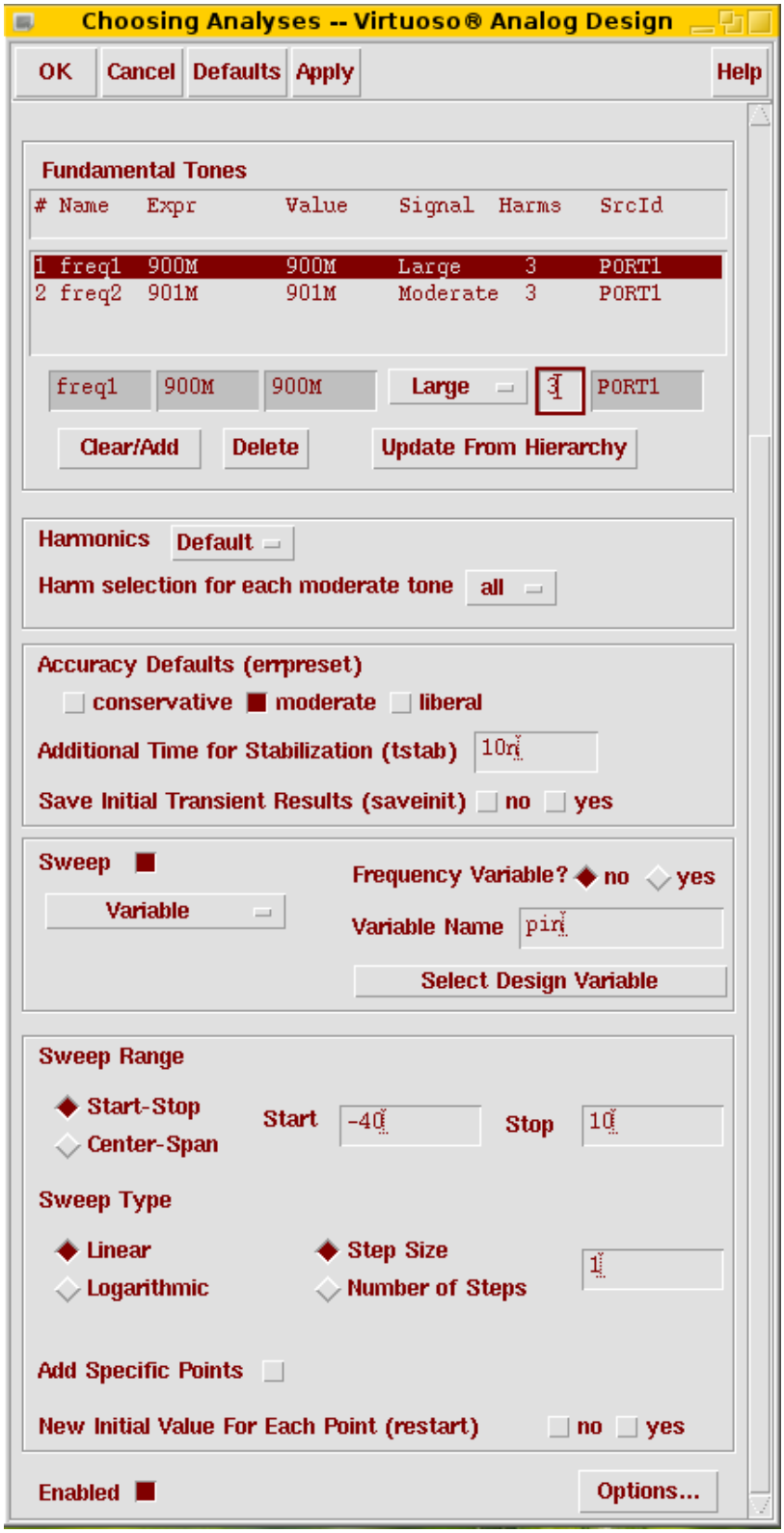

Fig. 19: Setting up the qpss analysis for IPN measurements

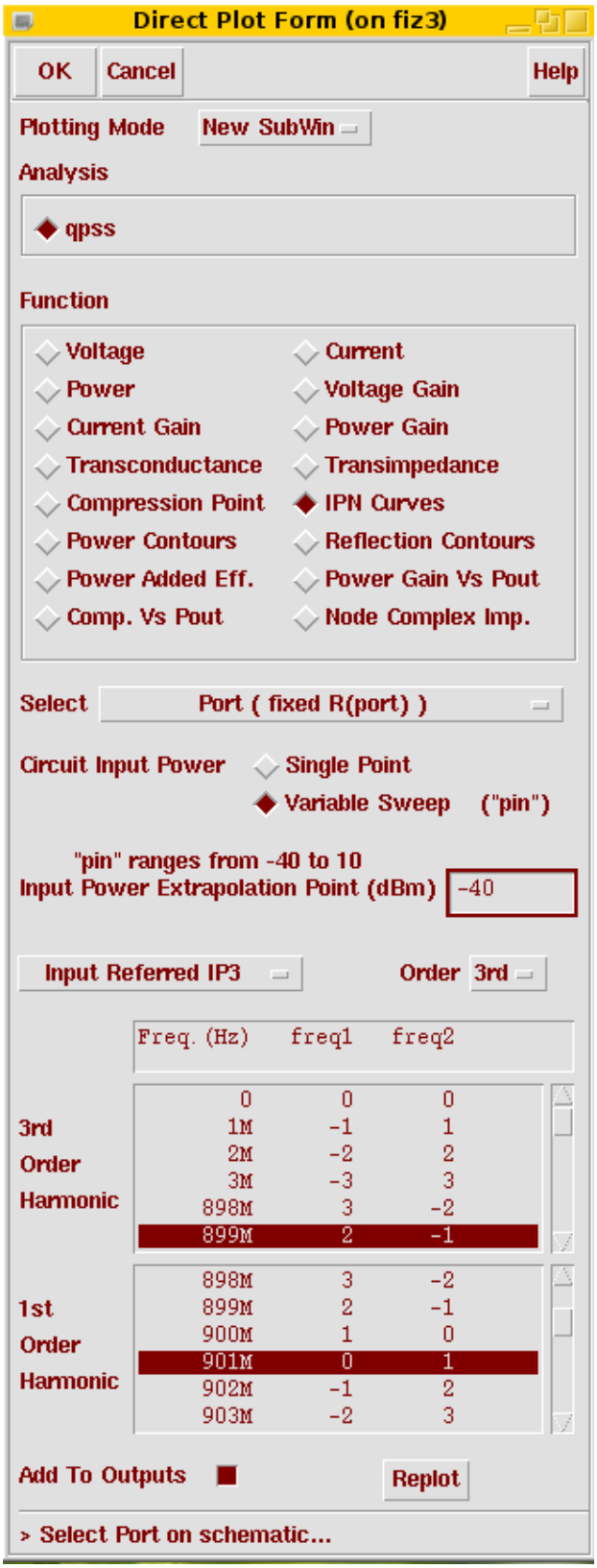

Fig. 20: Direct plot main form for qpss analysis

Under analysis, select “qpss”. Under function, select “IPN curves”. Select “Port (fixed R(port)) and for circuit input power, select “variable sweep”. Enter an extrapolation point close to the sweep range starting point. To see IIP_3, select “input referred IP3”, and to see OIP3, select “output referred IP3”. Select “3rd” for order. Select the third order harmonic to be equal to $2\omega_1-\omega_2$. Select the 1st order harmonic to be equal to your ω_2. Select output port by clicking on it to see the IIP_3 curves as in figure 21.

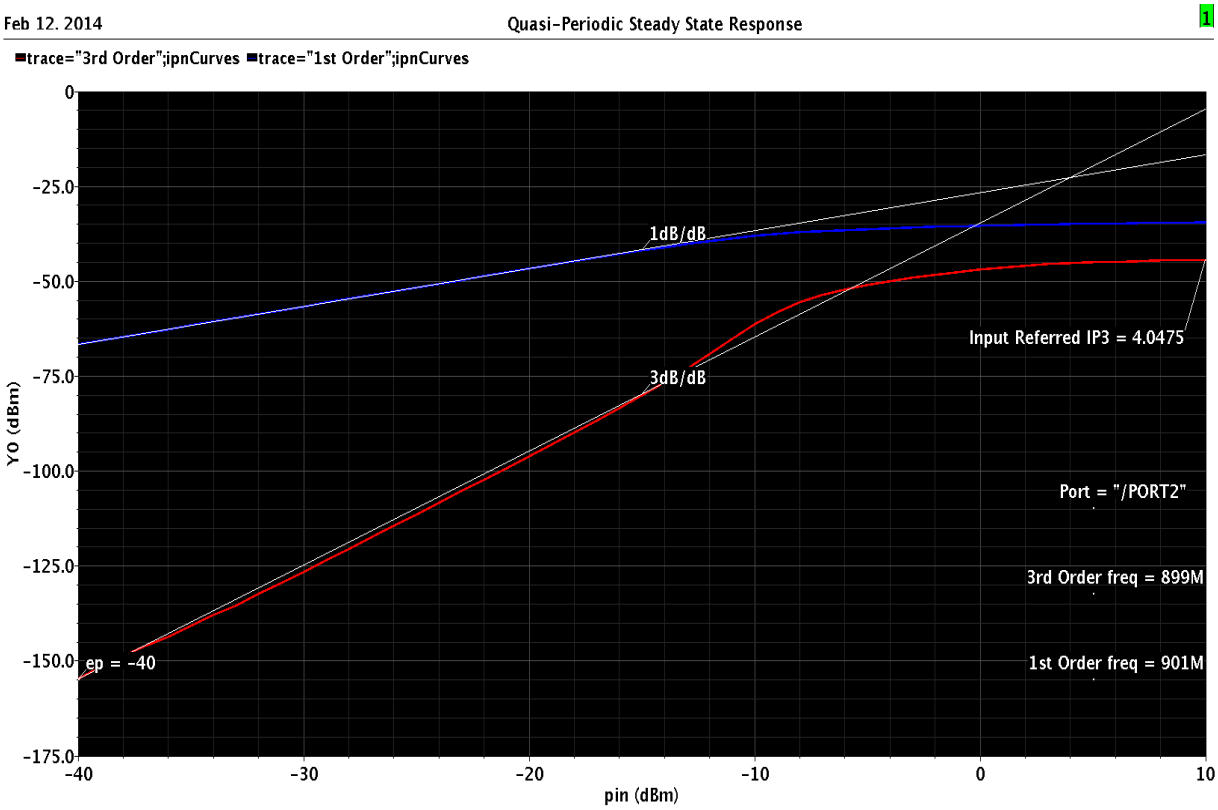

Fig. 21: IIP_3 measurements using qpss analysis

Can you compare the pss+pac results with the qpss results? Which analysis was faster?

It is shown in Razavi’s book (page 26) that $\frac{A_{IIP3}}{A_{1dB}} \approx 9.6dB$. Do you think this is valid for our circuit? In figure 21, do you think the “extrapolated” IIP_3 is close to the real intercept point? Refer to pages 26-29 of the book for further information.