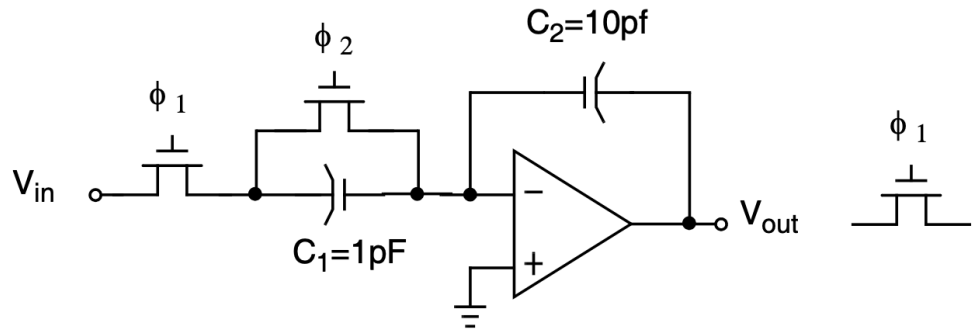
ELEC 501 Analog Integrated Circuit Design
Assignment 1
Nominal Due: Wednesday, February 25th, 2026 at 11:59pm

1. Ignoring parasitic capacitances of the components:

a) Find the discrete-time transfer function of the following switched-capacitor circuit.



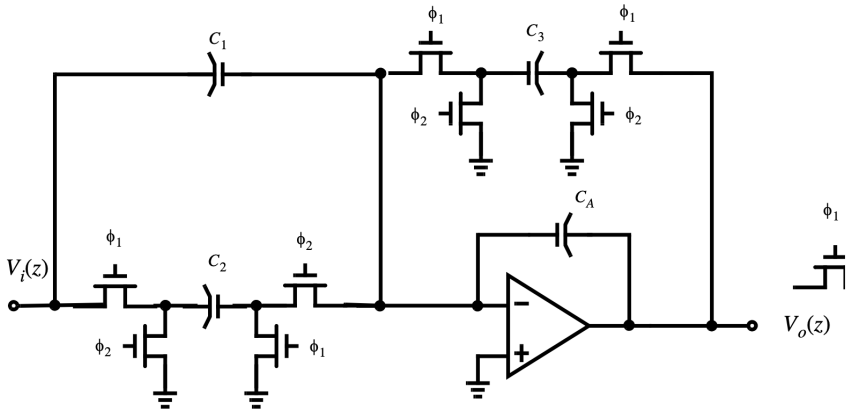
b) Verify that the transfer function that you have derived in part (a) is correct! To do this, use a circuit simulator of your choice to find the impulse response and step response of the circuit. For the purpose of simulation, assume the clock frequency is 200 kHz. Use pulse source functions in your simulator (e.g., PULSE command in HSPICE) to generate the two non-overlapping clocks: Φ_1 and Φ_2 with rise and fall times of 1 ns and pulse width of 2 μs). For simplicity, use the ideal opamp model (e.g., in HSPICE the syntax for ideal opamp is: Ename out+ out- OPAMP in+ in-). Assume simulation time of 200 μs.

Use the following two methods to model each switch:
i) A voltage-controlled resistor with on-resistance of 50 Ω and off-resistance of 5 MΩ
ii) An NMOS transistor in the process of your choice that is sized to have an on-resistance of 50 Ω.

Include the transient responses for input, output, Φ_1 and Φ_2 waveforms for each of the above cases.

c) Briefly discuss why there are some discrepancies (if any) between the simulation results in part (b) and the corresponding respond using the calculated transfer function in part (a).

2. For the following circuit:



a) Find the discrete-time transfer function.
b) Explain which of the clock signals should be advanced in order to reduce the effects of charge injection.
c) Draw the schematic of a fully differential implementation of the circuit where it is desired to realize a negative value for the capacitance C_2.

Good luck!