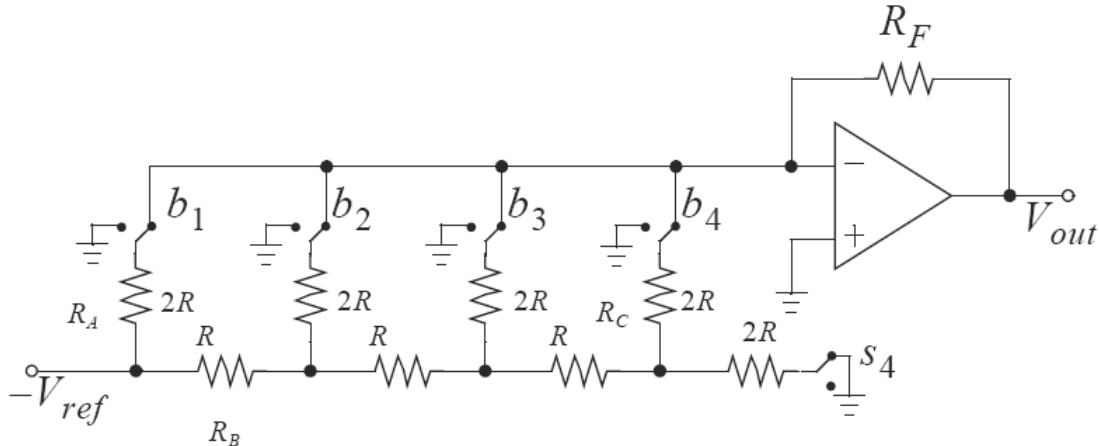


ELEC 501 Analog Integrated Circuit Design
Assignment #2
Nominal Due: Wednesday April 1, 2026 at 11:59pm

1. In the following R-2R-based DAC,



- a) What is the output error (in LSBs) when $R_A=2.01R$? What is the output error when $R_C=2.01R$? Based on your result, the precision of which resistor (R_A or R_C) is more important?
 - b) Assume that all switches in the above circuit are MOSFETs and are scaled such that their on resistance is much smaller than R , however, they each have an 80mV voltage drop across them (their drain to source) when on. What would the effect of this non-ideality on the accuracy of the converter?
2. A 12-bit binary-weighted DAC produces a glitch voltage of 0.4V when its MSB is changed. What would be this glitch voltage if a thermometer-code approach is used for the top 4 bits, whereas binary-weighting is used for the remaining 8 bits.
 3. Assuming the input capacitance of a differential stage (and/or comparator) is the same in either a flash or folding/interpolating ADC, what reduction of input capacitance over a flash converter would be achieved if an 8-bit folding/interpolating ADC having 4 folding blocks, each with a folding rate of 8 is used? If a straight interpolating ADC is to have the same reduction in input capacitance (as compared to an 8-bit flash ADC), how many resistors are required between each two consecutive input comparators.
 4. Find an expression for the number of latches in an N-bit folding A/D converter whether the folding rate is $FR=2^m$ (m is an positive integer number).
 5. Explain whether or not:
 - a) an 8-bit ADC can have a worst-case DNL of 1.2LSB
 - b) a 12-bit ADC can have $-0.5\text{LSB} < \text{DNL} < +0.5\text{LSB}$ and $-0.2\text{LSB} < \text{INL} < +0.2\text{LSB}$

6. You are to realize a third-order MASH by cascading three first-order stages as shown in the following block diagram. The second and third stages accept as their inputs the quantization errors of the previous stages, namely, $e_1(n)$ and $e_2(n)$. Assuming all of the discrete-time integrators in the first-order modulator are ideal, find the digital filters H_1 , H_2 , and H_3 so that the overall MASH output, y , includes only the input signal u (or the delayed version of it) and the third-order shaped quantization noise.

