ELEC 501: Analog Integrated Circuit Design

Substrate Noise

Shahriar Mirabbasi

Department of Electrical and Computer Engineering
University of British Columbia
shahriar@ece.ubc.ca

Technical contributions of Mohammad Hekmat are greatly acknowledged.

Single-Chip versus Multi-Chip Solutions

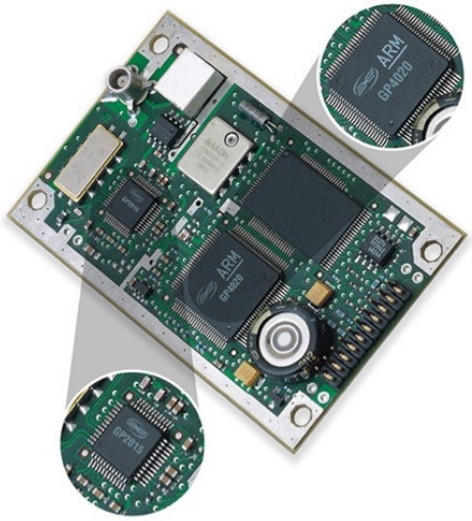
- Multi-chip solutions:

+Less susceptible to substrate noise

+ May use different technologies

- Increased cost and power

- Board level signal integrity issues



GP2015 & GP4020 on a CMC Electronics Superstar II OEM GPS Receiver

(CMC Electronics products available from http://www.cmcelectronics.ca/)

- Single-chip solutions:

+ Small size

+ Low cost

+ Low power

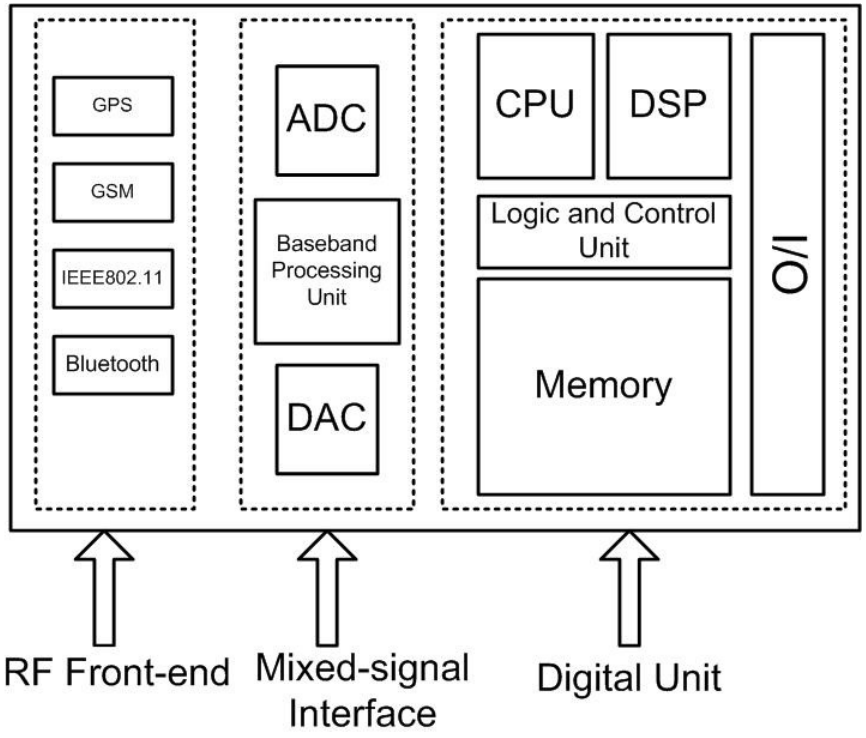
- Chip level signal integrity issues

Courtesy of STMicroelectronics

Example of a System

Multi-standard Wireless Device:

+ Small form factor
+ Convenient
+ Low cost
- Interference from other standards
- Need for broadband circuits



Multi-standard Radio SoCs

Substrate Noise

In mixed-signal designs

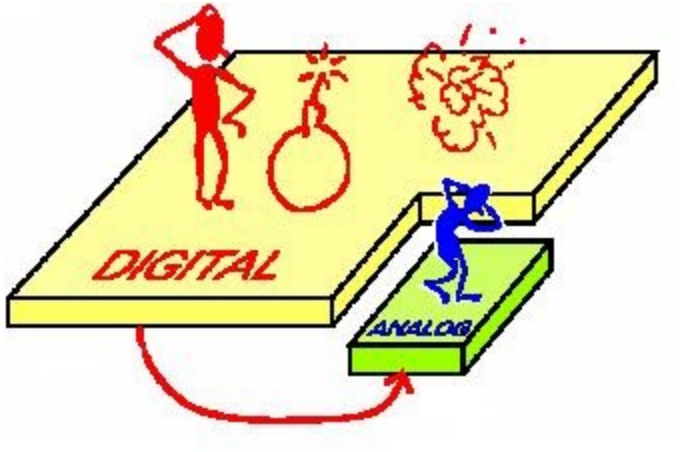
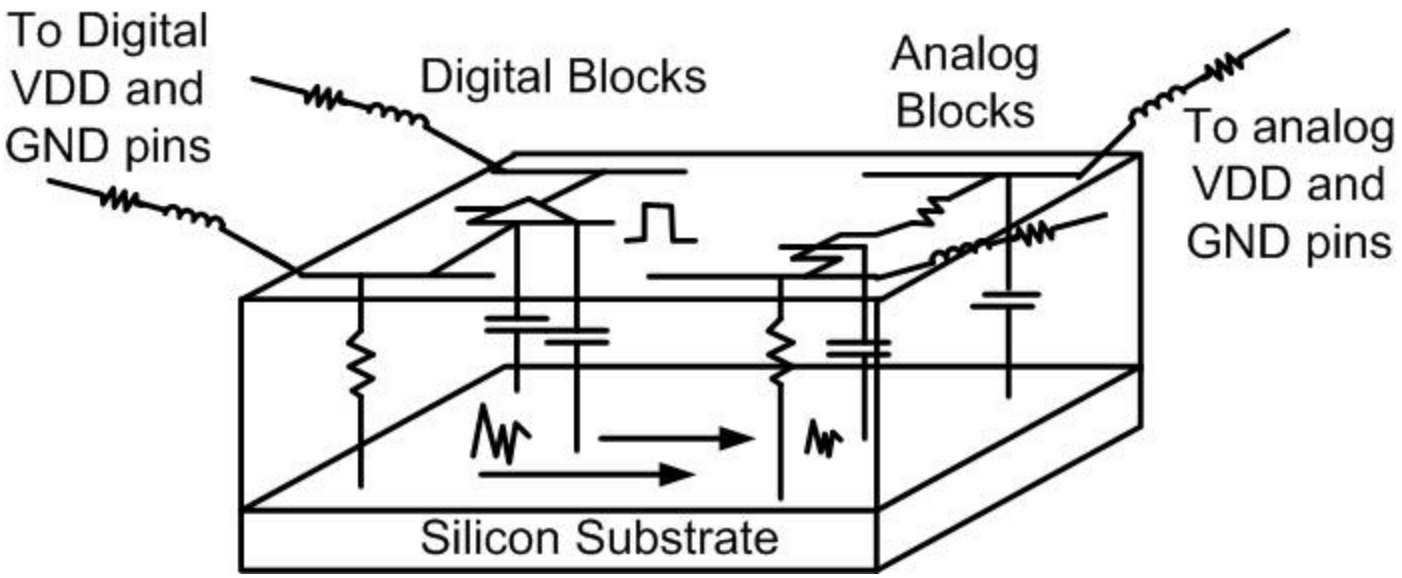


Figure courtesy of IMEC, Belgium

Substrate Noise

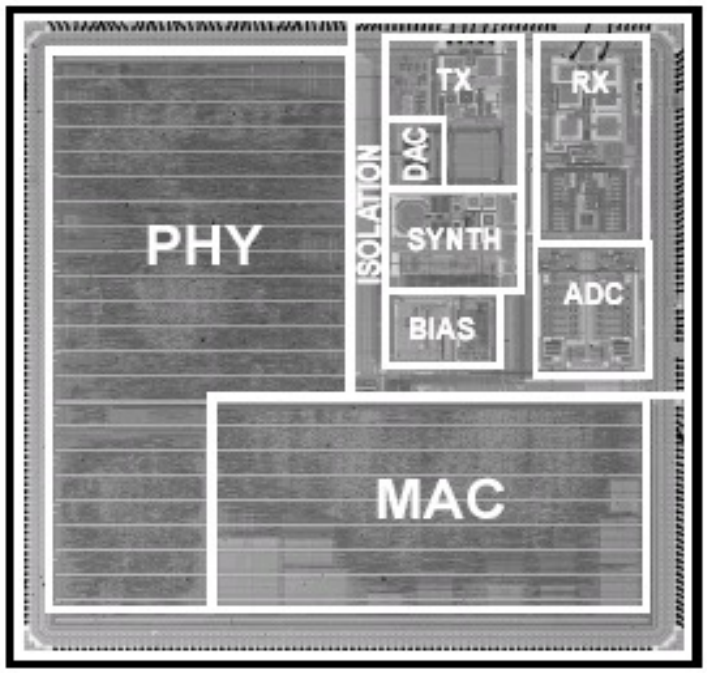
- All circuit blocks residing on a chip share the same substrate.
- Substrate perturbations are picked up by all the circuit elements.
- Digital circuits, contribute to both substrate and supply noise.
- Analog blocks are typically very sensitive to such noise.
- By proper design, the effects of noise can be reduced



Is it really important?

CMOS Example

IEEE802.11g WLAN SoC in 0.18μm CMOS

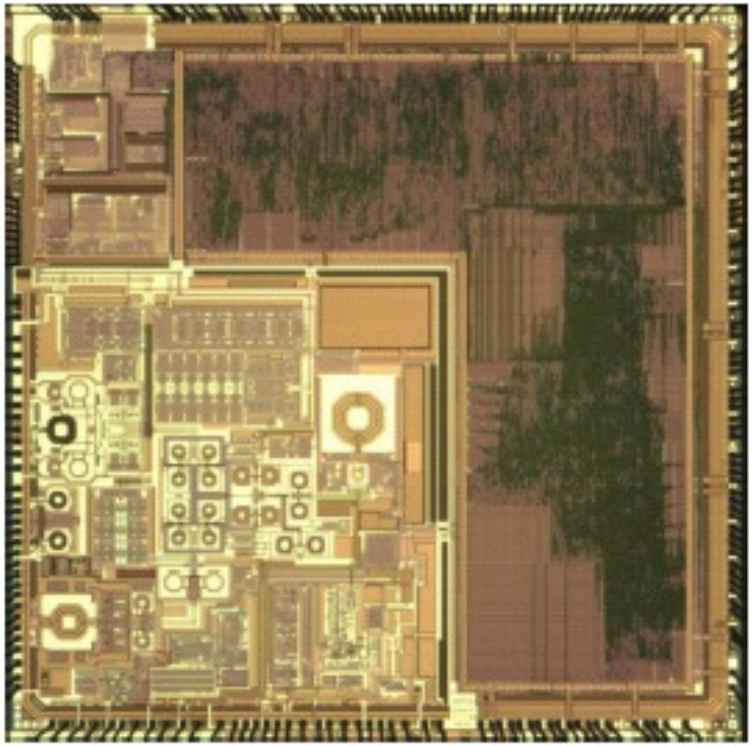


S. Mehta, et al. ISSCC05

- Fully differential analog and RF circuits
- Multiple supplies
- On-chip voltage regulators for more sensitive circuits
- deep N-well trench of 150μm

CMOS Example

IEEE802.11b WLAN SoC in 0.18μm CMOS



H. Darabi, et al. ISSCC05

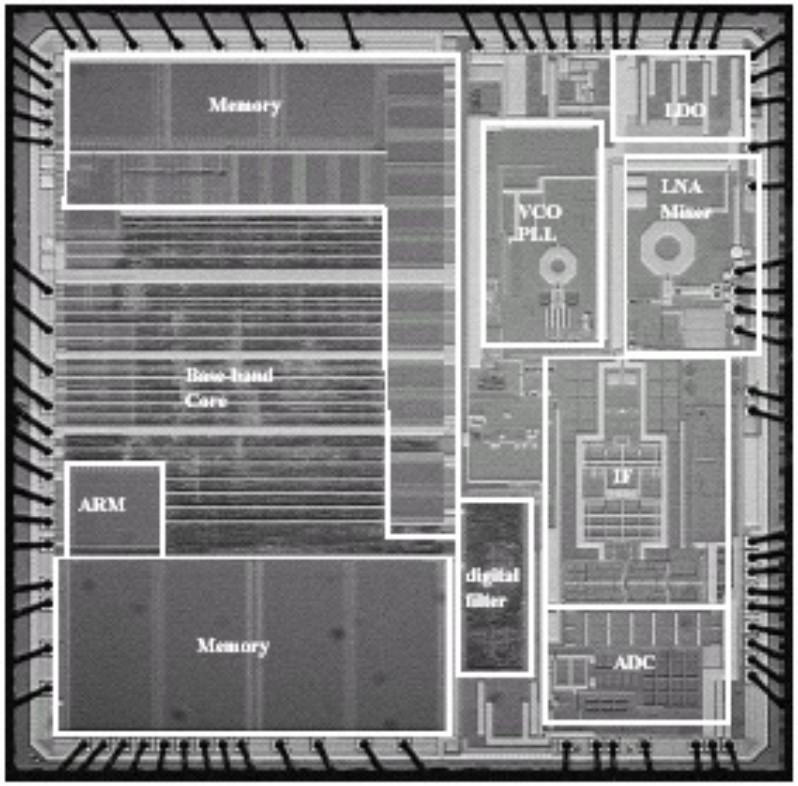
Physical Separation

Careful placement of blocks

Adding on-chip decoupling capacitance

CMOS Example

Single-Chip GPS in 90 nm CMOS



Use of guard rings

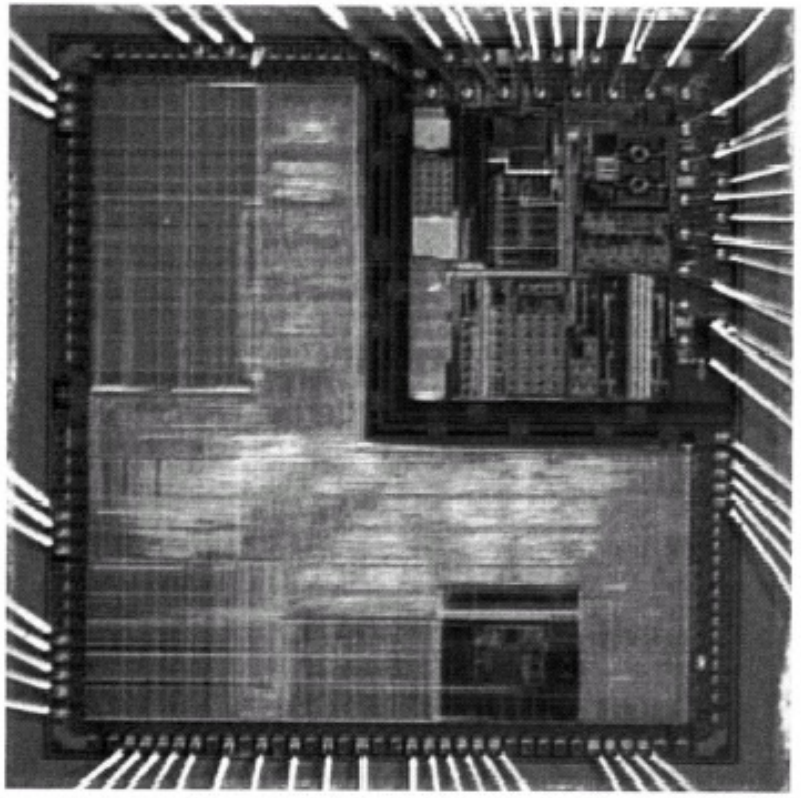
Optimized placement of digital blocks and routing

Reducing switching current in high-speed digital filters

Debapriya Sahu, et al., ISSCC05

CMOS Example

Single-Chip Bluetooth in 0.18 μm CMOS



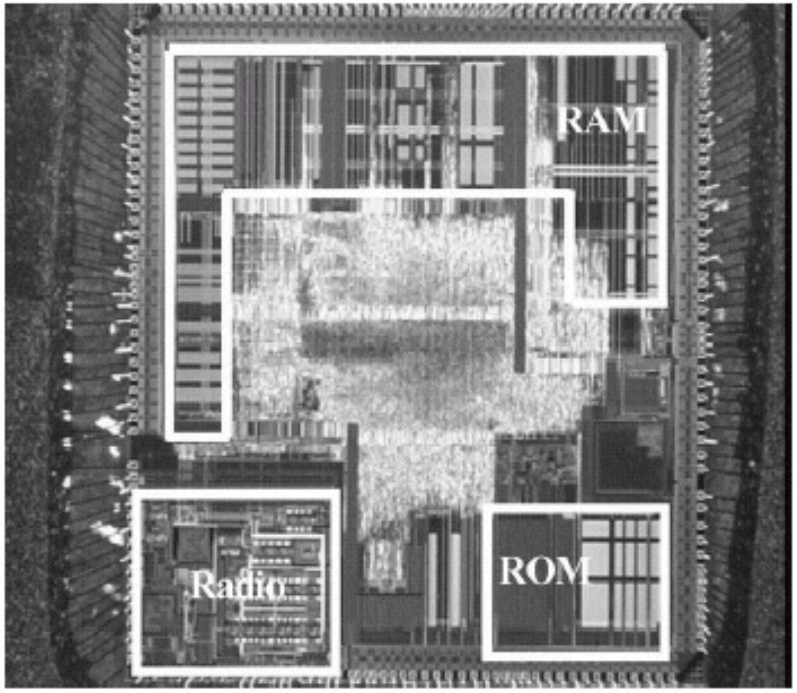
Isolation of RF blocks by using a 300μm width p+ guard ring

Multiple supplies (5 for digital, 5 for analog have been used)

P. Van Zeijl, et al. (ISSCC01, JSSC02)

CMOS Example

Single-Chip GPS in 0.18 μm CMOS



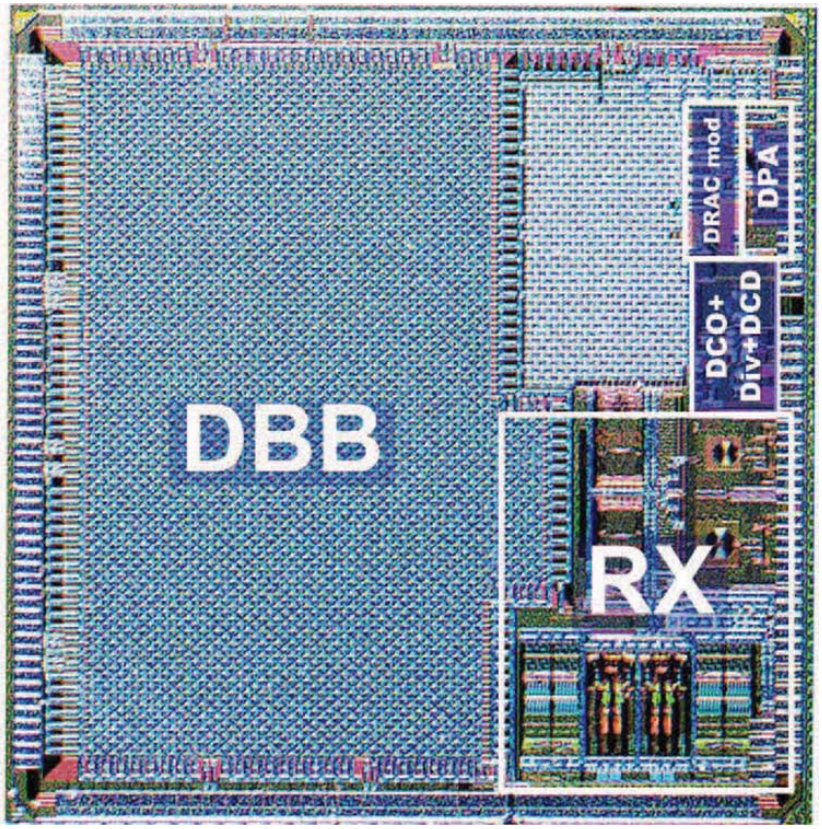
Deep n-well to increase isolation

Multiple guard rings around sensitive parts and the whole radio

Kadoyama et al. (VLSI03, JSSC04)

CMOS Example

65 nm CMOS GSM/GPRS/EDGE SoC



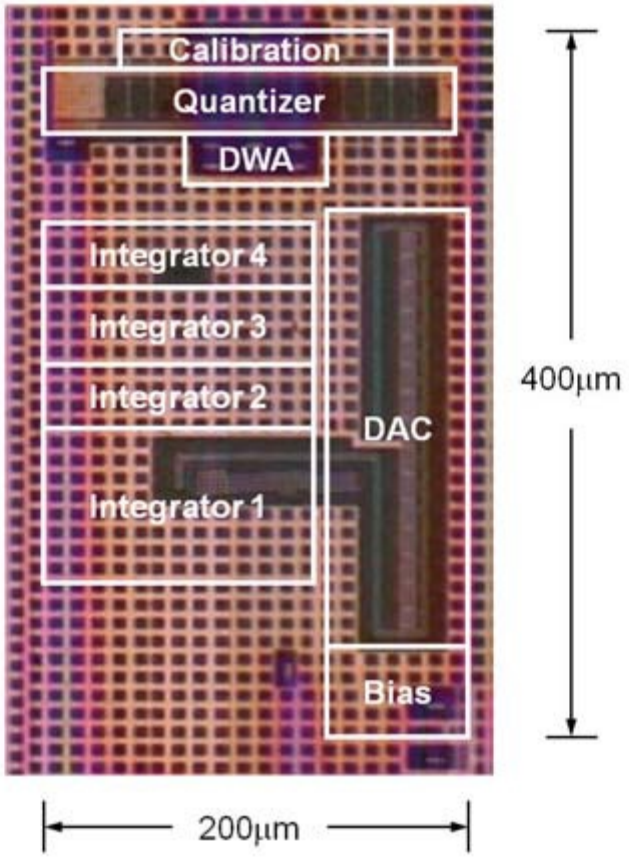
Previous techniques +

Digital signal processing techniques

I. Bashir, et al. JSSC 11

CMOS Example

- Continuous-Time Delta-Sigma Modulator in 28 nm CMOS

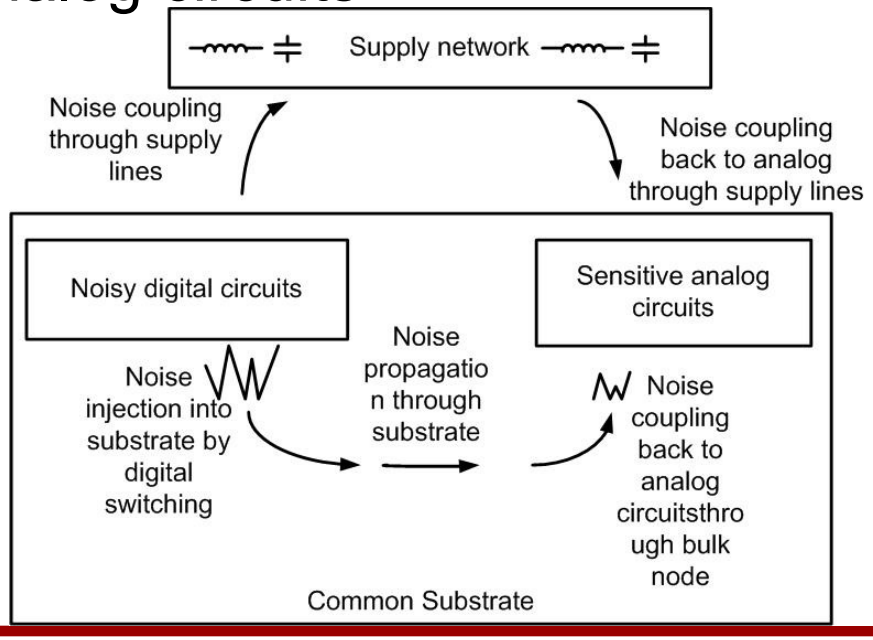


Y.-S. Shu et al., ISSCC 2013

Substrate Noise Coupling

- The process can be broken down into three steps:

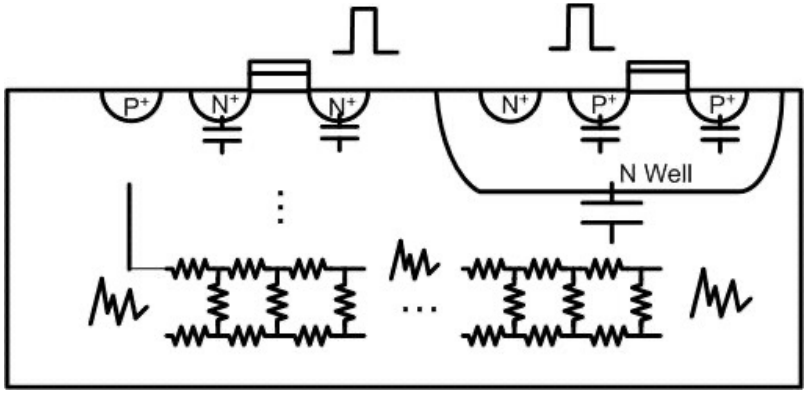
1. Generation of noise (or injection into the substrate and/or supply)
2. Propagation through the substrate
3. Coupling to analog circuits



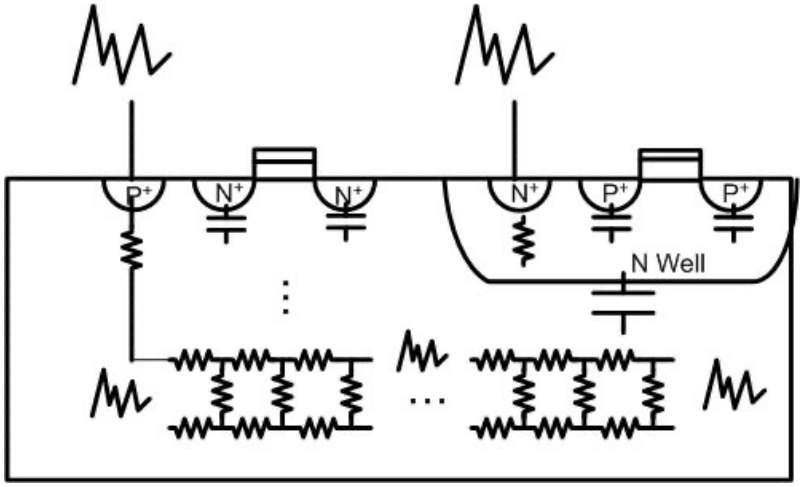
Major Mechanisms

- Two major mechanisms:

1. Capacitive coupling



2. Coupling through substrate contacts



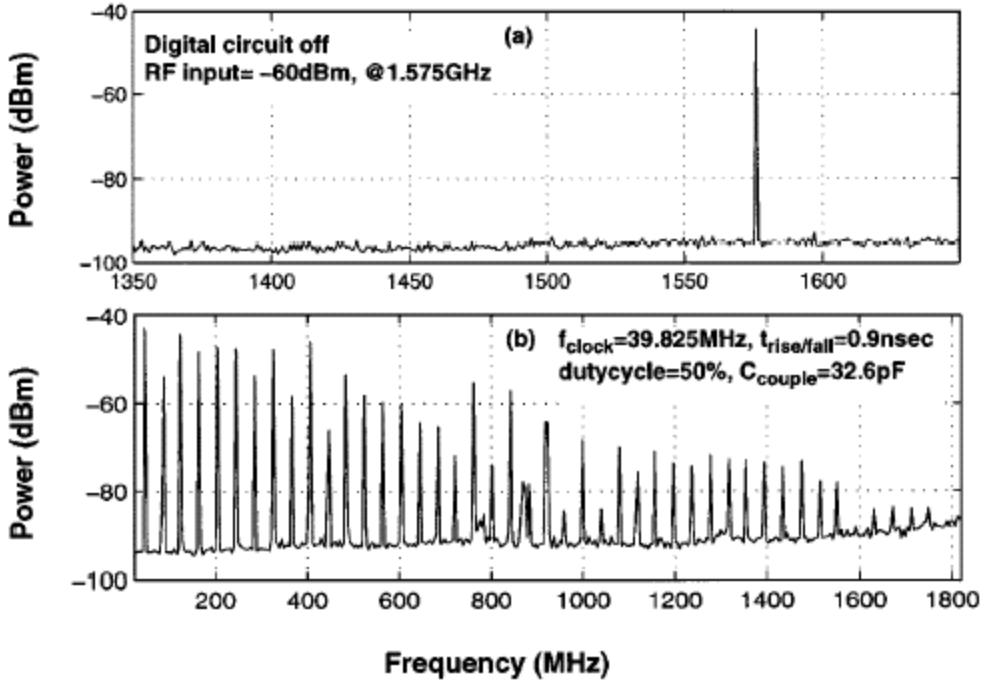
Effects of Substrate Noise

- In Digital Circuits:
- False switching
- Delay variation
- Reduced noise margin

- In Analog Circuits:
- Increased jitter
- Increased noise figure
- Reduced resolution (of ADCs).

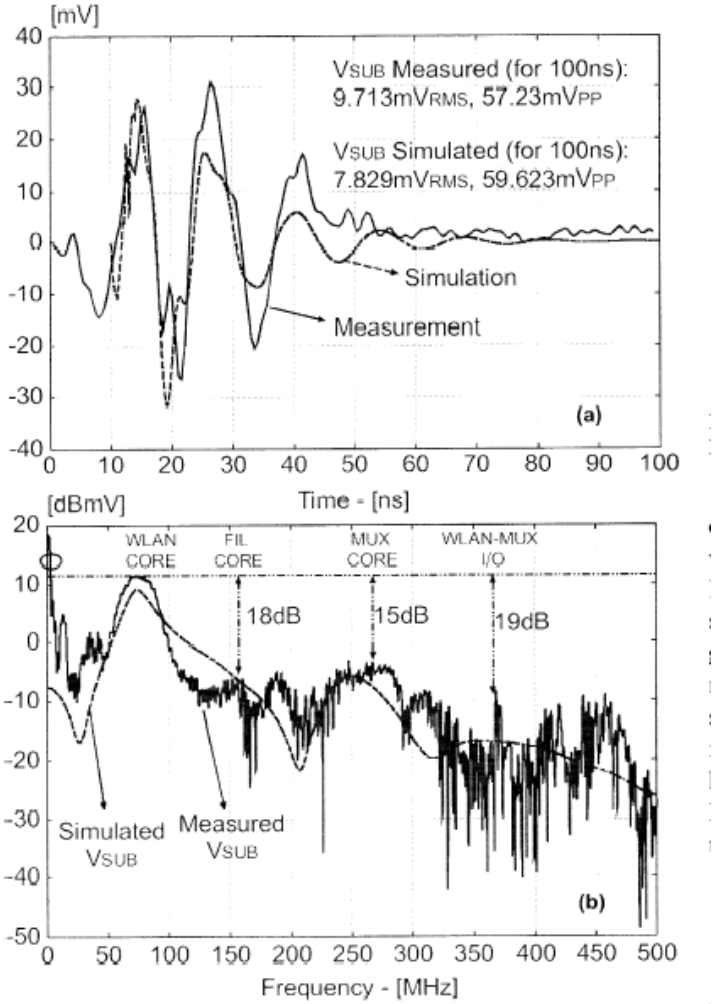
Noise in Frequency Domain

Strong noise components at the harmonics of clock, therefore, careful frequency planning is required



Measured output spectrum of a GPS LNA with digital circuits off and on (Xu, et al. [1])

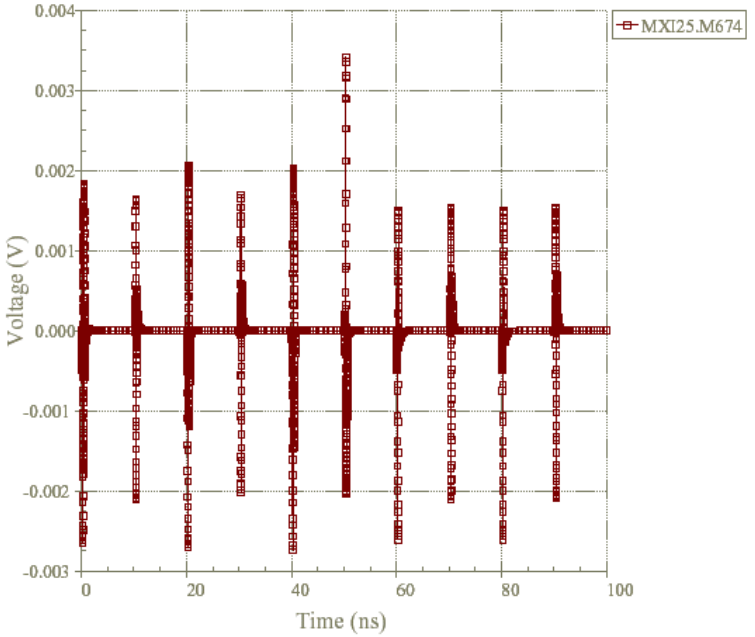
Noise in a SoC

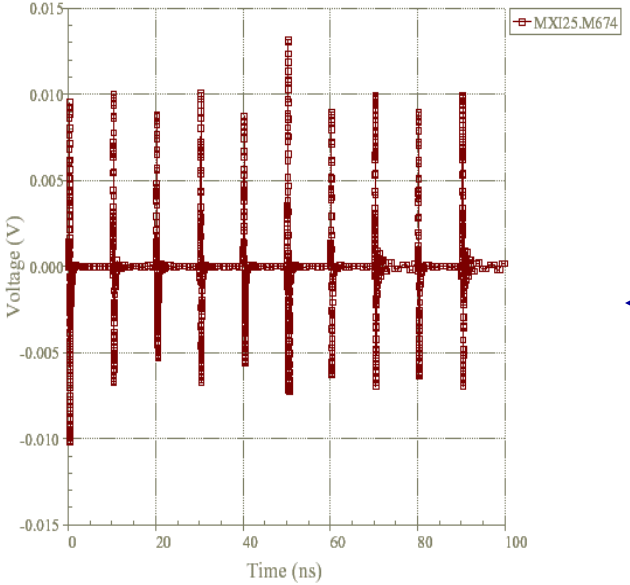


Substrate voltage in time and frequency domain in a 220kGate WLAN SoC (Badaroglu, et al. [2])

Package Inductance (Simulation Results)

Bulk node of an analog circuit (without package)





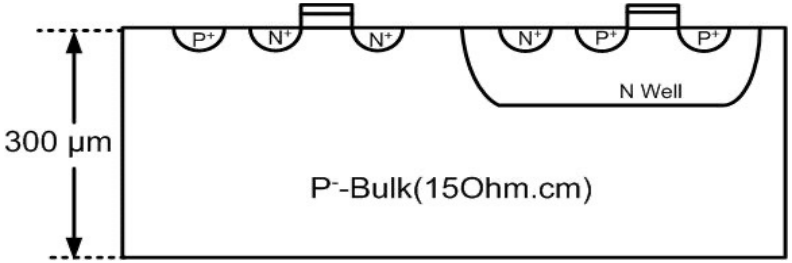
Bulk node of the analog circuit (package with 1nH inductance)

Substrate Types

Bulk Silicon, Silicon on Insulator (SOI), High-resistivity Substrate, Epitaxial Layer, Silicon on Sapphire (SOS)

- Lightly-doped substrate

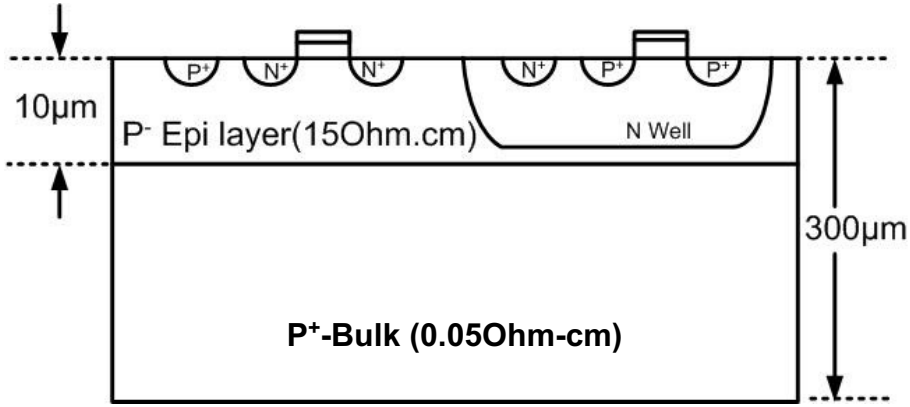
(high-resistivity substrate, 20 to 50Ω·cm)



Lightly-doped substrate

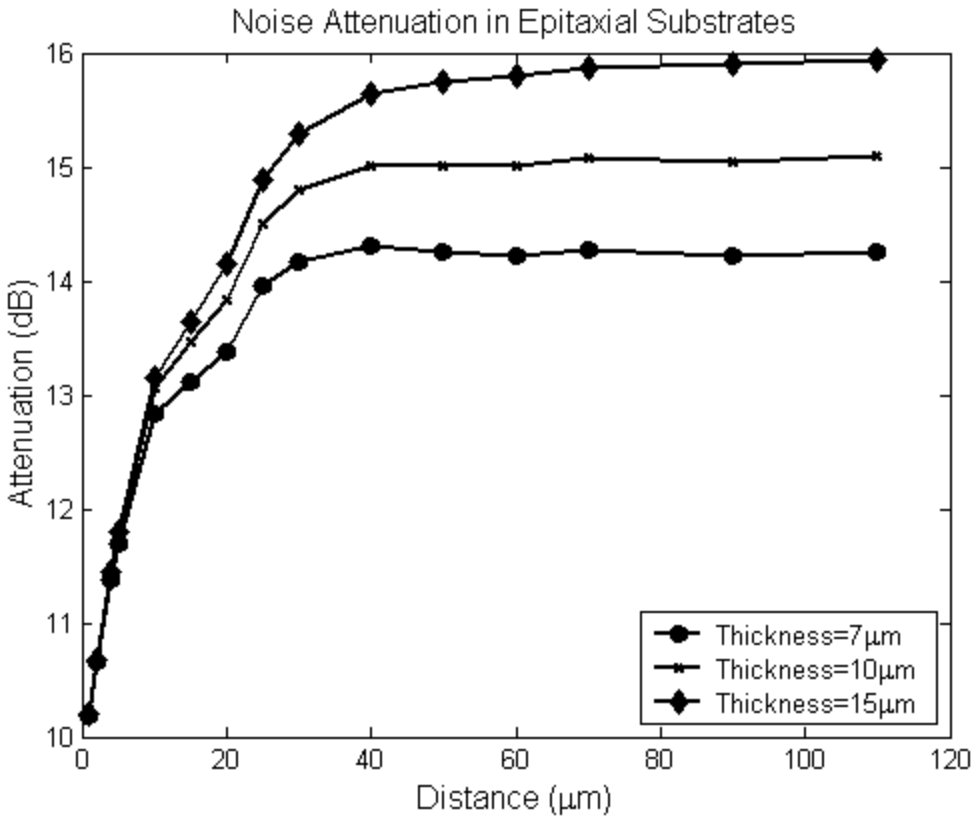
- Epitaxial substrate on top of a heavily doped bulk

(10 to 15Ω·cm on top of 1 to 50mΩ·cm)



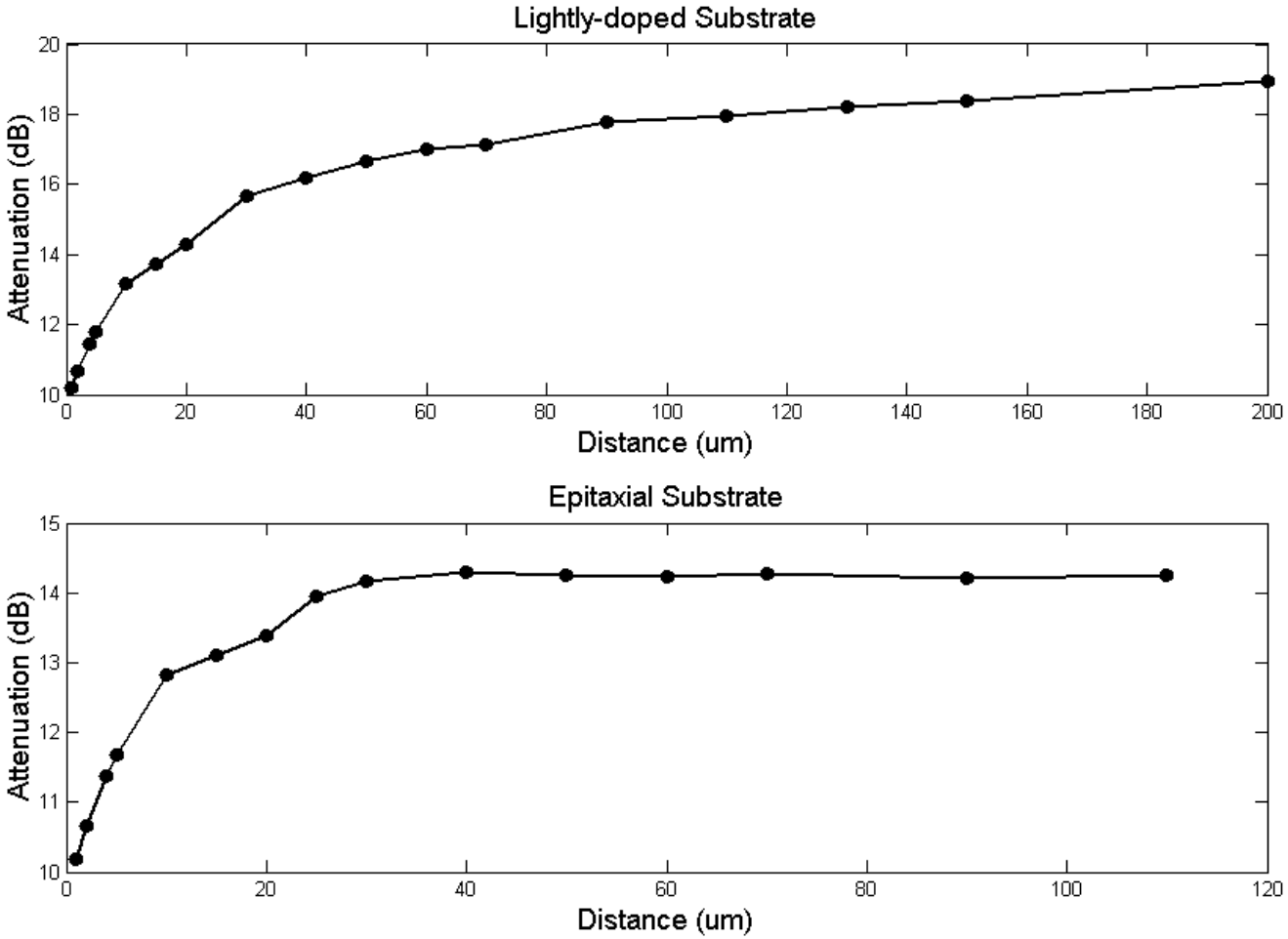
Epitaxial substrate

Effects of the Thickness of Epi Layer



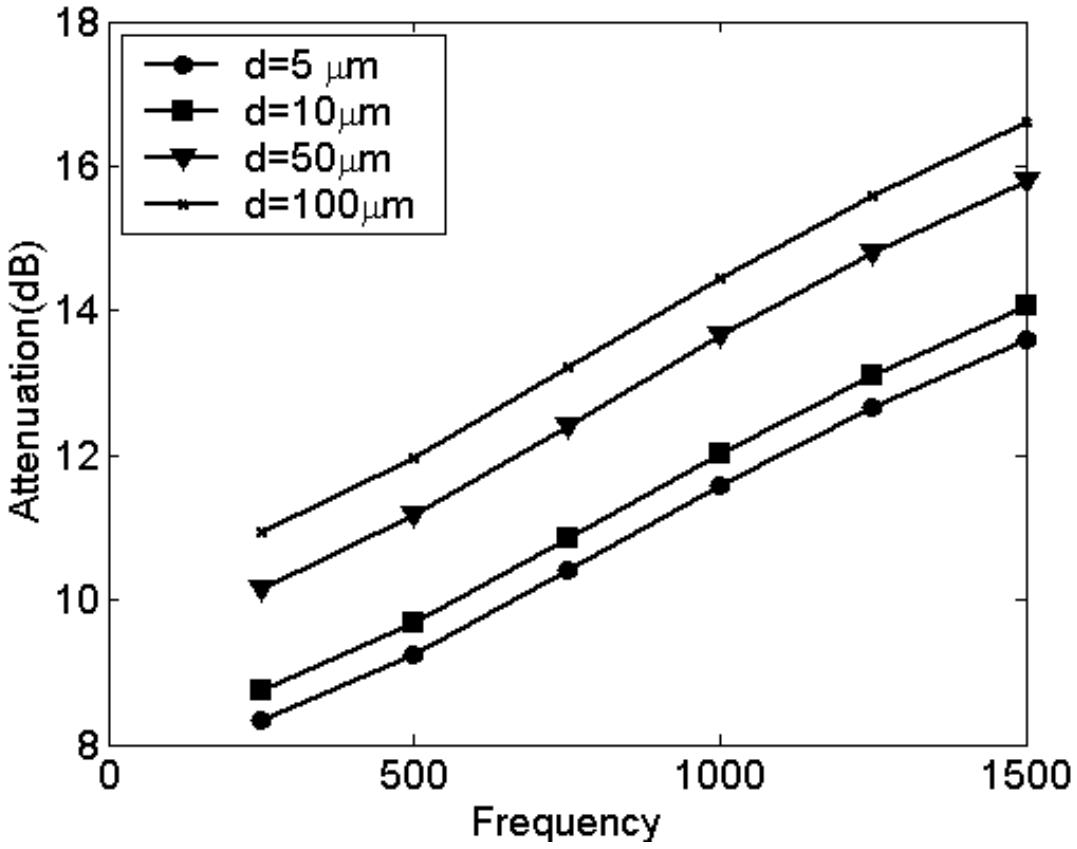
Attenuation vs. Thickness of the epi layer

Physical Separation



Effect of physical separation on noise attenuation depends on the type of substrate

Effect of Frequency



Seems that at higher frequencies attenuation is increased!.

On-chip Isolation Techniques

- Exotic technologies such as SOI
  - Reality: isolation is limited and depends on the frequency
- Guard rings
  - Effectiveness highly depends on the type of the substrate
- On-chip decoupling capacitance
  - Requires careful design and placement
- Multiple supplies for the chip
  - Number of supply pins

Common practice: overdesign (separation, guard-rings, …)

How to Simulate?

- BSIM3 (Berkeley Short-channel IGFET Model) and low-level SPICE models do not take substrate effects into account
- BSIM4 and beyond (BSIM-BULK, BSIM-IMG, and BSIM-CMG) account for the substrate underneath the device but not the whole substrate
- Complete simulation of the substrate requires precise 3D modeling of the substrate
- The resulting network may be prohibitively large to be included in SPICE simulations

How to Simulate?

- Commercial (and open-source) software packages for substrate noise analysis are available
  - Integrated tools within Cadence: Quantus Substrate Noise Analysis (SNA), Quantus Substrate Surface Noise Distribution (SND) (Virtuoso Studio integrates these extraction and analysis tools into mixed-signal flow)
  - Synopsys: StarRC and Ansys Totem-SE (SE: Substrate Engineering)
  - SWAN (Substrate Waveform Analysis) is another tool but its accuracy is not verified for lightly-doped substrates
  - Device simulators such as MEDICI can also be used but it is too computationally complex to be used in a large chip

Substrate Noise Reduction

- Noise can be reduced at three levels

  - System level

    Use less noise generating schemes and more robust systems

  - Circuit level

    Use of low-noise digital circuits and more robust analog circuits

  - Technology level

    Use technologies with better isolation options

Substrate Noise Reduction (Alternative View)

- Reduction in:
  - Generation
  - Propagation
  - Reception

Noise Generation Reduction

- Use:

  multiple substrate contacts

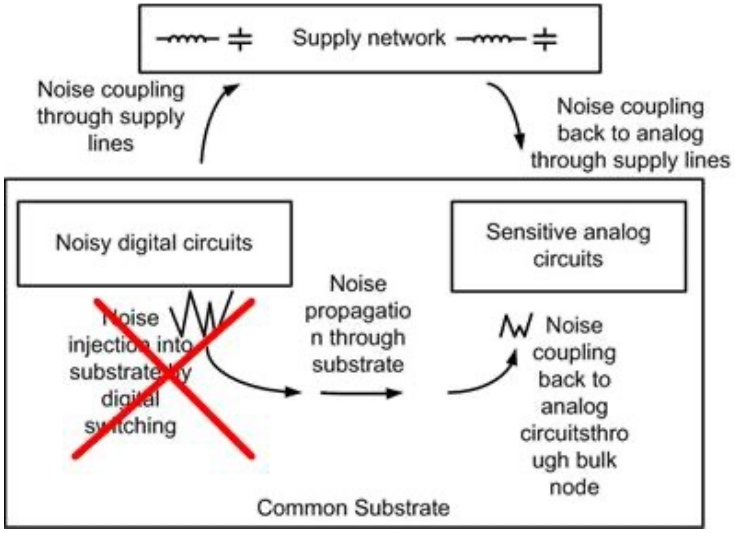
  low-noise digital families such as SCL (source-coupled logic), FSCL (fast source-coupled logic)

  low inductance packages

  Decoupling capacitance

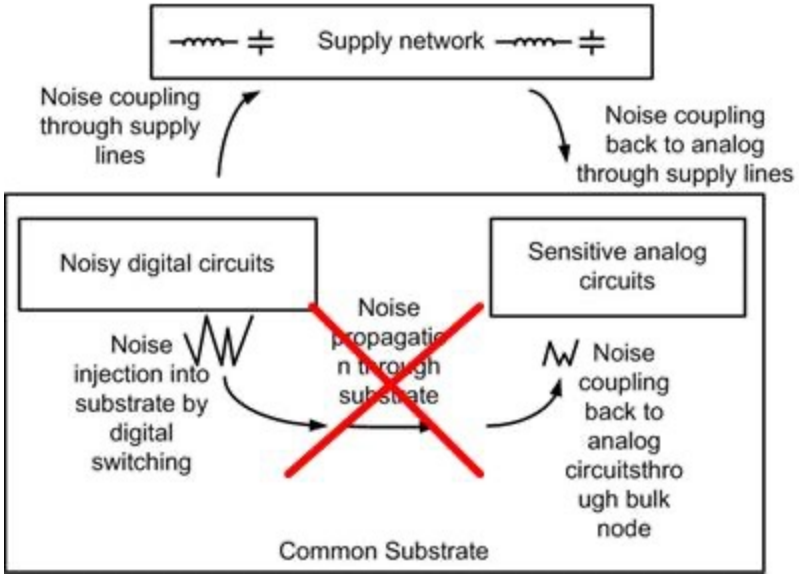
  Switching activity spreading

- Can also leverage low-power design techniques to reduce noise



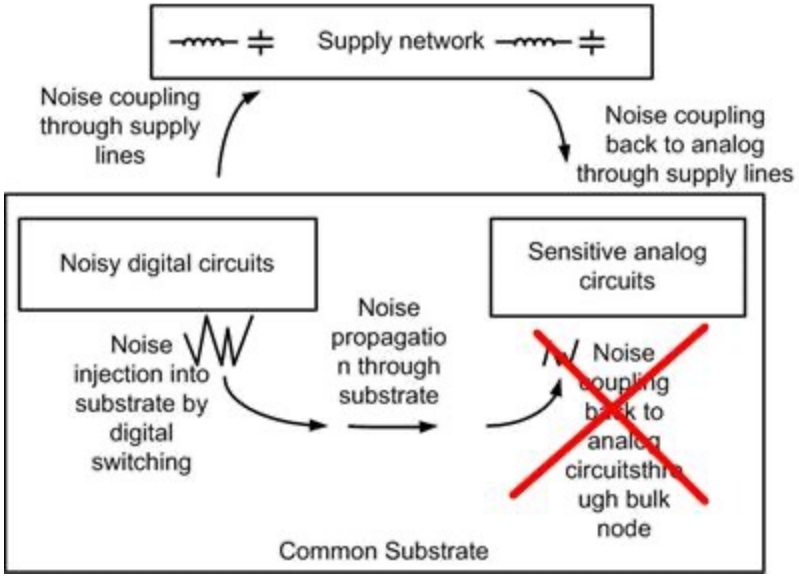
Noise Propagation Reduction

- Proper selection of substrate type
- Use of guard rings (p+ and/or n-well)
- Isolate devices with trenches and buried layers
- Use of exotic technologies such as SOI
- Active noise suppression



Noise Reception Reduction

- Use of differential structures (if possible)
- Careful simulation of the circuit
- Careful layout (increase symmetry)
- Careful routing of signals



References

1. M. Xu, D. K. Su, D. K. Shaeffer, T. H. Lee, and B. A. Wooley, "Measuring and Modeling the Effects of Substrate Noise on the LNA for a CMOS GPS Receiver," *IEEE J. Solid-State Circuits*, vol. 36, Mar. 2001, pp. 473-485.
2. M. Badaroglu, S. Donnay, H. J. De Man, Y. A. Zinzius, G. Gielen, W. Sansen, T. Fonden, and S. Signell, "Modeling and experimental verification of substrate noise Generation in a 220-kgates WLAN System-on-Chip with multiple supplies," *IEEE J. Solid-State Circuits*, vol. 38, Jul. 2003, pp. 1250-1260.
3. P. van Zeijl, J.-W.t. Eikenbroek, P.-P. Vervoort, S. Setty, J. Tangenherg, G. Shipton, E. Kooistra, I.C. Keekstra, D. Belot, K. Visser, E. Bosma, and S.C. Blaakmeer, "A Bluetooth Radio in 0.18um CMOS," *IEEE J. Solid-State Circuits*, vol. 37, Dec. 2002, pp. 1679-1687.
4. T. Kadoyama, N. Suzuki,N. Sasho,H. Iizuka, I. Nagase, H. Usukubo, and M. Katakura, "A Complete Single-Chip GPS Receiver With 1.6-V 24-mW Radio in 0.18um CMOS," *IEEEE J. Solid State Circuits*, vol. 39, pp. 562-568, Apr. 2004.
5. L. Connell, N. Hollenbeck, M. Bushman, D. McCarthy, S. Bergstedt, R. Cieslak, and J. Caldwell, "A CMOS broadband tuner IC," *Digest of Technical Papers IEEEE Solid-State Circuits Conference*, vol. 1, pp. 400-476, Feb. 2002.
6. X. Li et al, "A Single-chip CMOS Front-End Receiver Architecture For Multi-Standard Wireless Applications," *Proc. of IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 374-377, May 2001.
7. I. Bashir, R. B. Staszewski, O. Eliezer, et al., "A novel approach for mitigation of RF oscillator pulling in a polar transmitter," *IEEE J. Solid-State Circuits*, vol. 46, iss. 2, pp. 403-415, Feb. 2011.
8. Y.-S. Yu et al., "A 28fJ/conv-step CT ΔΣ Modulator with 78dB DR and18MHz BW in 28nm CMOS Using a Highly Digital Multibit Quantizer," *ISSCC*, pp. 268-269, Feb. 2013.
9. B. Razavi, *RF Microelectronics*, Prentice Hall, 1998
10. T. H Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd edition, Cambridge Press, 1998.