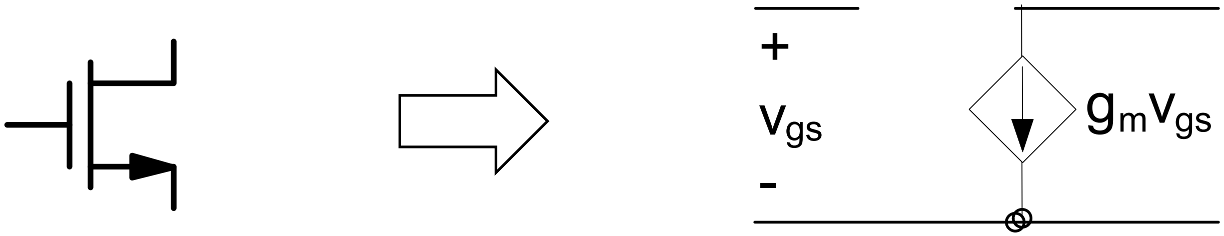
Design Based on g_m/I_D Approach

**Reference: CICC 2008 Educational Session on
Fundamentals of Analog Design,**

**“Design and Optimization of Operational Transconductance
Amplifiers in Fine-line CMOS,” by Boris Murmann**

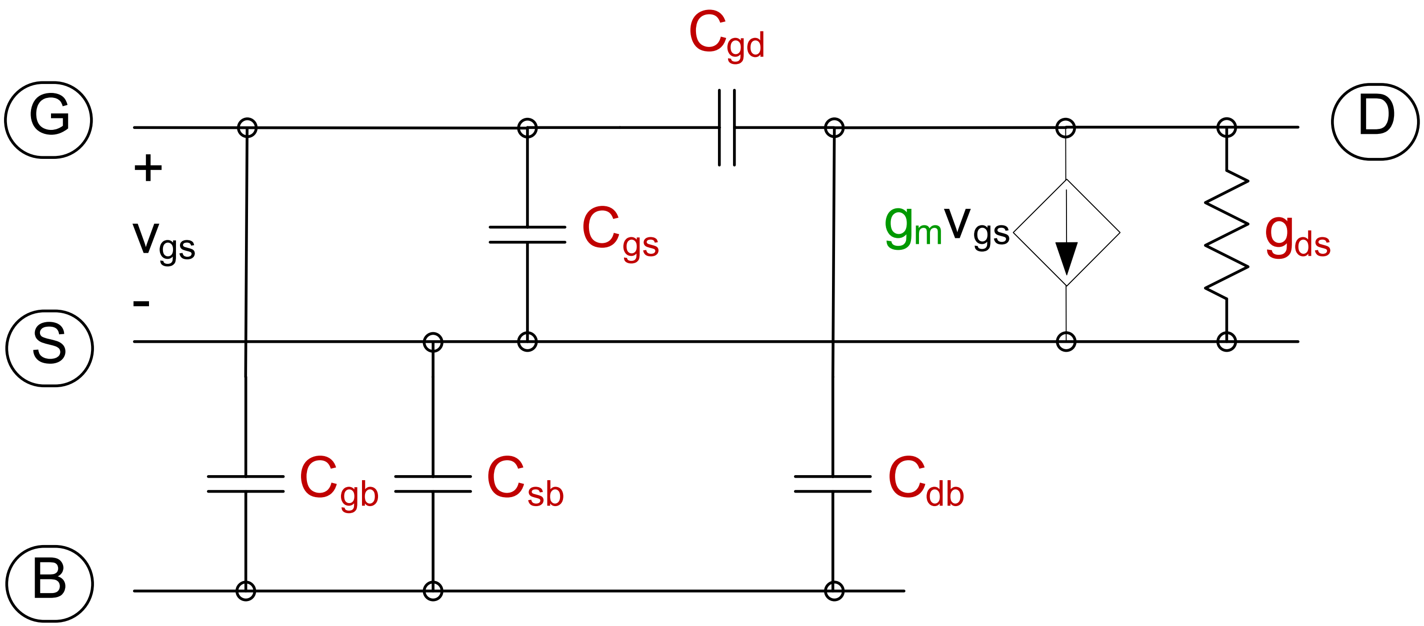
Square Law Model (Saturation Region)



$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right)^2 \qquad g_m = \sqrt{2 I_D \mu C_{ox}\frac{W}{L}} = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}}$$

- Inaccurate for short channel devices or MOS devices biased in moderate to weak inversion

MOSFET Small-Signal Model



$$C_{gg} \overset{\Delta}{=} C_{gs} + C_{gb} + C_{gd} \qquad C_{dd} \overset{\Delta}{=} C_{db} + C_{gd}$$

Basic Figures of Merit

Square Law

- **Transconductance efficiency**
  - large g_m per current

$$\frac{g_m}{I_D} = \frac{2}{V_{OV}}$$

- **Transit frequency**
  - large g_m without large C_{gg}

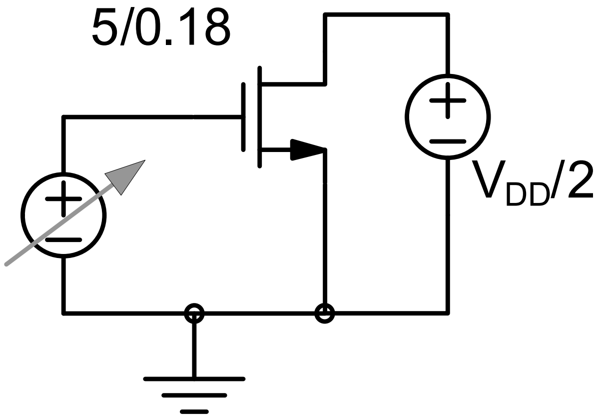
$$\frac{g_m}{C_{gg}} = \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

- **Intrinsic gain**
  - large g_m with small g_{ds}

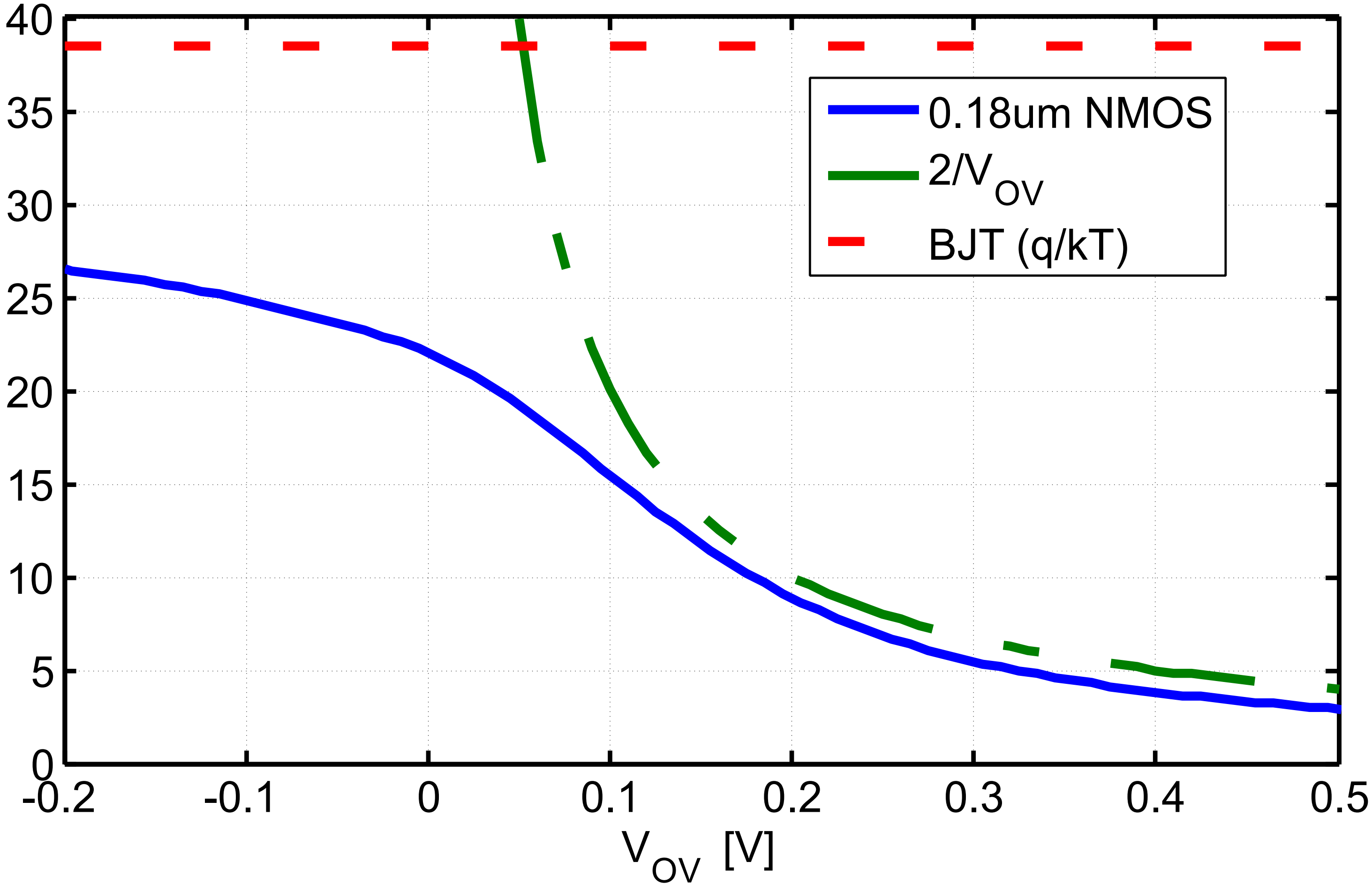
$$\frac{g_m}{g_{ds}} \cong \frac{2}{\lambda V_{OV}}$$

Device Characterization

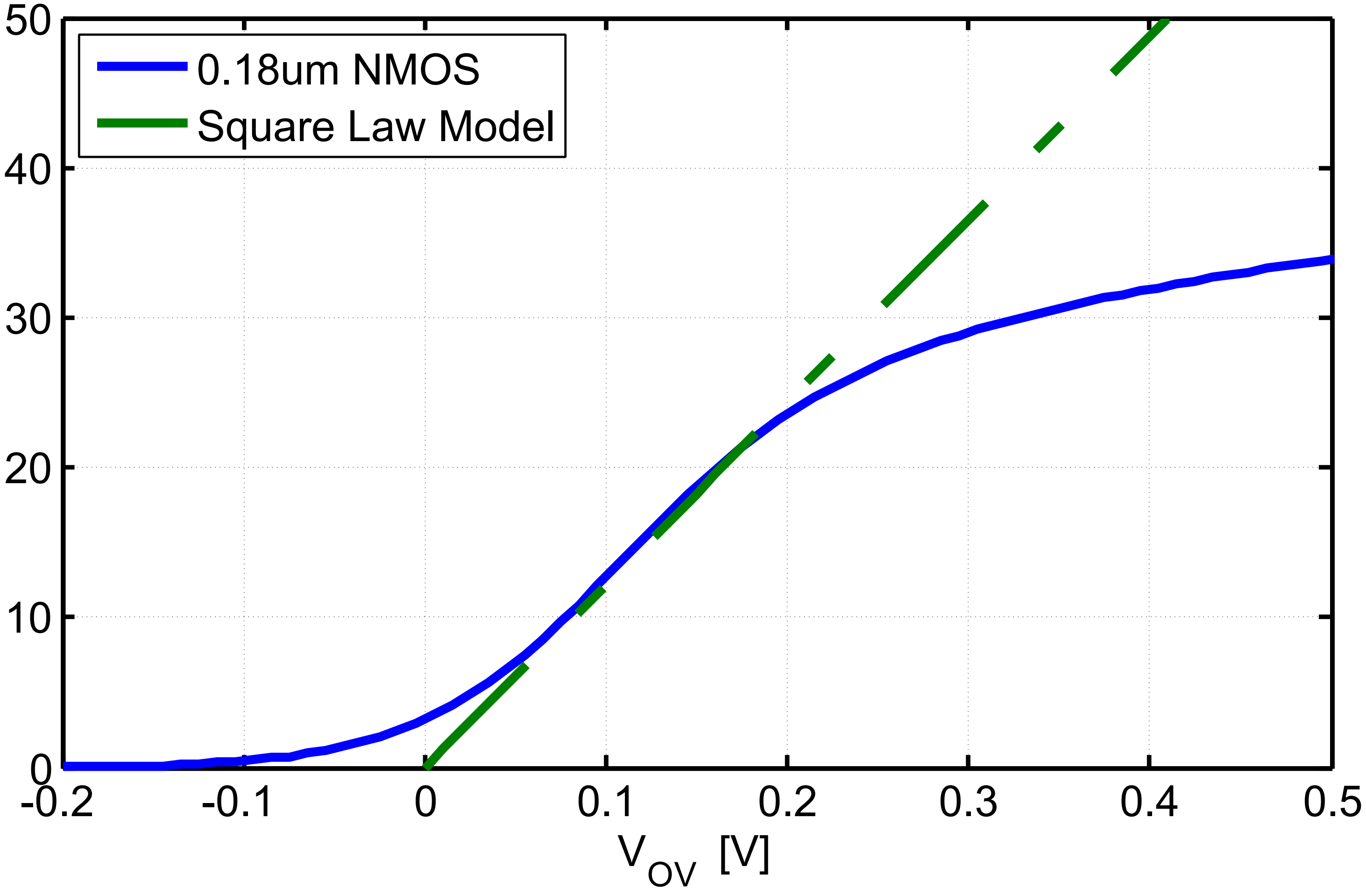
```
* gmid.sp
* NMOS characterization, L=0.18um

.param  gs=0.7
.param  dd=1.8
vds     d 0      dc   'dd/2'
vgs     g 0      dc   'gs'
mn      d g 0 0  nch  L=0.18um  W=5um

.op
.dc gs 0.2V 1V 10mV
.probe ov     = par('gs-vth(mn)')
.probe gm_id  = par('gmo(mn)/i(mn)')
* For BSIM4, use cggbm in the following line
.probe ft     = par('1/6.28*gmo(mn)/cggbo(mn)')
.probe gm_gds = par('gmo(mn)/gdso(mn)')

.options post brief dccap
.inc cmos018.sp
.end
```



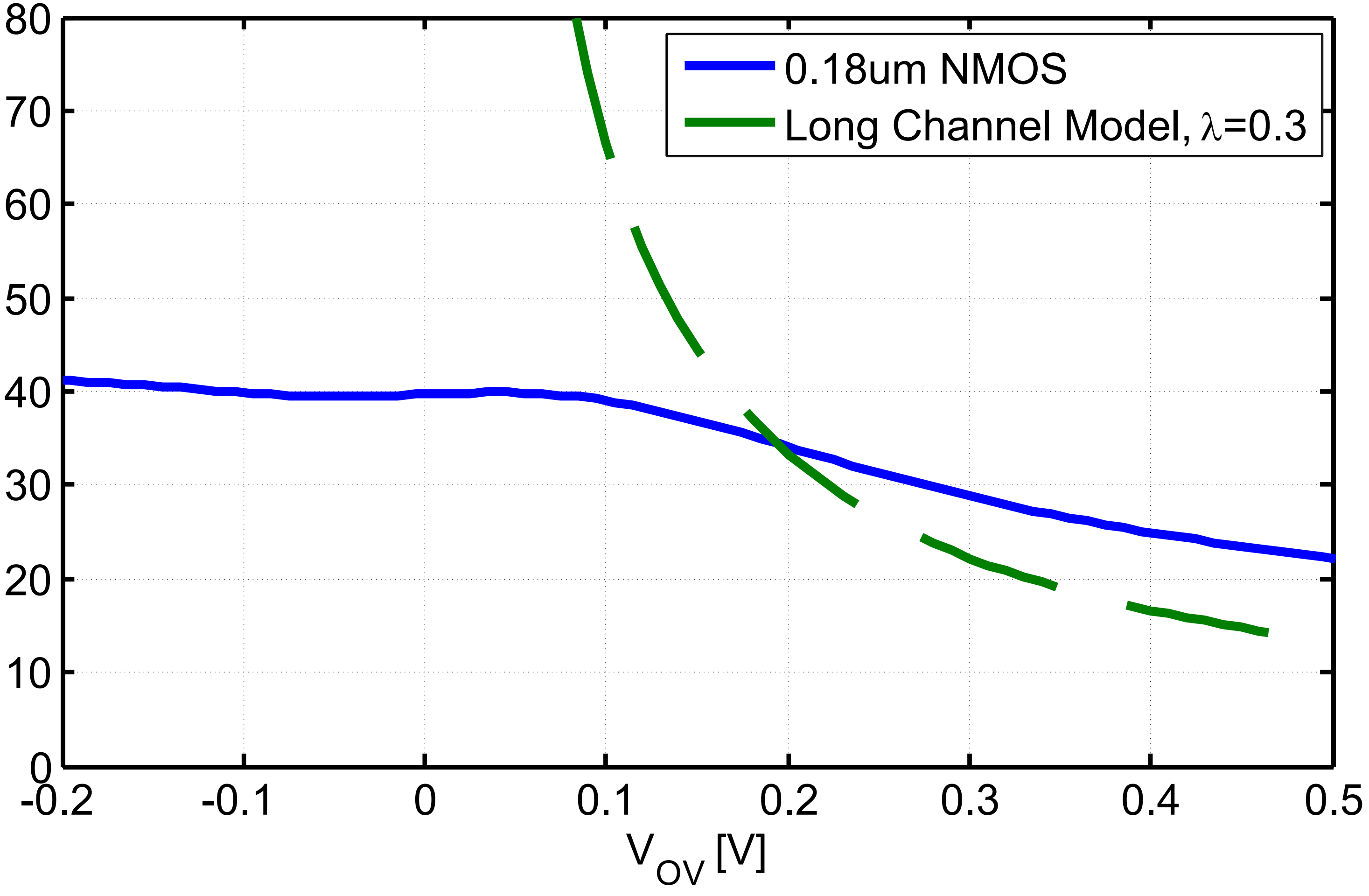
g_m/I_D Plot


40
35
30
25
20
15
10
5
0
-0.2
-0.1
0
0.1
0.2
0.3
0.4
0.5
V_{OV} [V]
0.18um NMOS
$2/V_{OV}$
BJT (q/kT)

Transit Frequency Plot



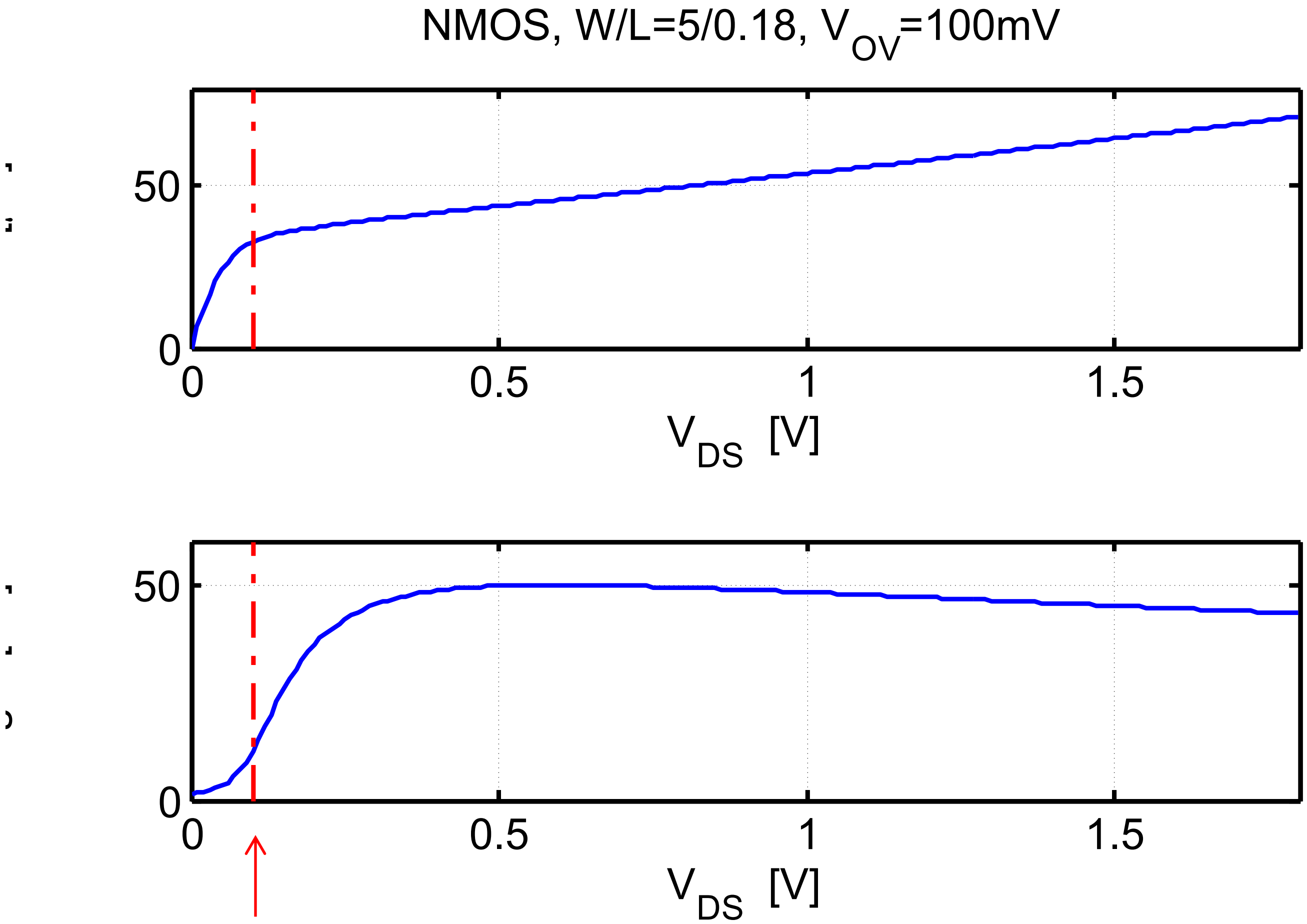
Intrinsic Gain Plot



Replacing V_{OV} with g_m/I_D

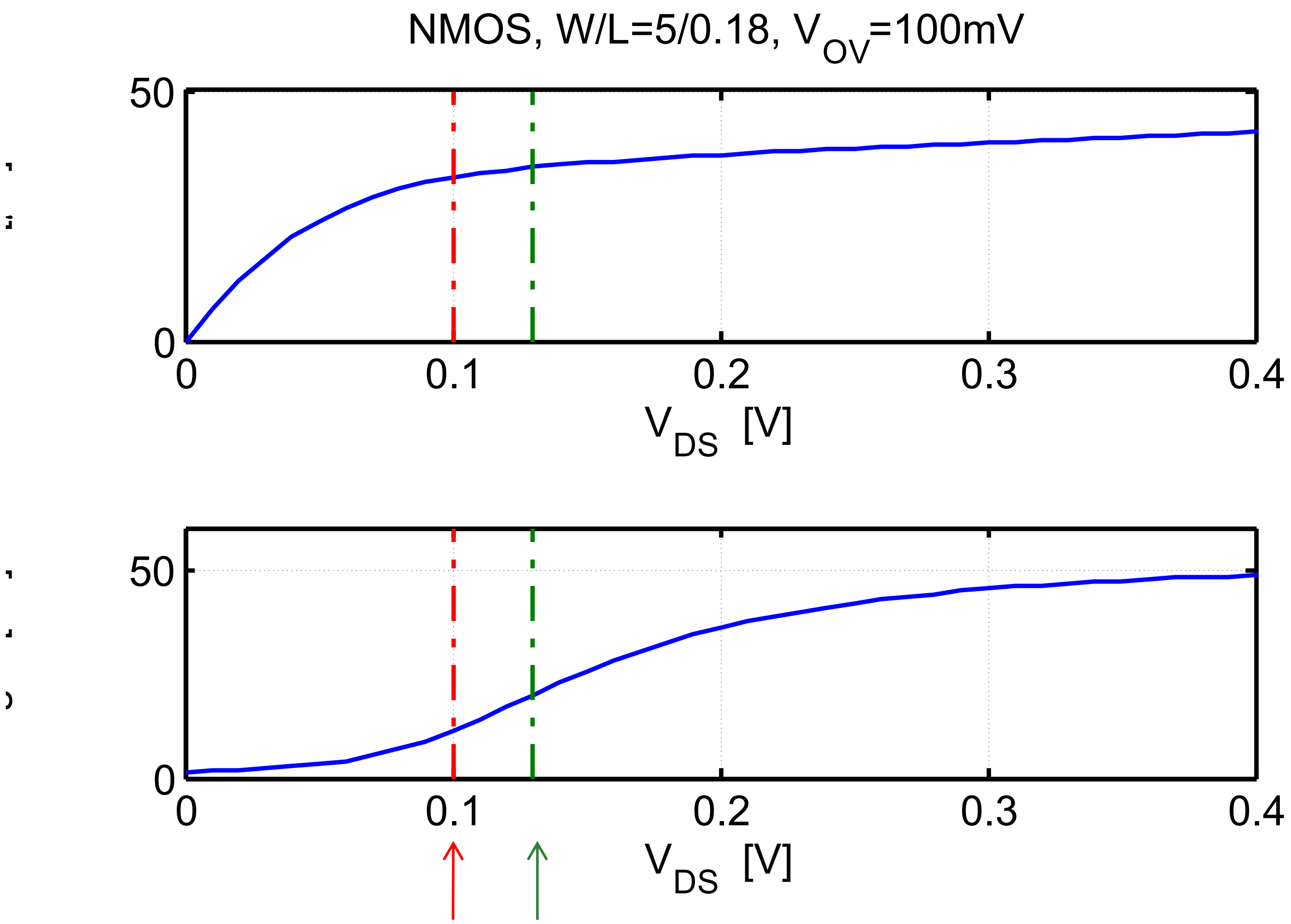
- V_{OV} and in general square law variables (such as μC_{ox}) are not very useful for circuit design in deep-submicron technologies
- Designing based on g_m/I_D is a better choice
  - g_m/I_D has a similar range and behavior over different technologies
  - has useful design information
- How about V_{OV} or V_{DSsat}?
  - $V_{DSsat} = V_{OV}$ defines the onset of saturation in square law model
    - It is used for swing and headroom calculations

Onset of Saturation


NMOS, W/L=5/0.18, V_{OV}=100mV

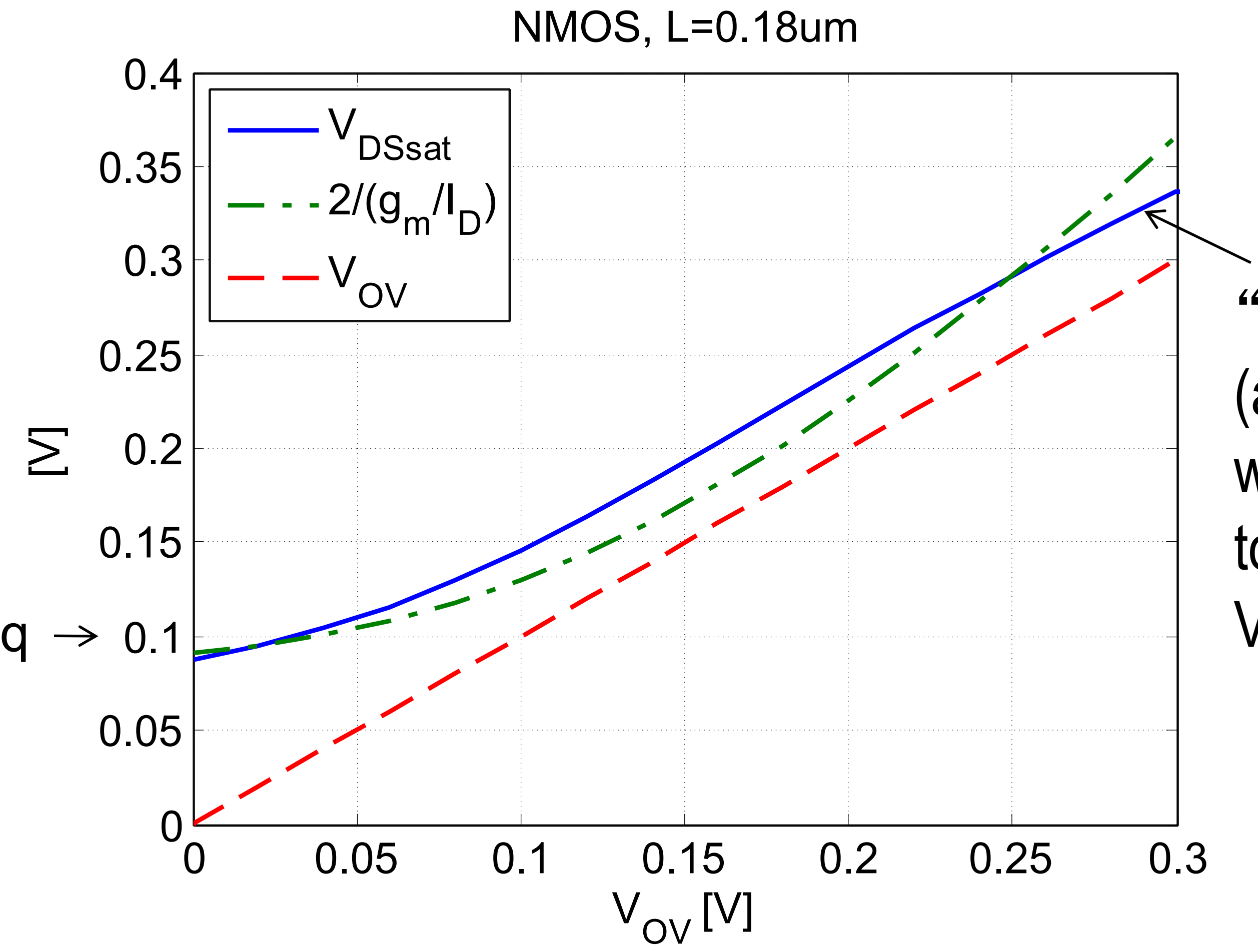
$V_{DS} = V_{OV}$

Onset of Saturation (Zoom)


NMOS, W/L=5/0.18, V_{OV}=100mV

$V_{DS} = V_{OV}$ $V_{DS} = 2/(g_m/I_D)$

V_{DSsat} Estimate Based on g_m/I_D



~4kT/q →

" V_{DSsat} " defined (arbitrarily) as V_{DS} at which $1/g_{ds}$ is equal to ½ of the value at $V_{DS} = V_{DD}/2$

- $2/(g_m/I_D)$ is a reasonable estimate of "V_{DSsat}"

Design Charts

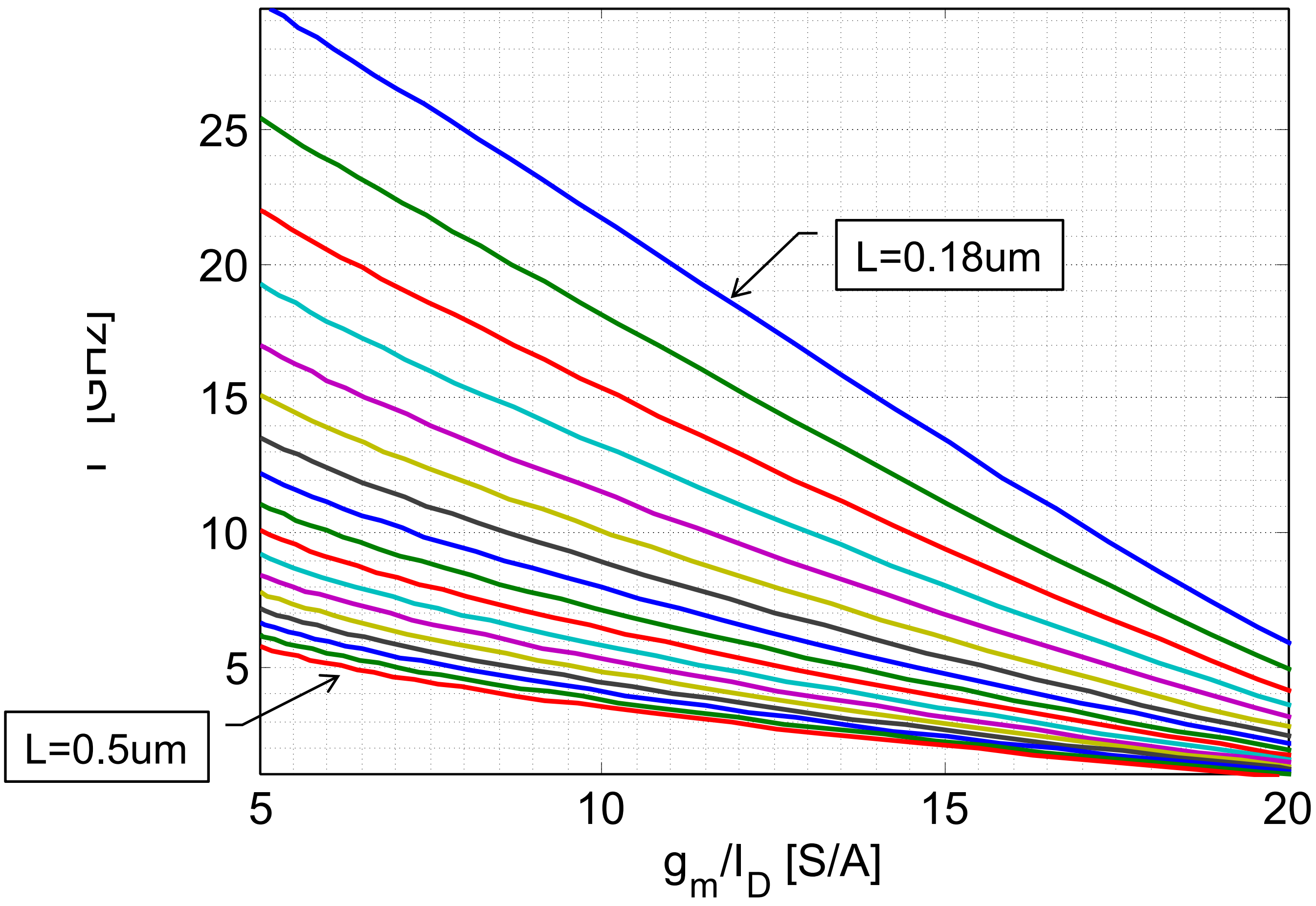
- **Plot of the following parameters (over a reasonable range of g_m/I_D and channel length)**
  - Transit frequency (f_T)
  - Intrinsic gain (g_m/g_{ds})
  - Current density (I_D/W)

- **These plots are (to the first order) independent of device width**
  - Enable "normalized design" and re-use of charts

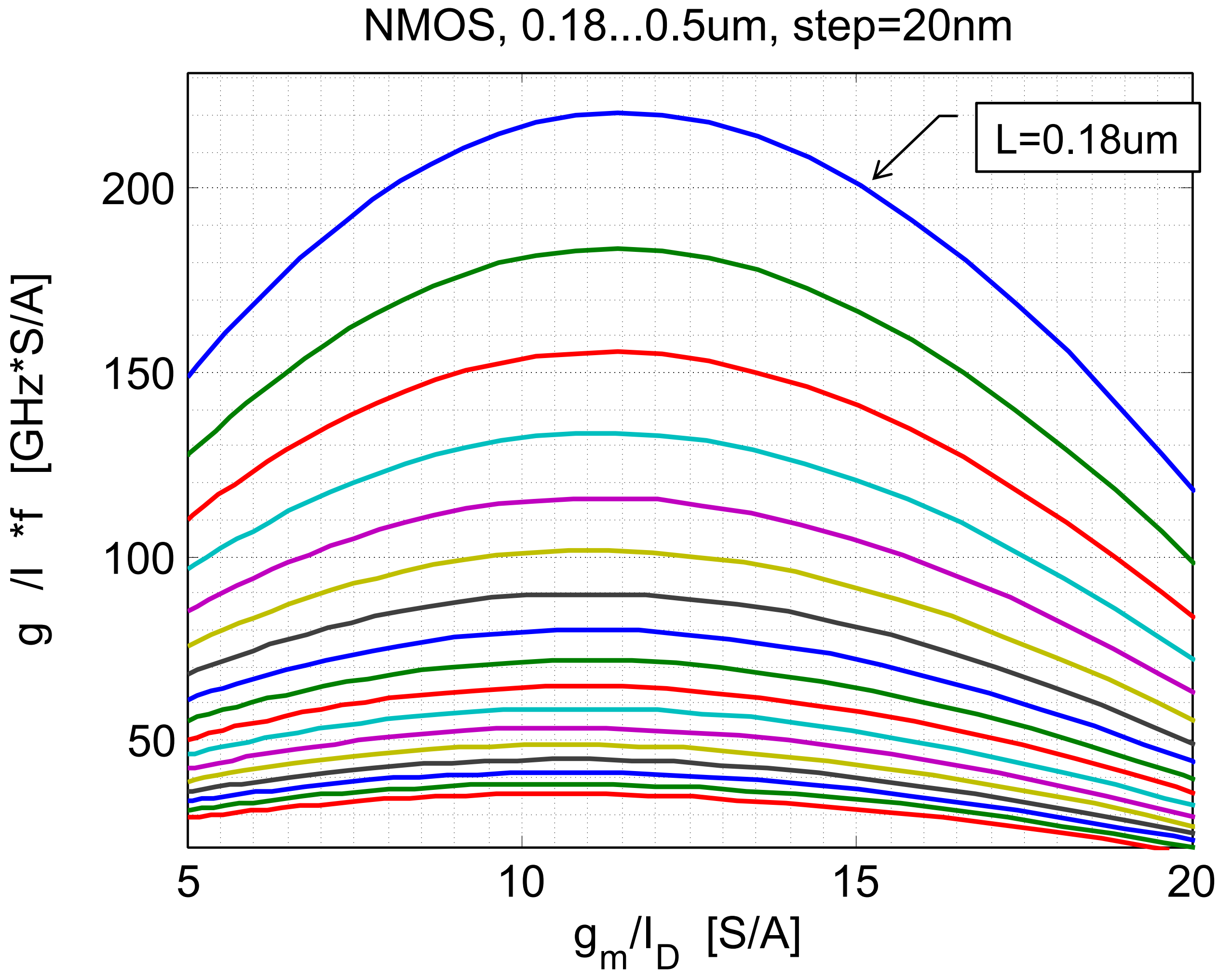
- **Tabulate relative estimates of extrinsic capacitances**
  - C_{gd}/C_{gg} and C_{dd}/C_{gg}

Transit Frequency Plot

NMOS, 0.18...0.5um (step=20nm), V_{DS}=0.9V

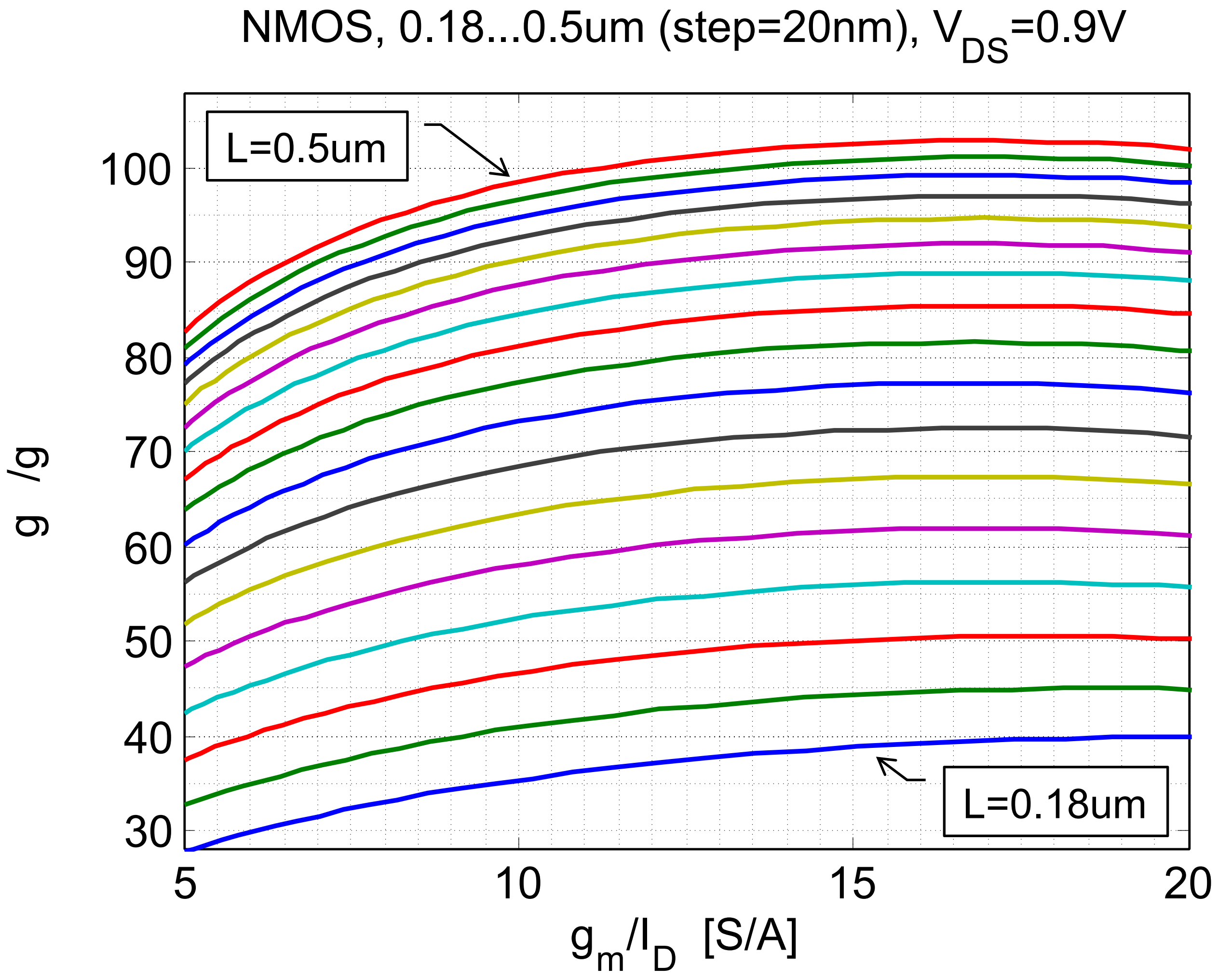


$g_m/I_D \times f_T$ Plot

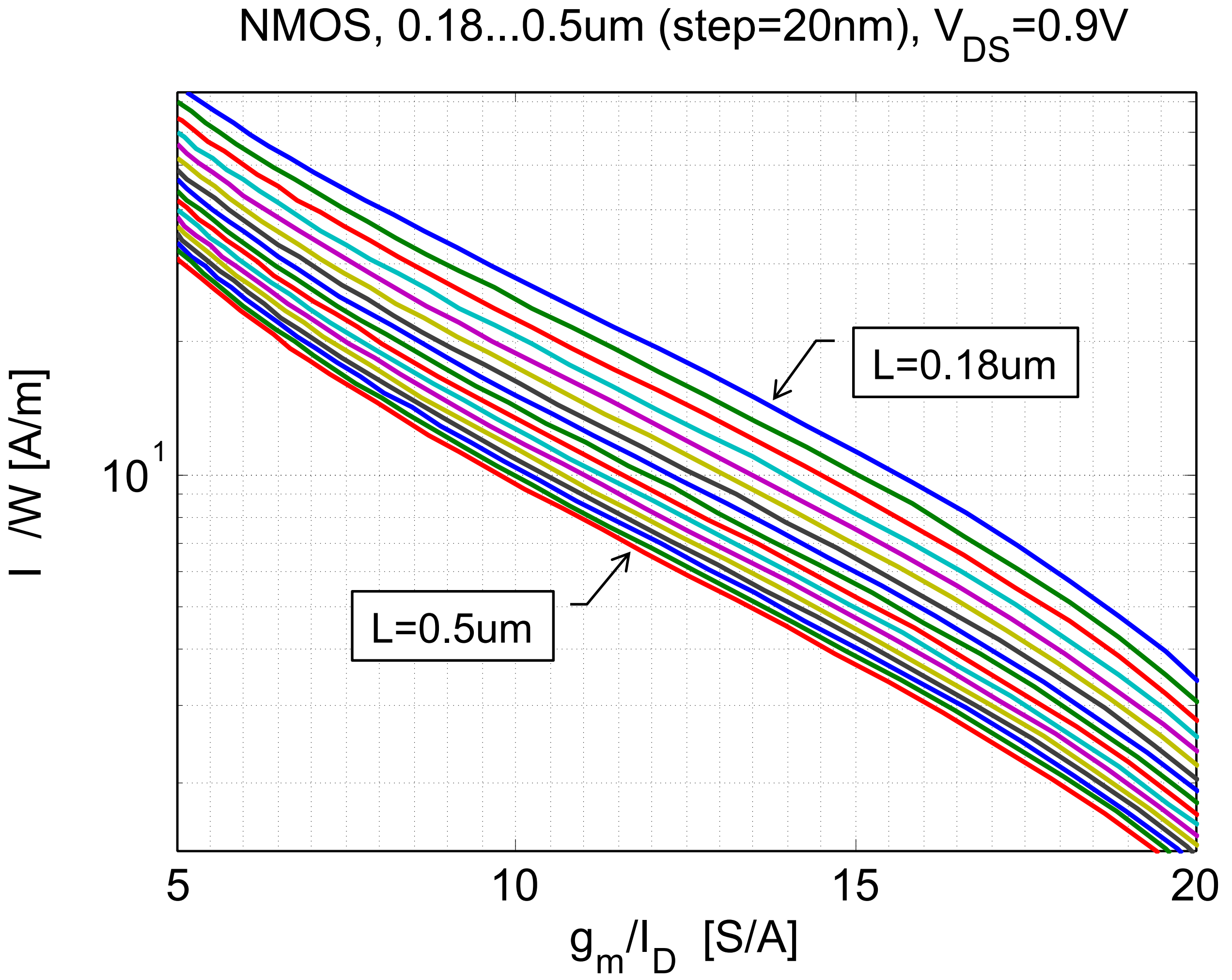


$10S/A \le g_m/I_D \le 13S/A$ can be a good choice for designs in which both power and speed are important

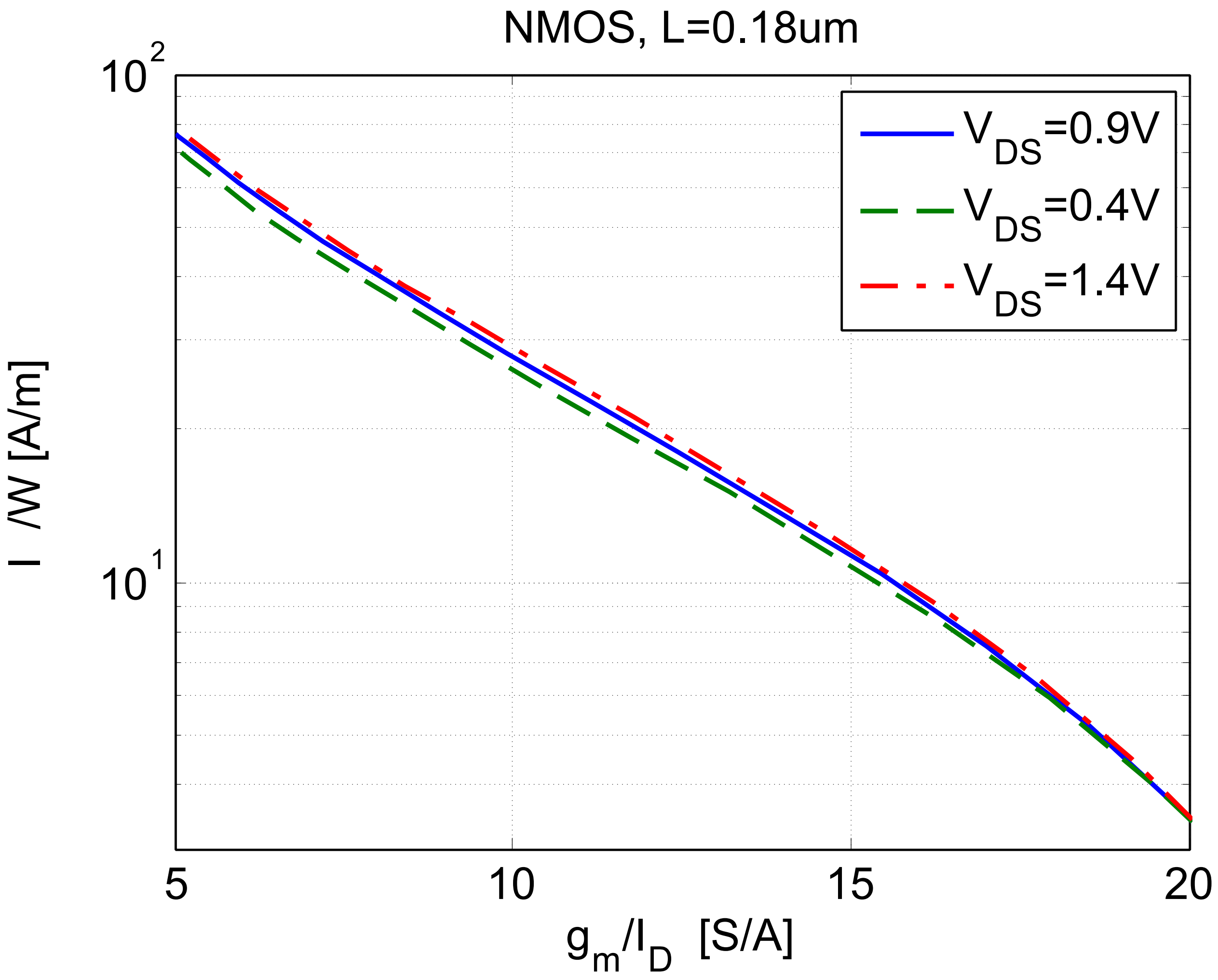
Intrinsic Gain Plot



Current Density Plot (Sizing Chart)

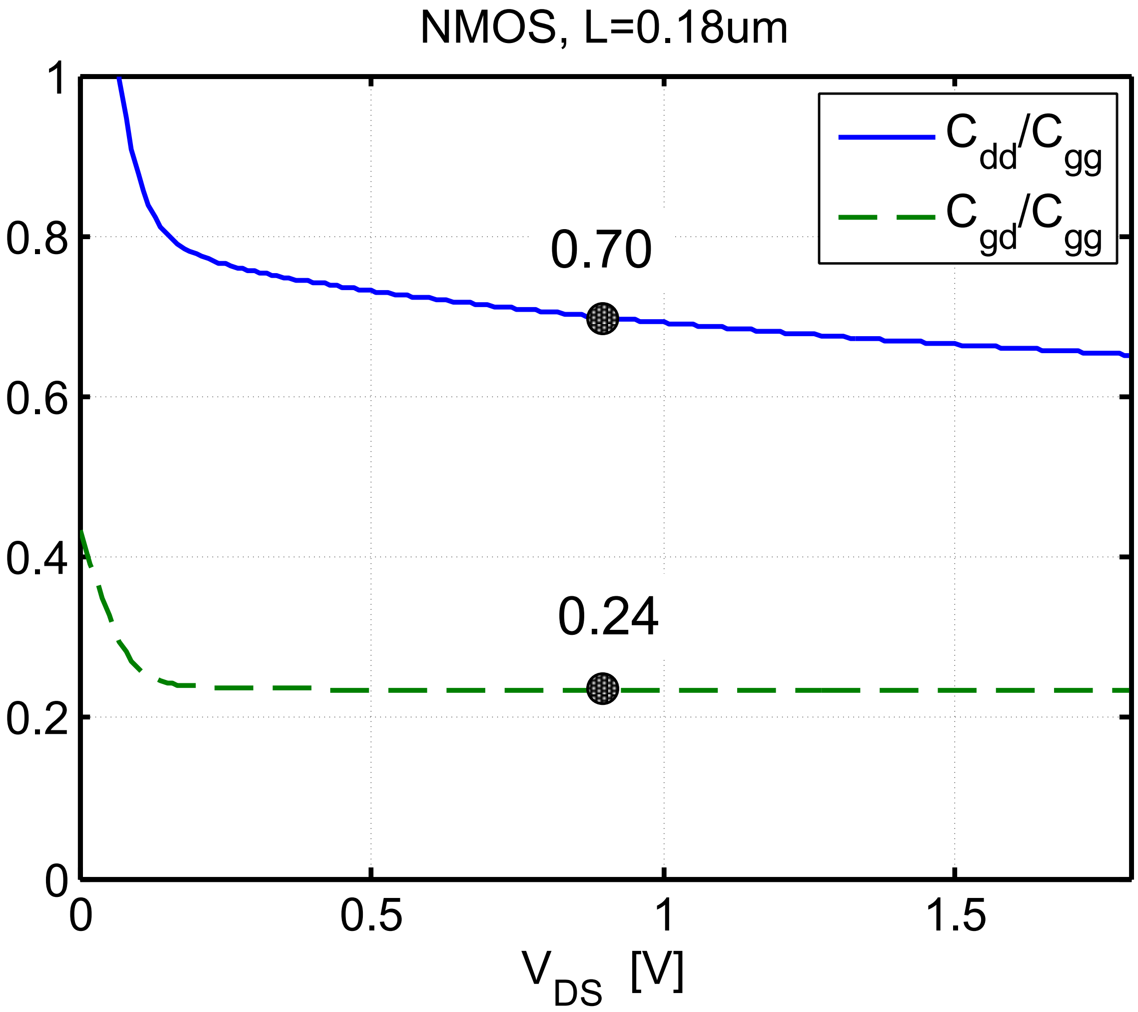


V_{DS} Dependence



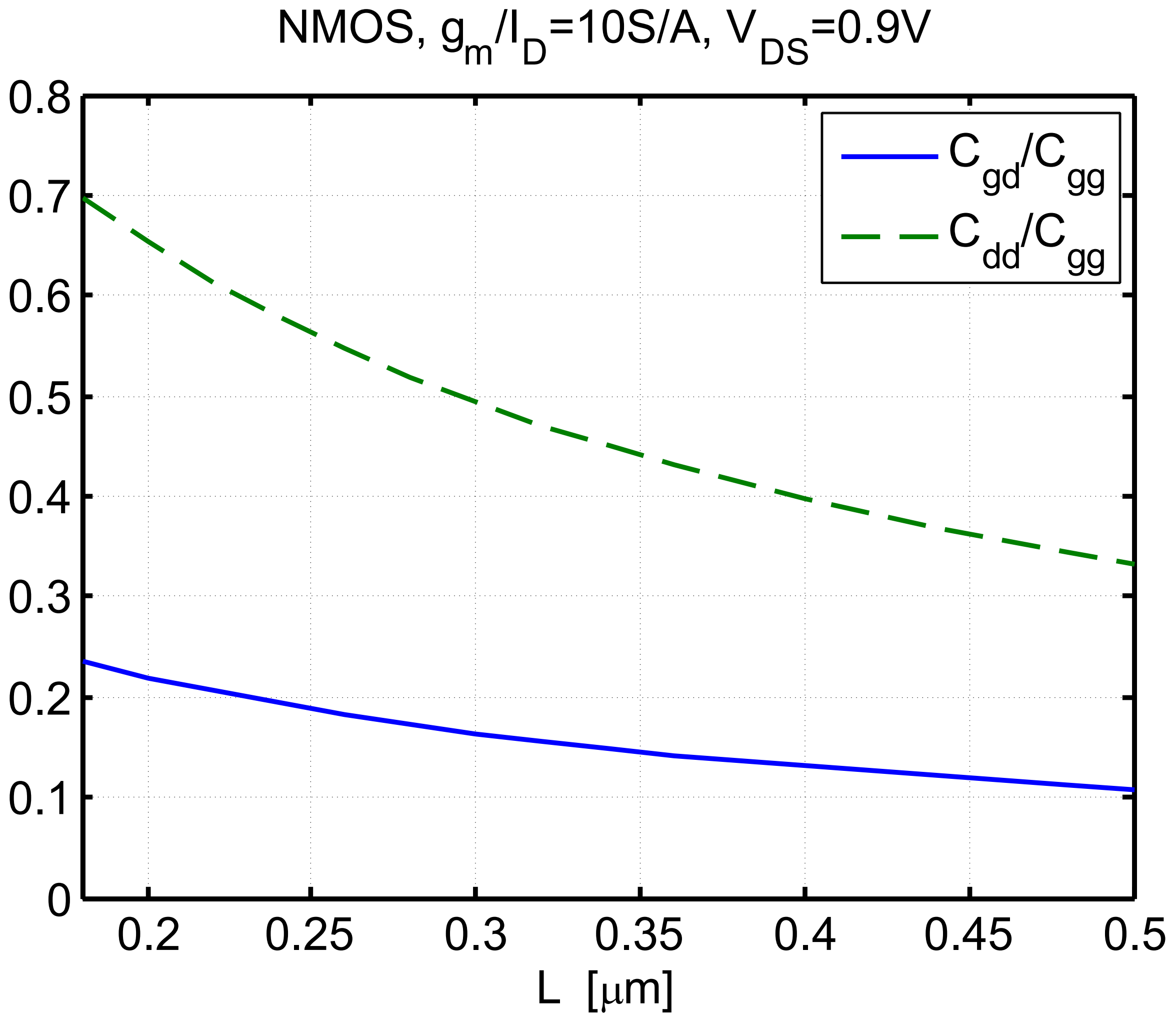
- **Dependence on V_{DS} is relatively weak**
- **Typically we can work with plots generated for $V_{DD}/2$**

Extrinsic Capacitances (1)



- **Again, usually it is fine to work with estimates taken at $V_{DD}/2$**

Extrinsic Capacitances (2)

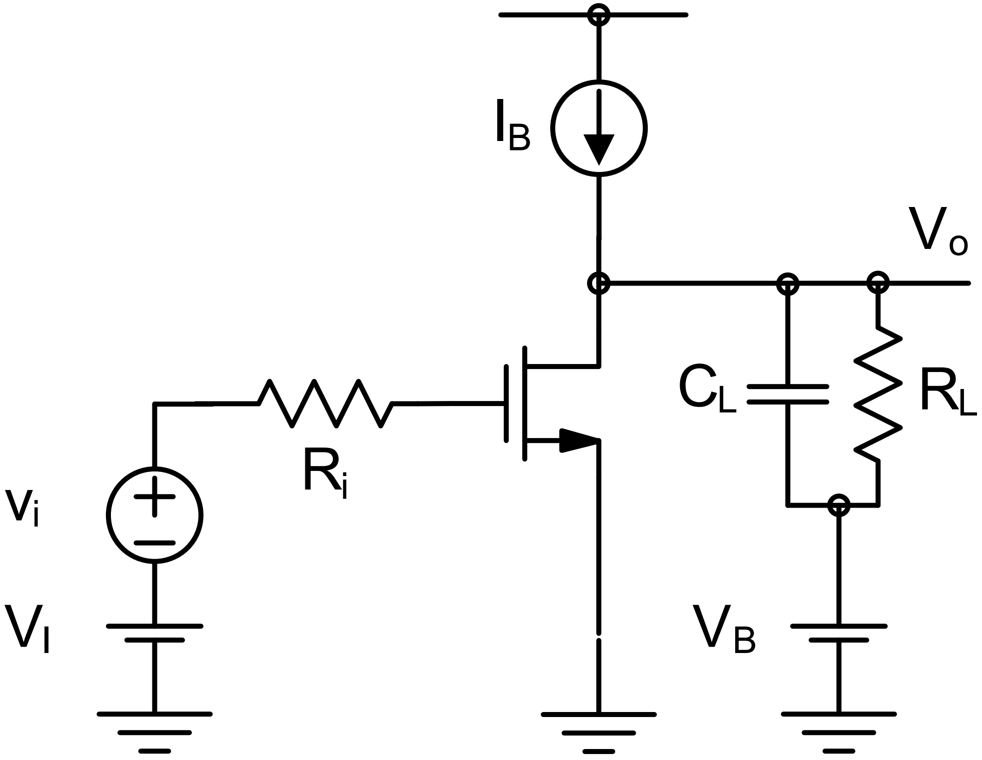


Generic Design Flow

1) **Determine g_m (from design objectives)**
2) **Pick L**
    1) Short channel → high f_T (high speed)
    2) Long channel → high intrinsic gain
3) **Pick g_m/I_D (or f_T)**
    1) Large g_m/I_D → low power, large signal swing (low V_{DSsat})
    2) Small g_m/I_D → high f_T (high speed)
4) **Determine I_D (from g_m and g_m/I_D)**
5) **Determine W (from I_D/W, current density chart)**

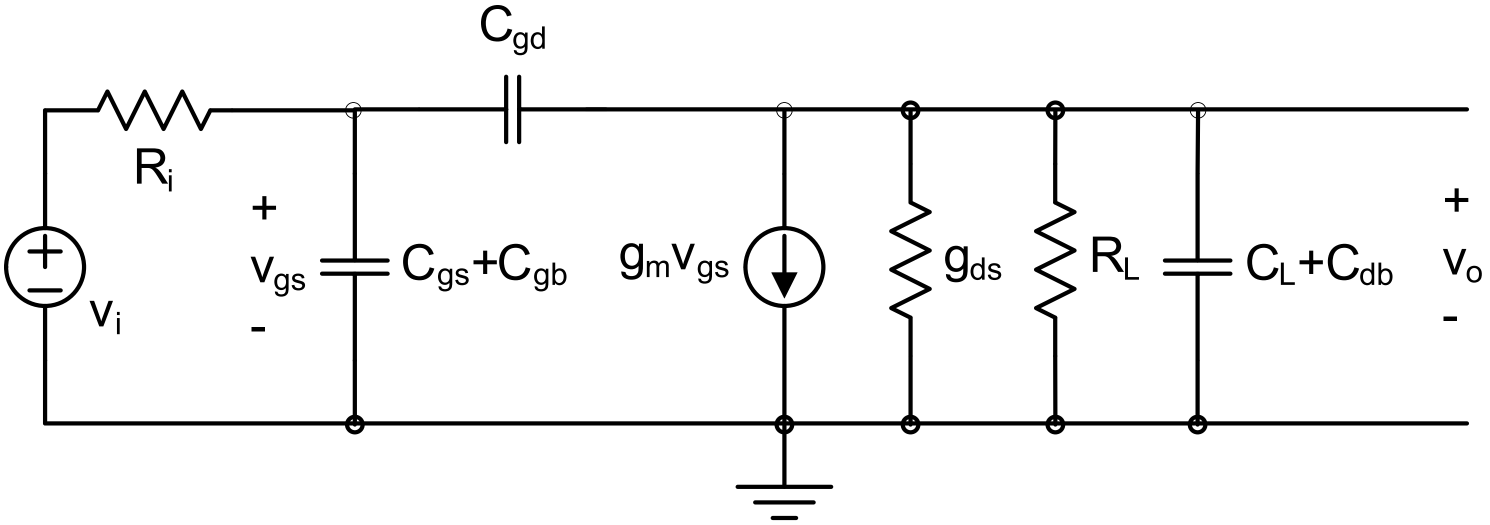
- **Many other possibilities exist (depending on circuit specifics, design constraints and objectives)**

Simple Design Example



- **Specifications**
  - 0.18µm technology
  - DC gain = -4
  - R_L=1kΩ, C_L=50fF, and R_i=10k Ω
  - Maximize bandwidth while keeping $I_B \leq 300\mu A$
  - Determine device width
  - Estimate the dominant pole

Small-Signal Model



- **Calculate g_m and g_m/I_D**

$$|A_{DC}| \cong g_m R_L = 4 \quad \Rightarrow \quad g_m = \frac{4}{1k\Omega} = 4mS$$

$$\boxed{\frac{g_m}{I_D} = \frac{4mS}{300\mu A} = 13.3\frac{S}{A}}$$

Zero and Pole Expressions

High frequency zero (negligible)

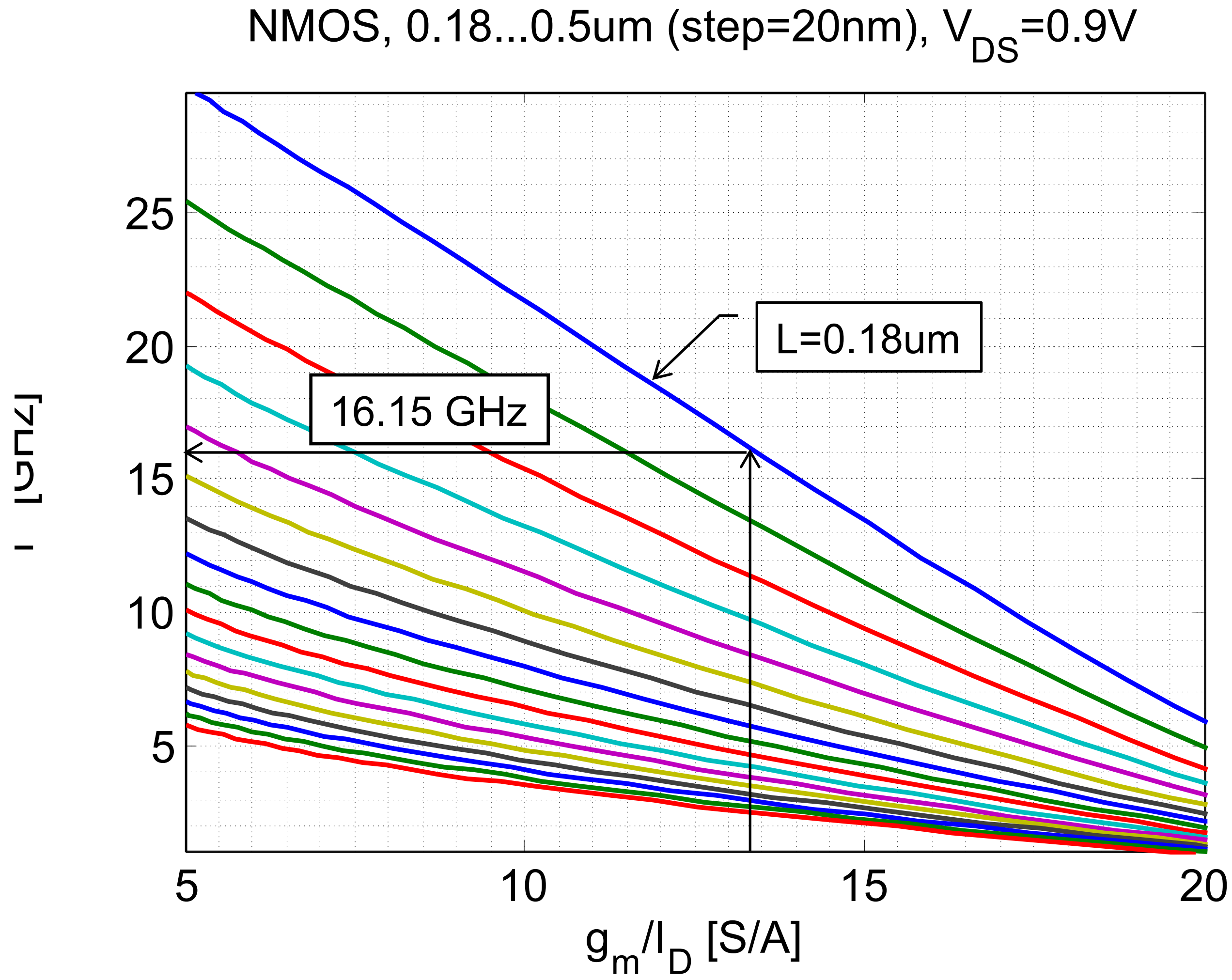
$$\omega_z \cong \frac{g_m}{C_{gd}} >> \omega_T$$

Dominant pole (Miller approximation)

$$\omega_{p1} \cong \frac{1}{R_i\left[C_{gs} + C_{gb} + \left(1 + g_m R_L\right) \cdot C_{gd}\right]}$$

$$\cong \frac{1}{R_i\left[C_{gg} + g_m R_L \cdot C_{gd}\right]}$$

Determine C_{gg} via f_T Look-up



Find Capacitances and Plug in

$$C_{gg} = \frac{1}{2\pi}\frac{g_m}{f_T} = \frac{1}{2\pi}\frac{4mS}{16.15GHz} = 39.4\,fF$$

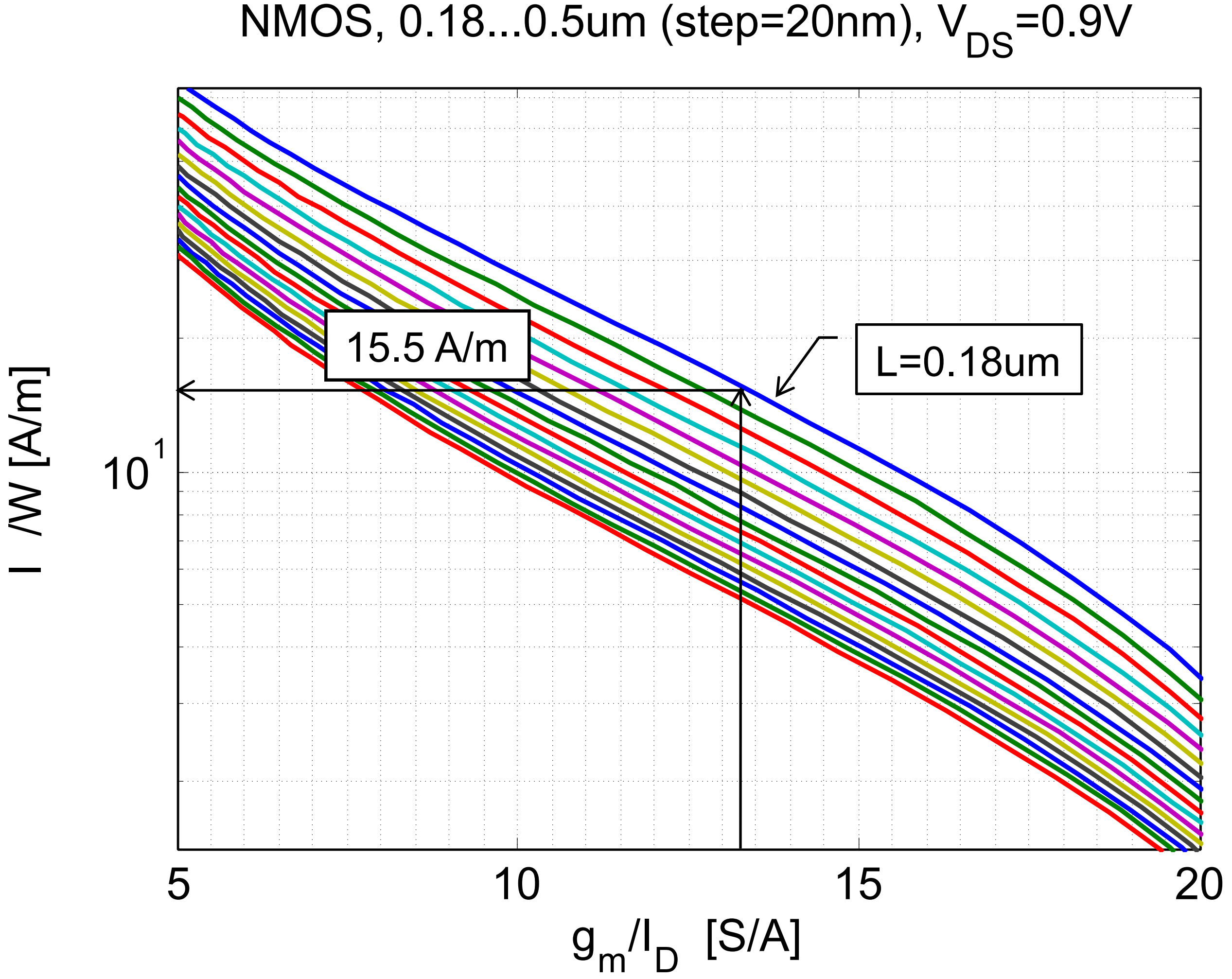
$$C_{gd} = \frac{C_{gd}}{C_{gg}}C_{gg} = 0.24\cdot 39.4\,fF = 9.46\,fF$$

$$C_{dd} = \frac{C_{dd}}{C_{gg}}C_{gg} = 0.70\cdot 39.4\,fF = 27.6\,fF$$

$$\boxed{\therefore f_{p1} \cong 206MHz}$$

$$\boxed{\therefore f_{p2} \cong 4.2GHz}$$

Device Sizing

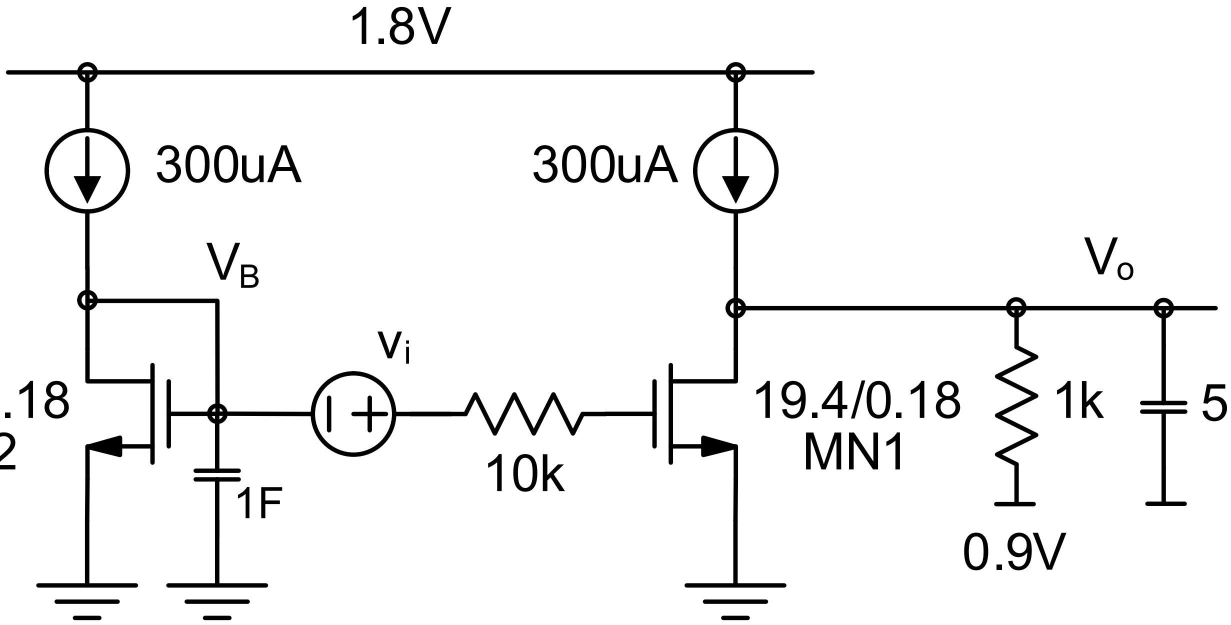


Circuit For Spice Verification

- **Device width**

$$W = {I_D}\Big/{\frac{I_D}{W}} = \frac{300\mu A}{15.5 A/m} = 19.4\mu m$$

- **Simulation circuit**

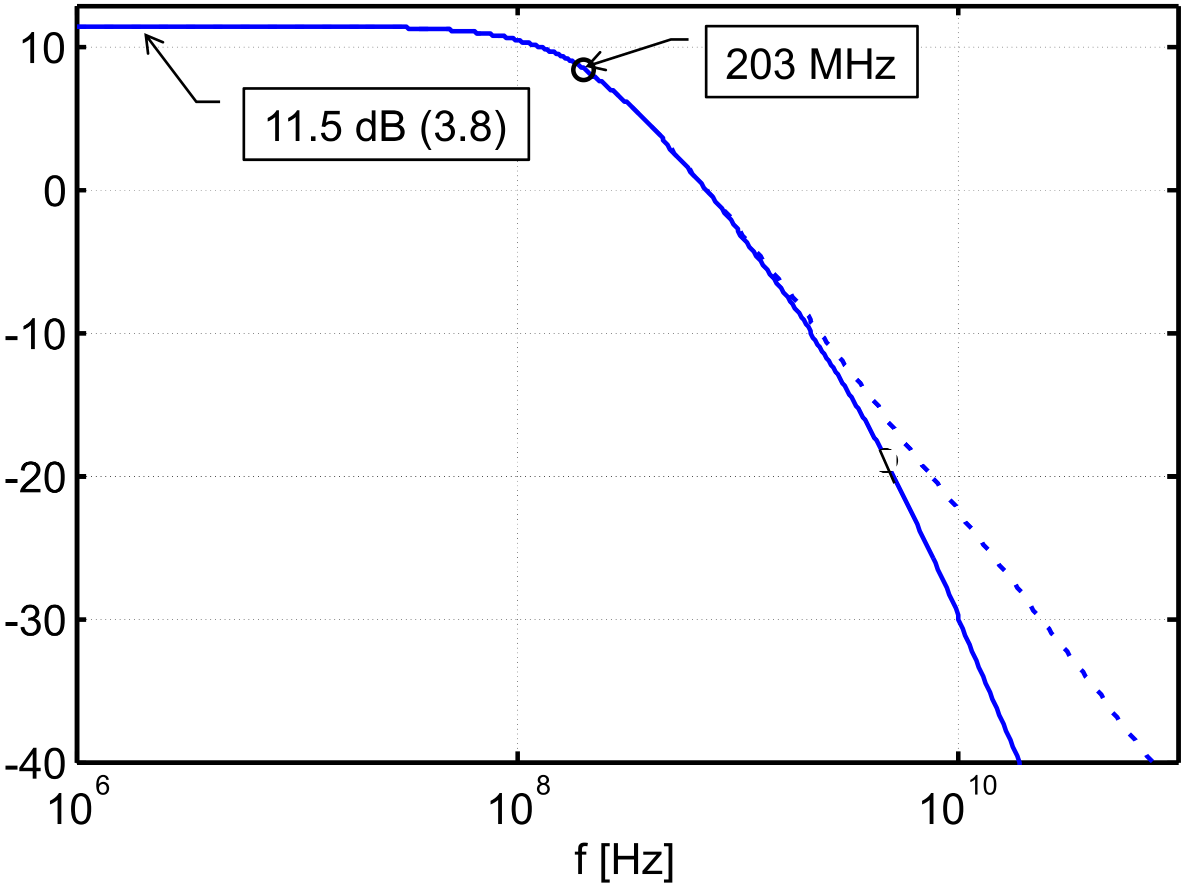


Simulated DC Operating Point

SPICE	Calculation
Id=327. 6259µA	300 µA
gm=4.1837 mS	4 mS
cdtot=27.0360 fF	27.6 fF
cgtot=39.5020 fF	39.4 fF
cgd=9.3506 fF	9.46 fF
gm/Id=12.8 S/A	13.3 S/A

Fairly good agreement!

Simulated AC Response



- **Calculated values: A_{DC}=12 dB (4.0) and f_{p1}=206 MHz**

Observations

- **The design is essentially right on target!**
  - Typical discrepancies are on the order of 10 to 20%, mostly due to V_{DS} dependencies, finite output resistance, etc.
- **We accomplished this by using pre-computed spice data in the design process**
- **Even if discrepancies are more significant, there's always the possibility to track down the root causes**
  - Hand calculations use only parameters that also exist in Spice, e.g., g_m/I_D, f_T, etc.
  - Different from square law calculations using μC_{ox}, V_{OV}, etc.
    - Based on artificial parameters that do not exist or have no significance in the spice model

Other Useful References

[1] F. Silveira et al., “A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA,” IEEE Journal of Solid-State Circuits, pp. 1314-1319, Sep. 1996.

[2] D. Foty, M. Bucher, D. Binkley, “Re-interpreting the MOS transistor via the inversion coefficient and the continuum of gms/Id,” Int. Conference on Electronics, Circuits and Systems, pp. 1179-1182, Sep. 2002.

[3] B. E. Boser, “Analog Circuit Design with Submicron Transistors,” IEEE Solid-State Circuits Society (SSCS) Chapter Meeting, Santa Clara Valley, http://www.ewh.ieee.org/r6/scv/ssc/May1905.htm, May 2005.