An Introduction to Phase-Locked Loops and Clock and Data Recovery

Shahriar Mirabbasi

References used to prepare these slides:

Behzad Razavi ed., *Monolithic Phase-Locked Loops and Clock Recovery Circuits, Theory and Design*, Wiley-IEEE Press, 1996

Richard C. Walker, Clock and Data Recovery for Serial Digital Communication, ISSCC Short Course, 2002

Behzad Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003

Bahzad Razavi ed., *Phase-Locking in High-Performance Systems From Devices to Architectures*, Wiley-IEEE Press, 2003

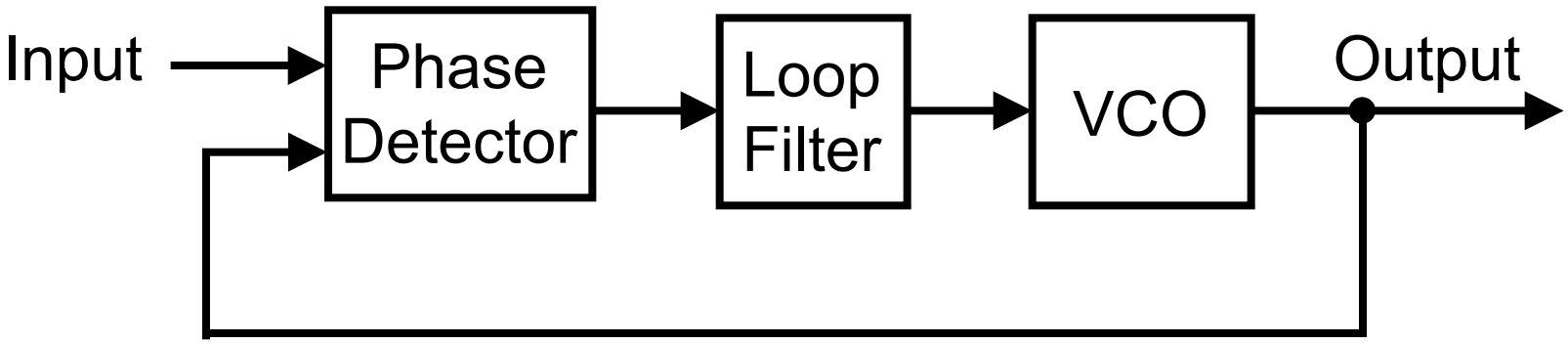
Dennis Fischette, Introduction to PLL and DLL Design for Digital Systems, ISSCC Tutorial, 2004

Agilen Technologies, Measuring Jitter in Digital Systems, Application Note 1448-1

Technical contributions of Marwa Hamour and Pedram Sameni are greatly acknowledged.

Simplified Block Diagram of a PLL

- PLL is a feedback system that, when in lock, aligns the phase of its periodic input and output.

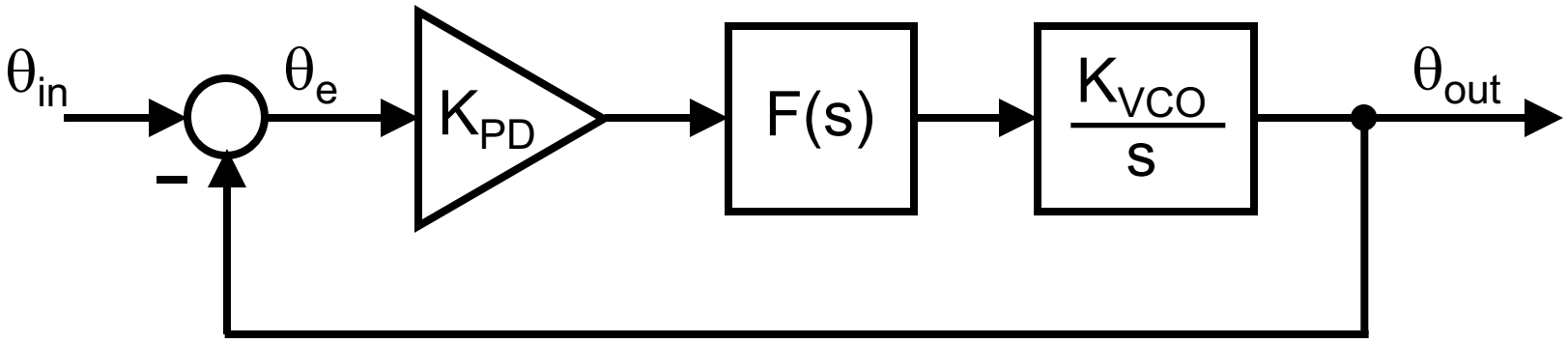


- Feedback path may include a frequency divider.

Applications

- PLLs are ubiquitous blocks and are used in almost all communication-related applications. They are used for:
  - Jitter reduction
  - Skew suppression
  - Frequency synthesis
  - Clock and data recovery
  - …

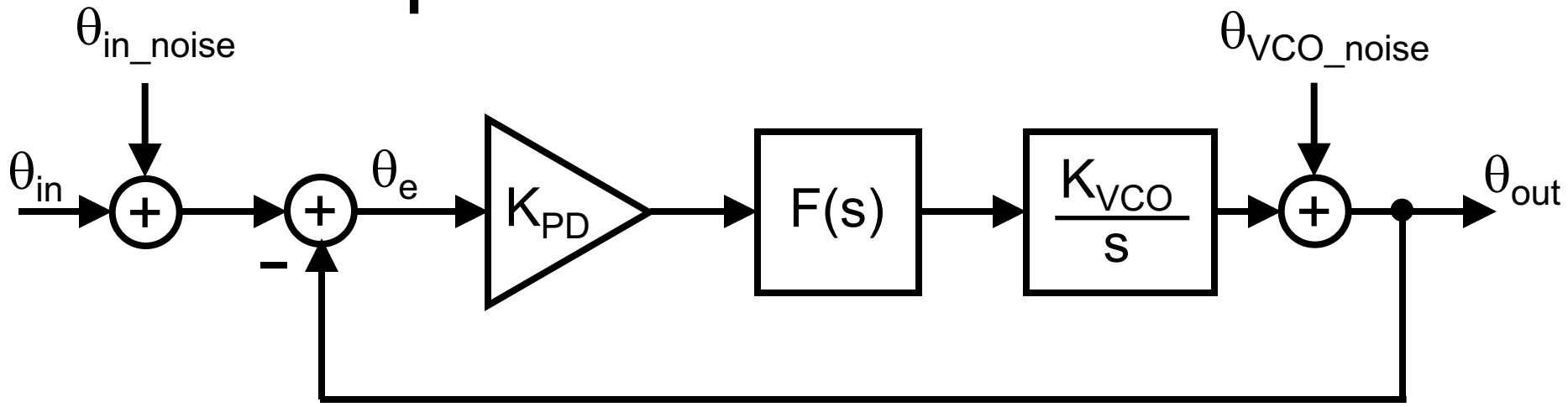
Simple PLL Linear Model



$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + K_{PD}K_{VCO}F(s)}$$

$$H_e(s) = \frac{\theta_e(s)}{\theta_{in}(s)} = \frac{\theta_{in}(s) - \theta_{out}(s)}{\theta_{in}(s)} = \frac{s}{s + K_{PD}K_{VCO}F(s)}$$

Simple PLL Linear Model



$$\frac{\theta_{out}(s)}{\theta_{in\_noise}(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + K_{PD}K_{VCO}F(s)}$$

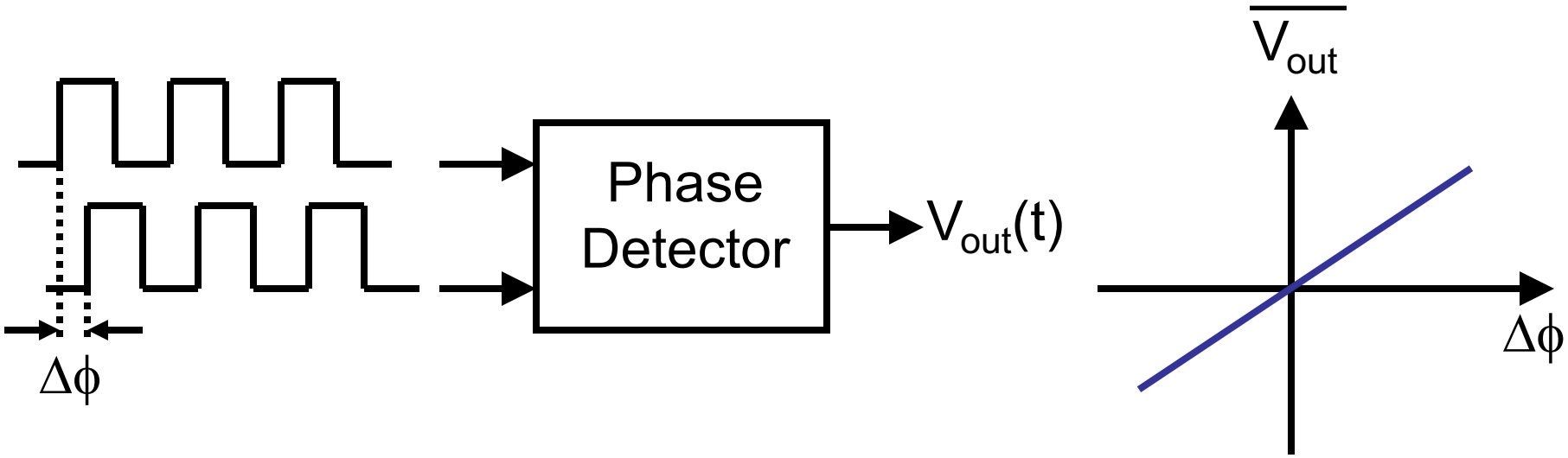
$$\frac{\theta_{out}(s)}{\theta_{VCO\_noise}(s)} = \frac{s}{s + K_{PD}K_{VCO}F(s)}$$

Design Trade-off

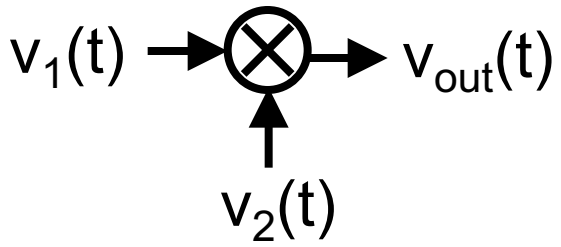
- Jitter of the PLL input is low pass filtered. Thus reducing the loop bandwidth improves the input phase noise rejection.
- Jitter generated in the VCO is high pass filtered through the loop. This noise is reduced as the bandwidth increases.
- Depending on the application proper loop bandwidth should be designed to minimize the overall phase noise at the output.

PLL Blocks: Phase Detector (PD)

- Ideally, the average value of the output of the phase detector is linearly proportional to the phase difference of its two (periodic) inputs.



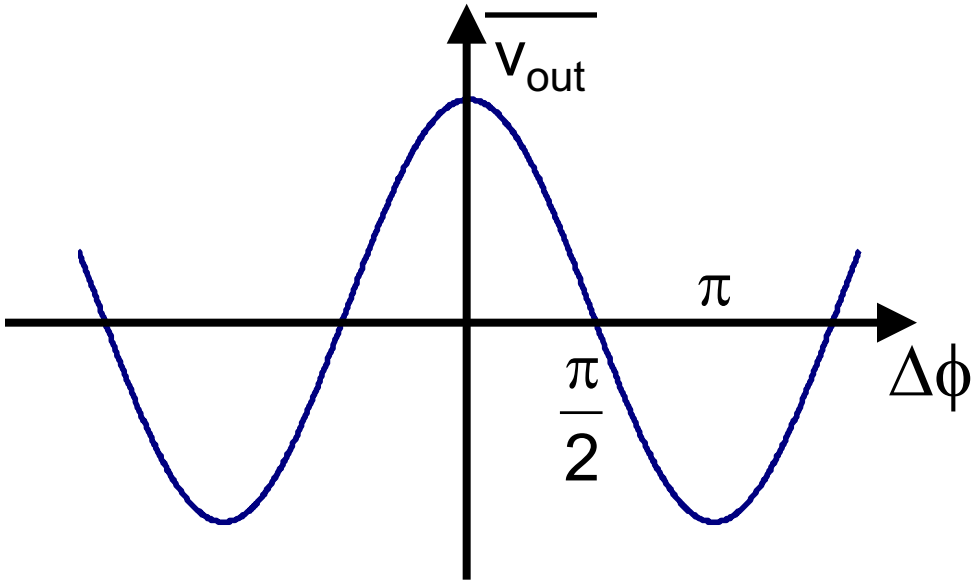
Mixer (Multiplier) as a PD



- For $v_1(t)=A_1\cos(\omega_1 t)$ and $v_2(t)=A_2\cos(\omega_2 t+\Delta\phi)$:
  $v_{out}(t)=0.5kA_1A_2\{\cos[(\omega_1+\omega_2)t+\Delta\phi]+\cos[(\omega_1-\omega_2)t-\Delta\phi]$
  where k is the mixer gain.
- For $\omega_1=\omega_2$ average output is given by $0.5kA_1A_2\cos(\Delta\phi)$
- For $\omega_1\neq\omega_2$ the average output is zero.

Multiplier as a PD

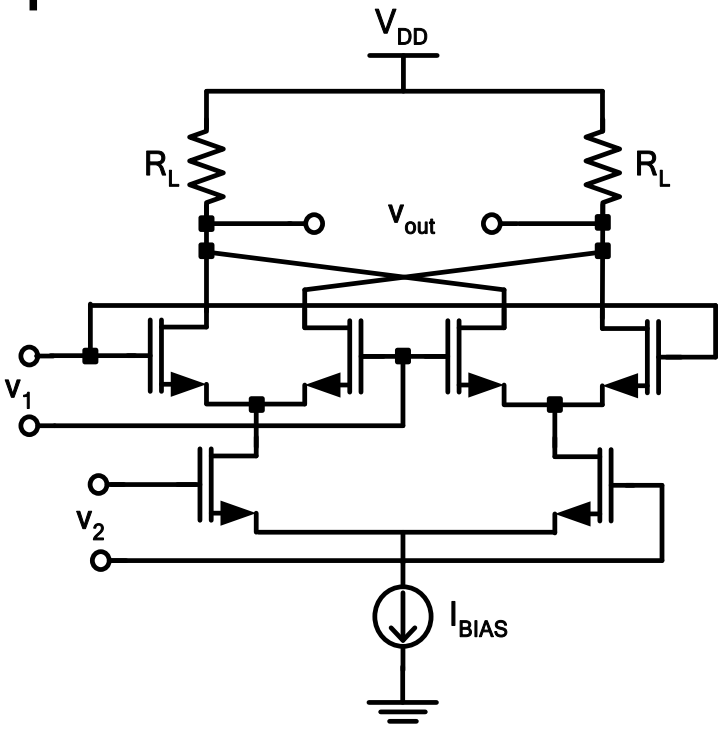
- Also called sinusoidal phase detector, it has the following characteristic curve:



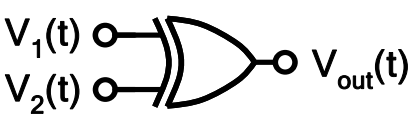
- In the vicinity of $\pi/2$ we have $\overline{v_{out}} \approx 0.5 k A_1 A_2 (\pi/2 - \Delta\phi)$

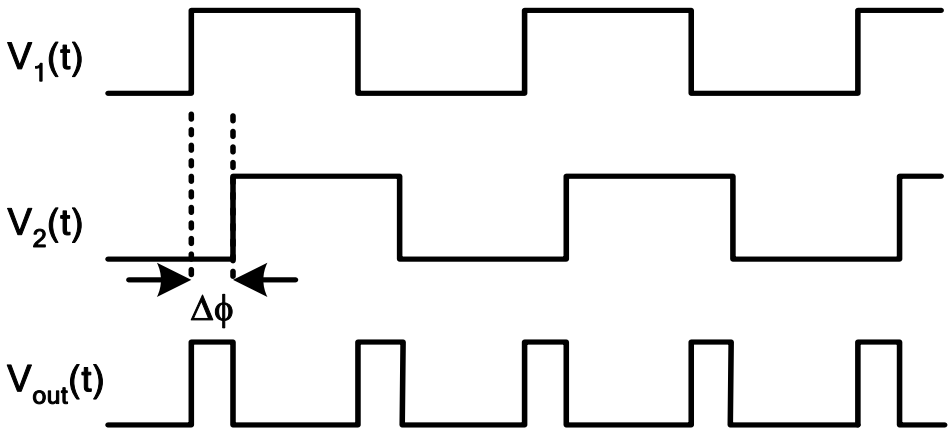
Multiplier as a PD

- K_{PD}=-0.5kA_1A_2
- K_{PD} is amplitude dependent (undesired)
- Gilbert multiplier can be used



Exclusive-OR as a PD

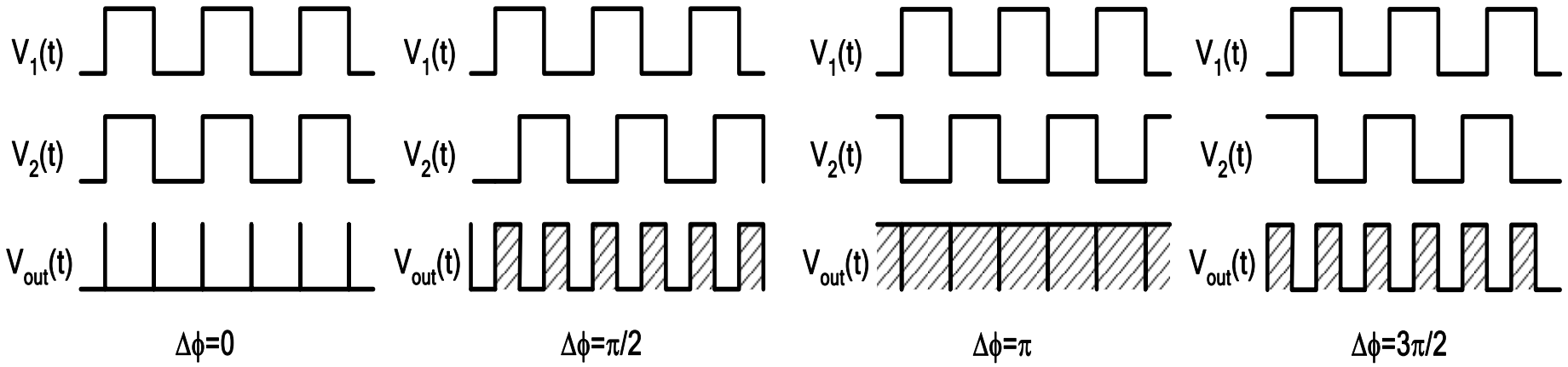




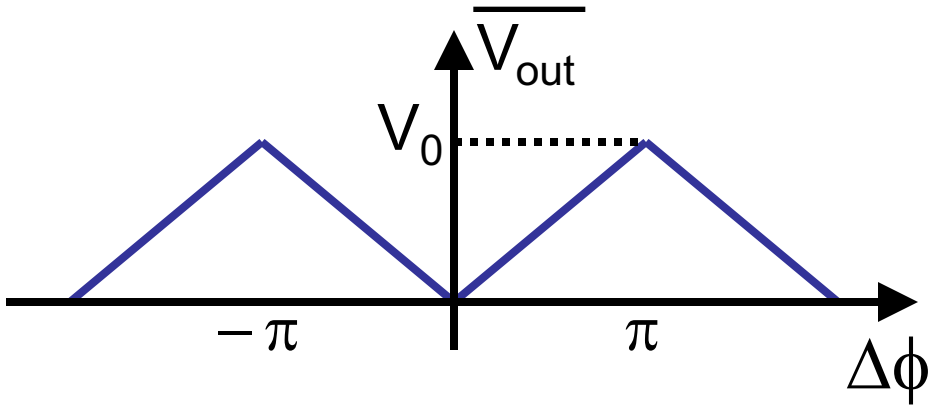
- For large input signals Gilbert cell operates as an XOR gate

Exclusive-OR as a PD

- For inputs with 50% duty-cycle

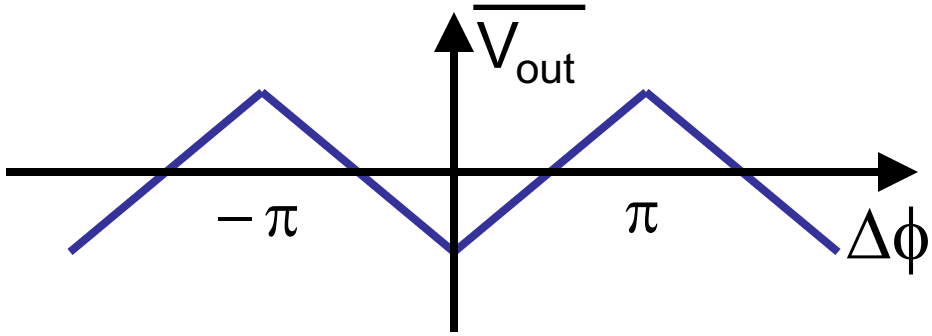


- $K_{PD}=V_0/\pi$



Exclusive-OR as a PD

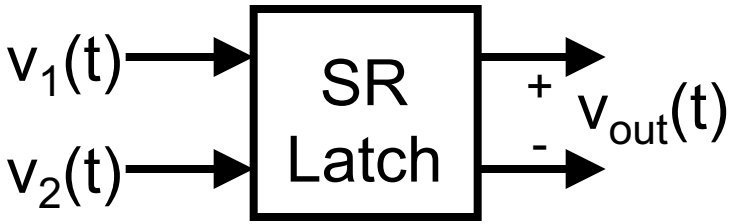
- K_{PD} is constant over the range of π (advantage over multiplier based PD)
- In differential implementations the phase characteristic would be

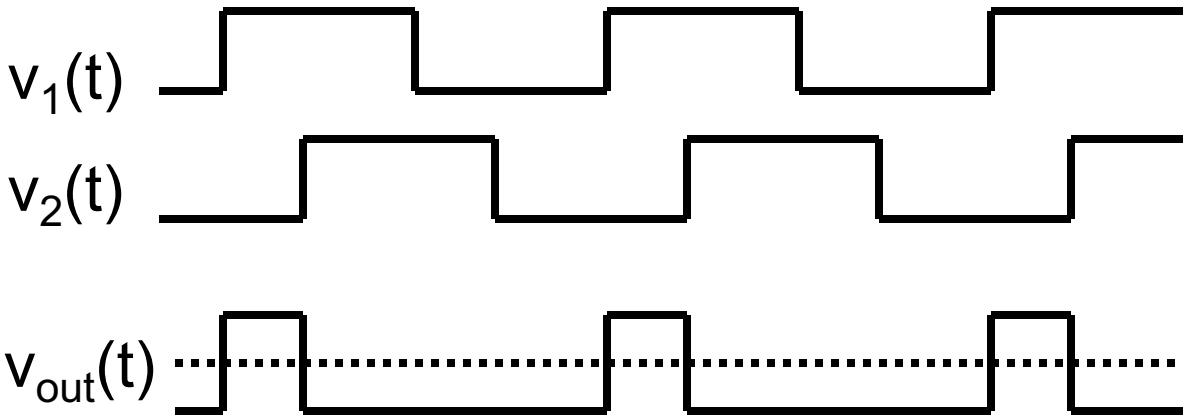


- The peak value also depends on the input duty cycle.

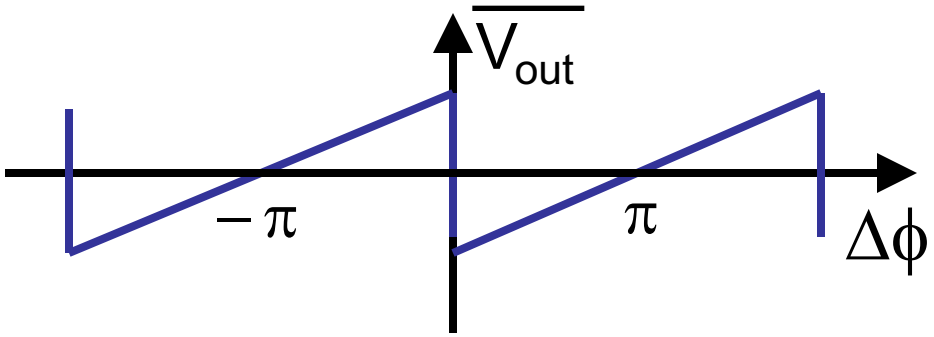
S-R Latch as a PD

- An edge-triggered S-R latch can be used as a PD.



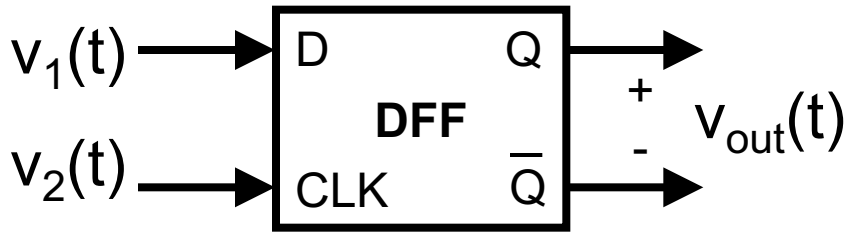


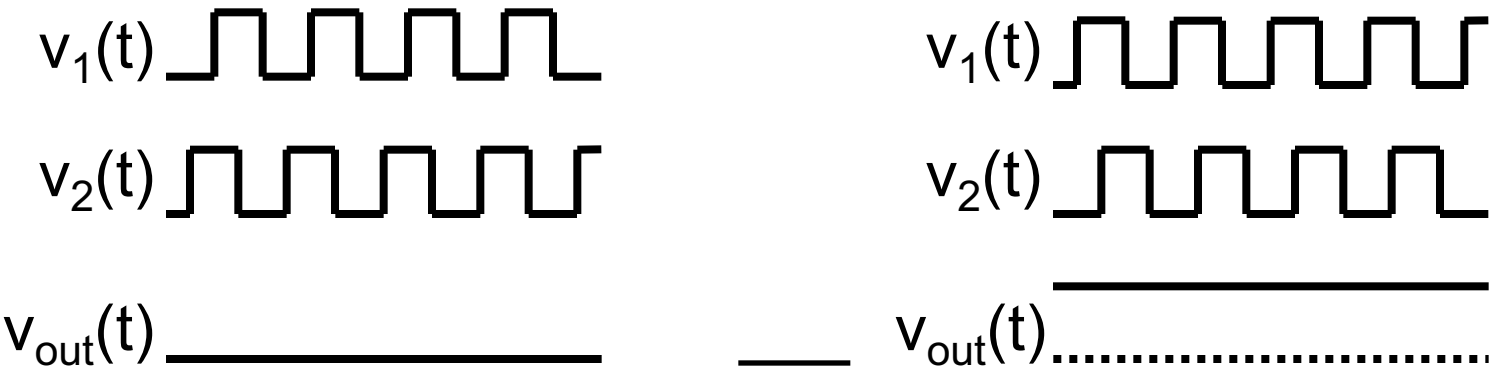
S-R Latch as a PD

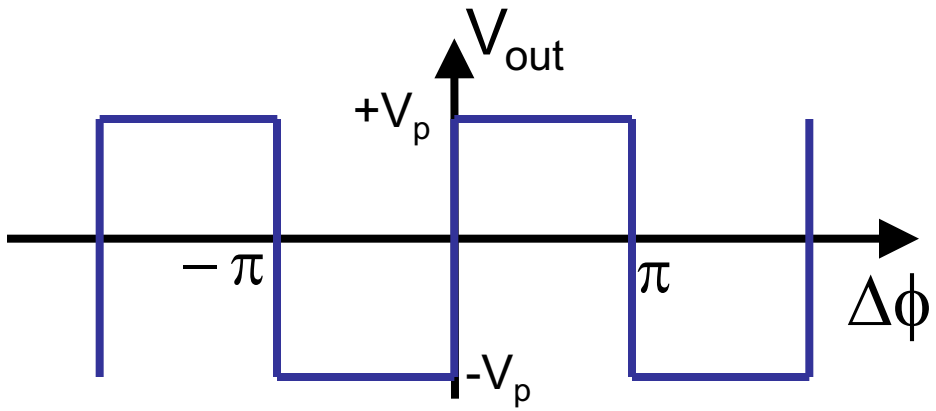


- Average output is independent of input duty cycle
- The monotonic range of PD is 2π
- Output jitter at lock due to metastability

D-Flip Flop as a PD

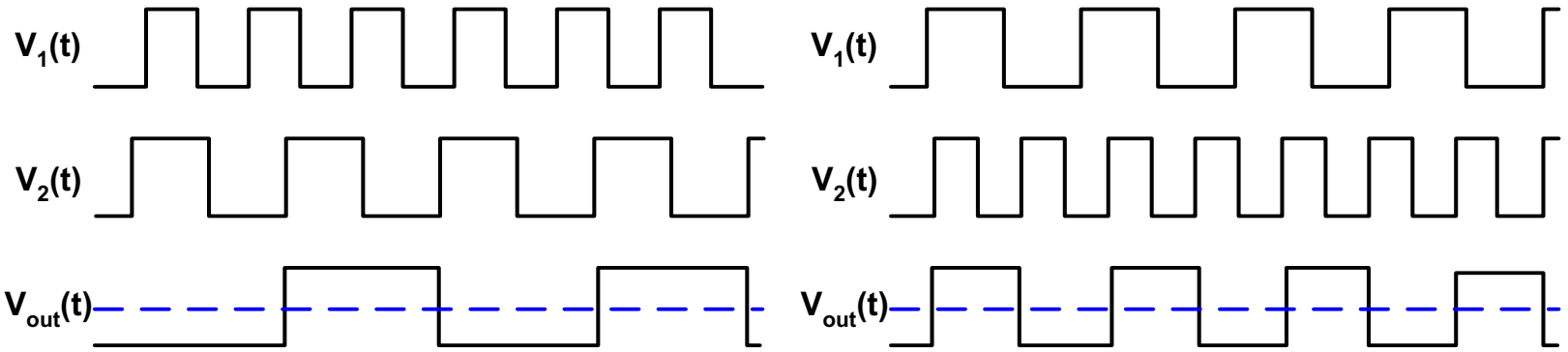




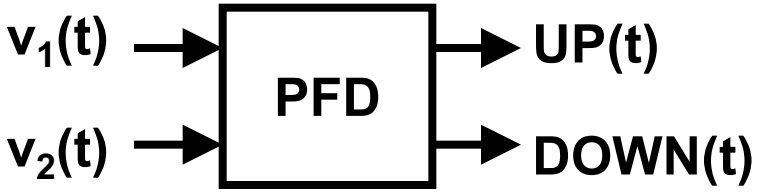


D-FF as a Frequency Detector

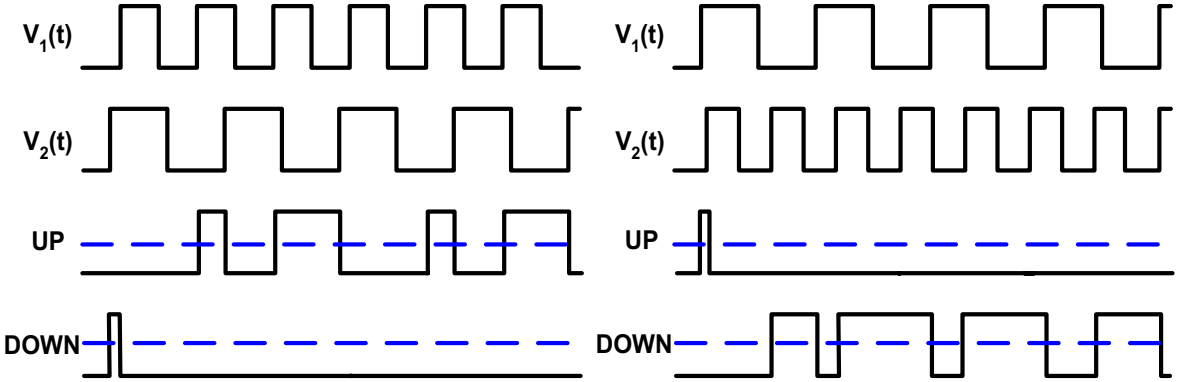
- Not a good choice!

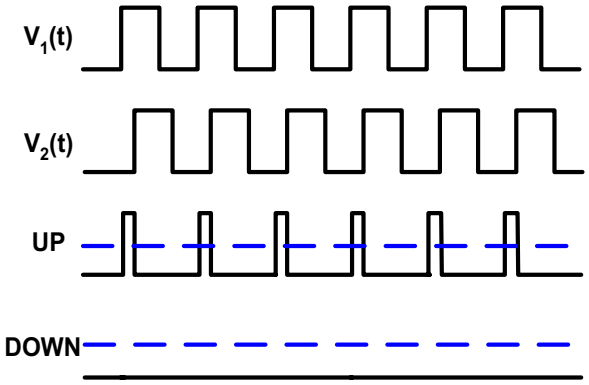


Phase/Frequency Detector

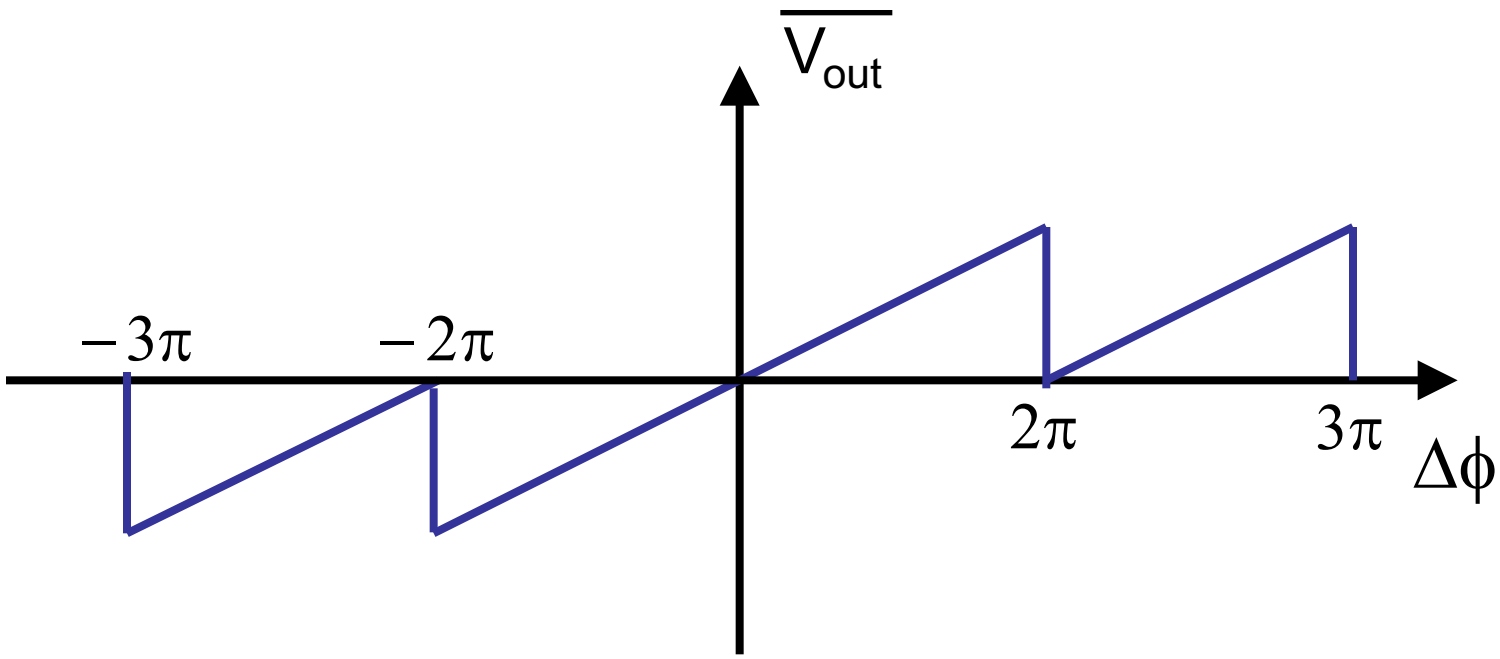


- Conceptual operation

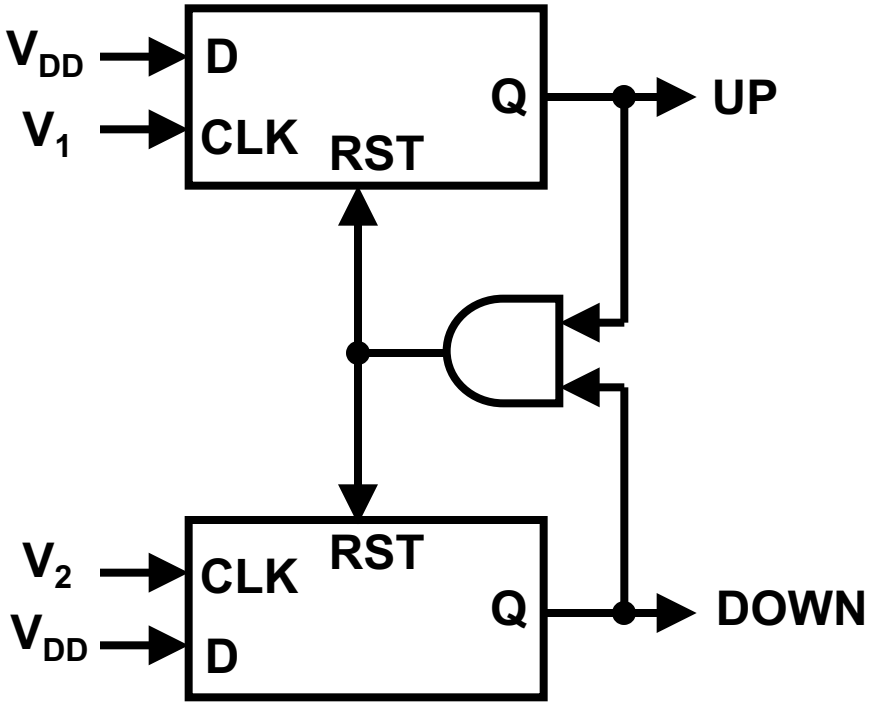


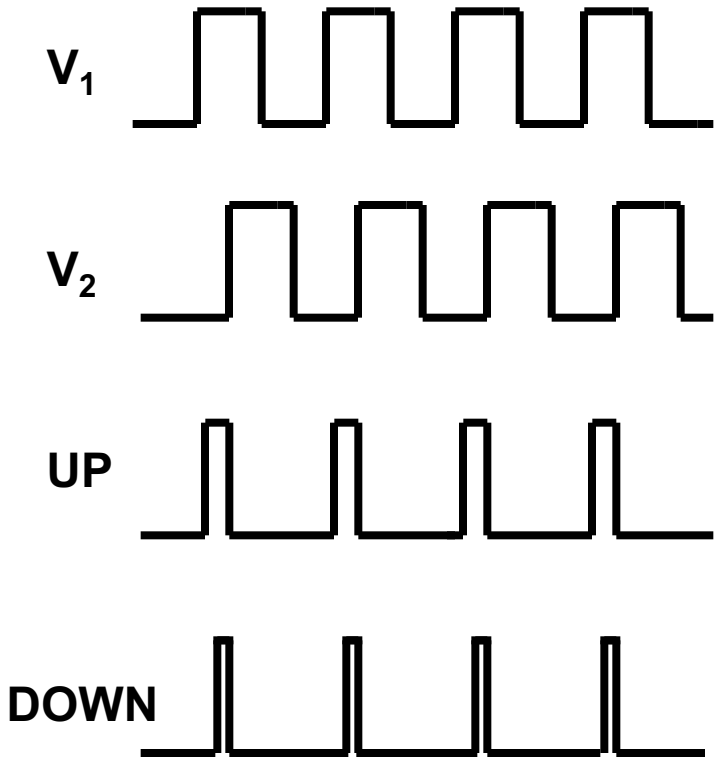


Phase Characteristics of the PFD

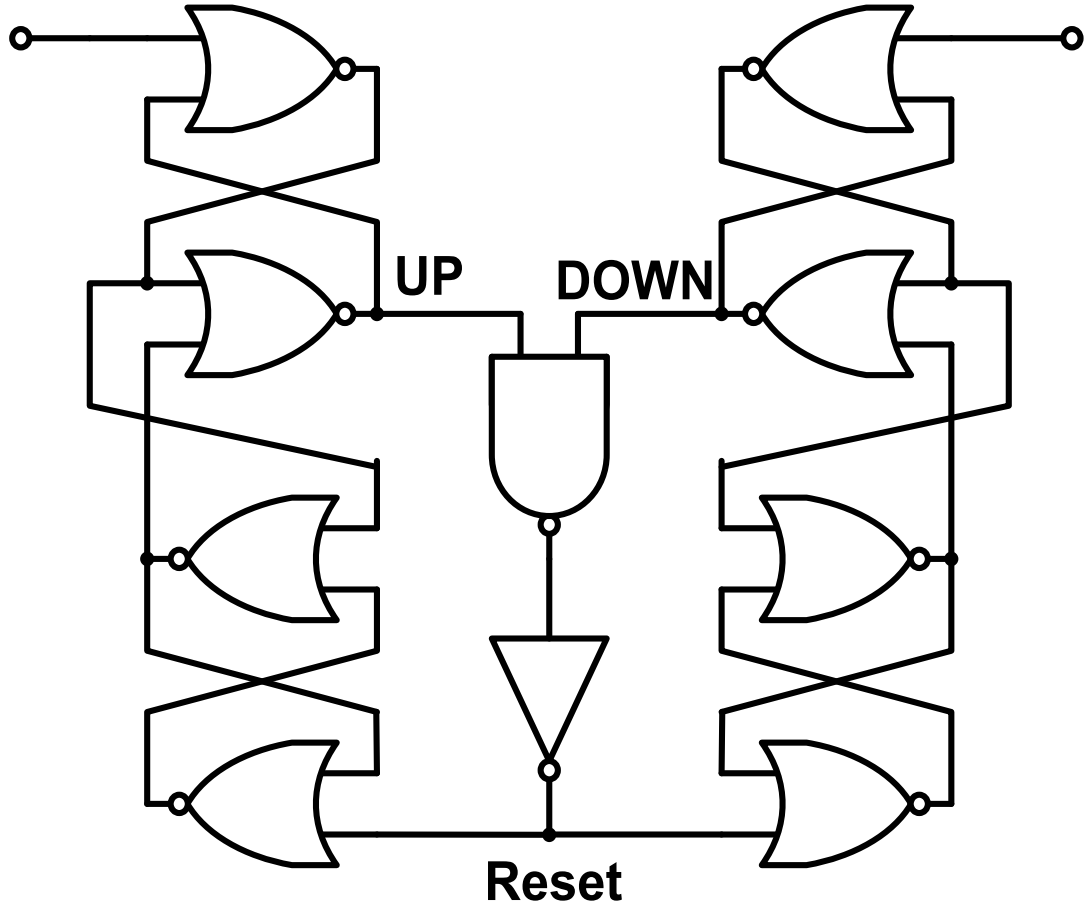


An Implementation for PFD



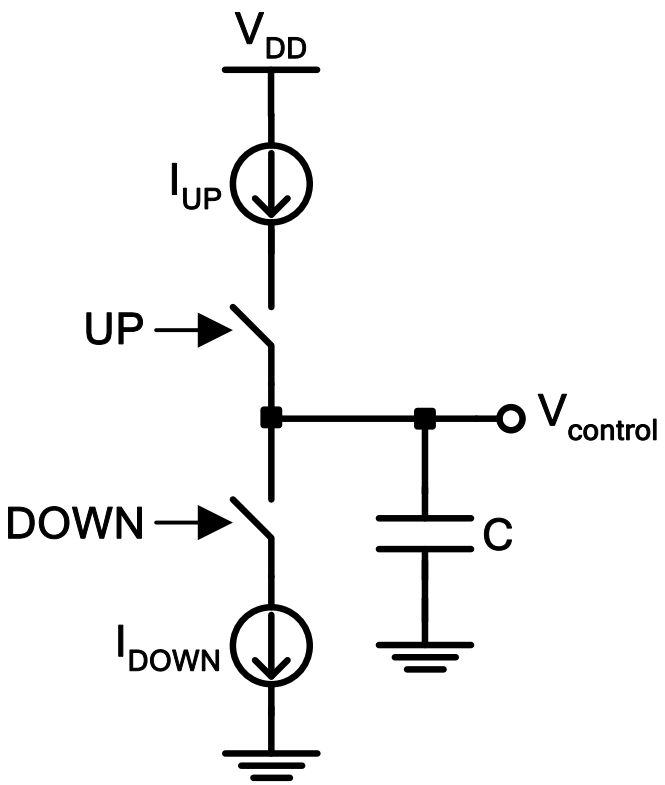


An Implementation for PFD



Charge Pump

- Converts the output pulse of the PD/PFD to charge that is proportional to PD/PFD pulse widths

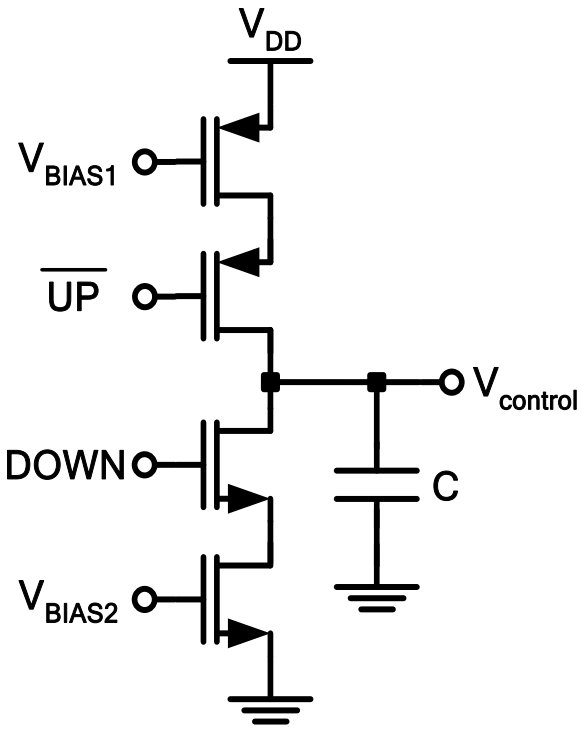


(Ideal) Charge Pump

- Equal UP/DOWN currents over the entire control voltage range (preferably programmable currents to control the loop dynamics)
- No charge coupling to control voltage during the switching
- Insensitive to power supply, process and temperature variations

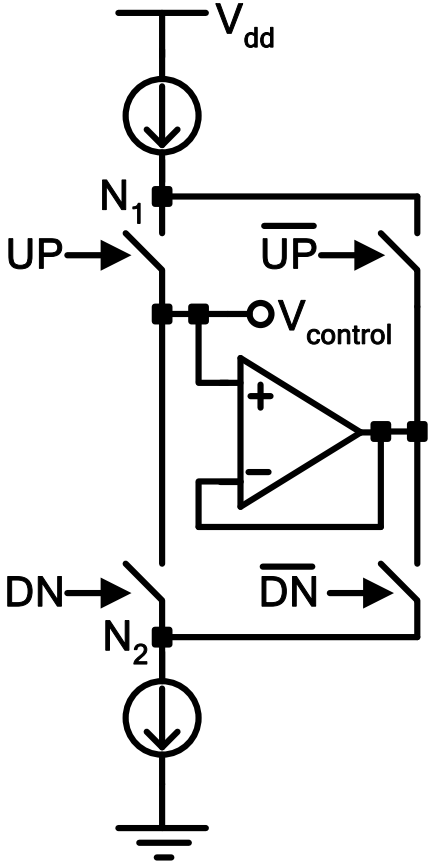
Simple Charge Pump

- Resistance of the switches varies (e.g., due to body effect)
- Can use CMOS pass gates as switches
- Long channel M_1 and M_2 for matching and higher output resistance



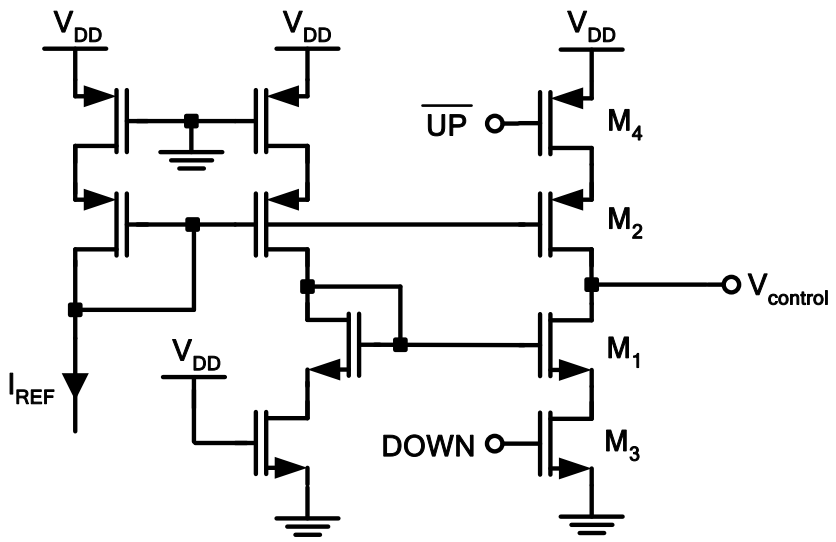
CP: Constant Current with Amp [YGW92]

- Unity gain amplifier suppresses charge sharing from parasitic capacitances on nodes N_1/N_2 and $V_{control}$ (reduced mismatch between I_{UP} and I_{DN})
- Buffer sinks "waste" current when UP(DN) is off



Charge Pump [LaR00]

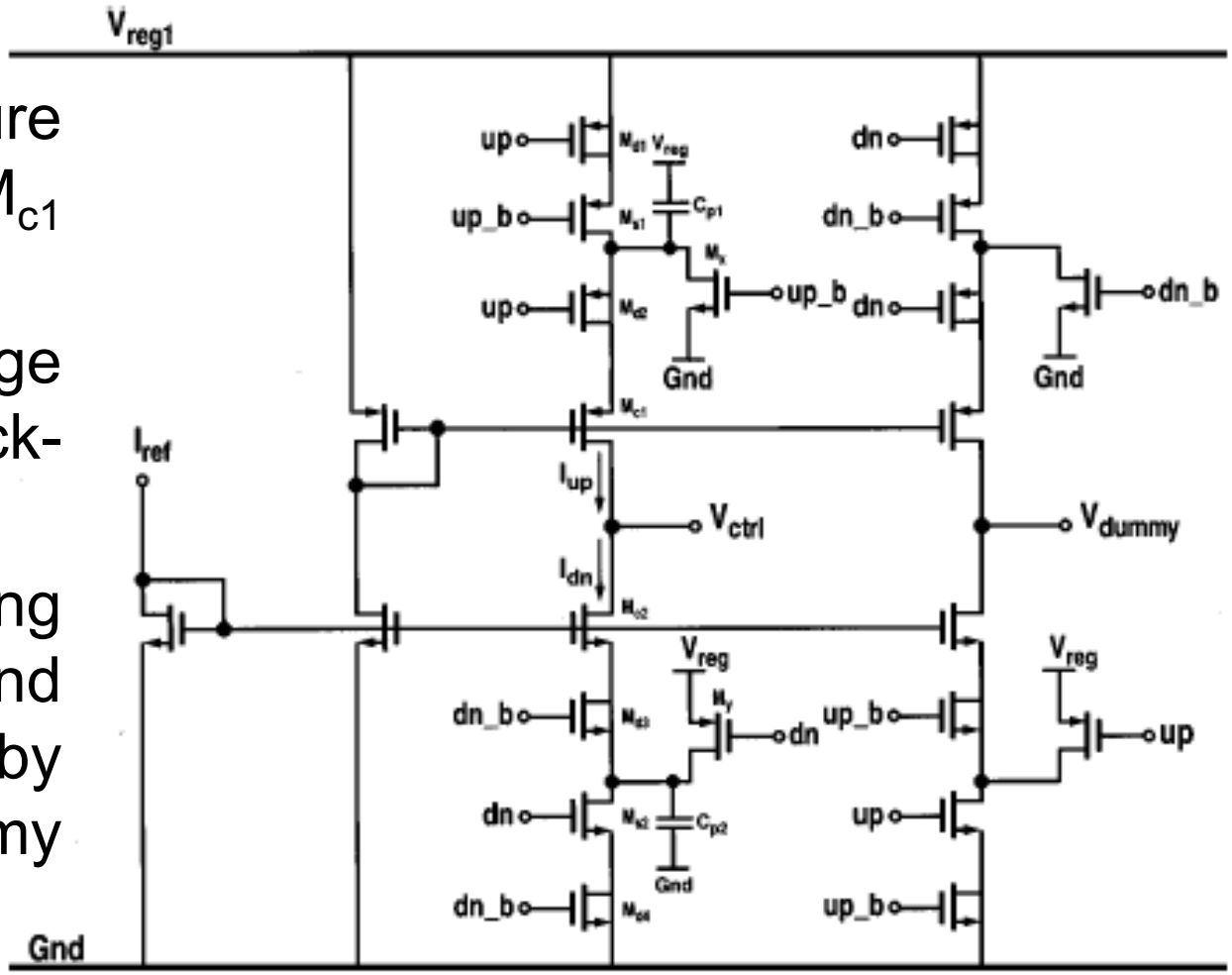
- Move Switches closer to the rails to reduce the body-effect of switches, charge injection and clock feed-through



- M_1, M_2 and corresponding biasing transistors are long channel

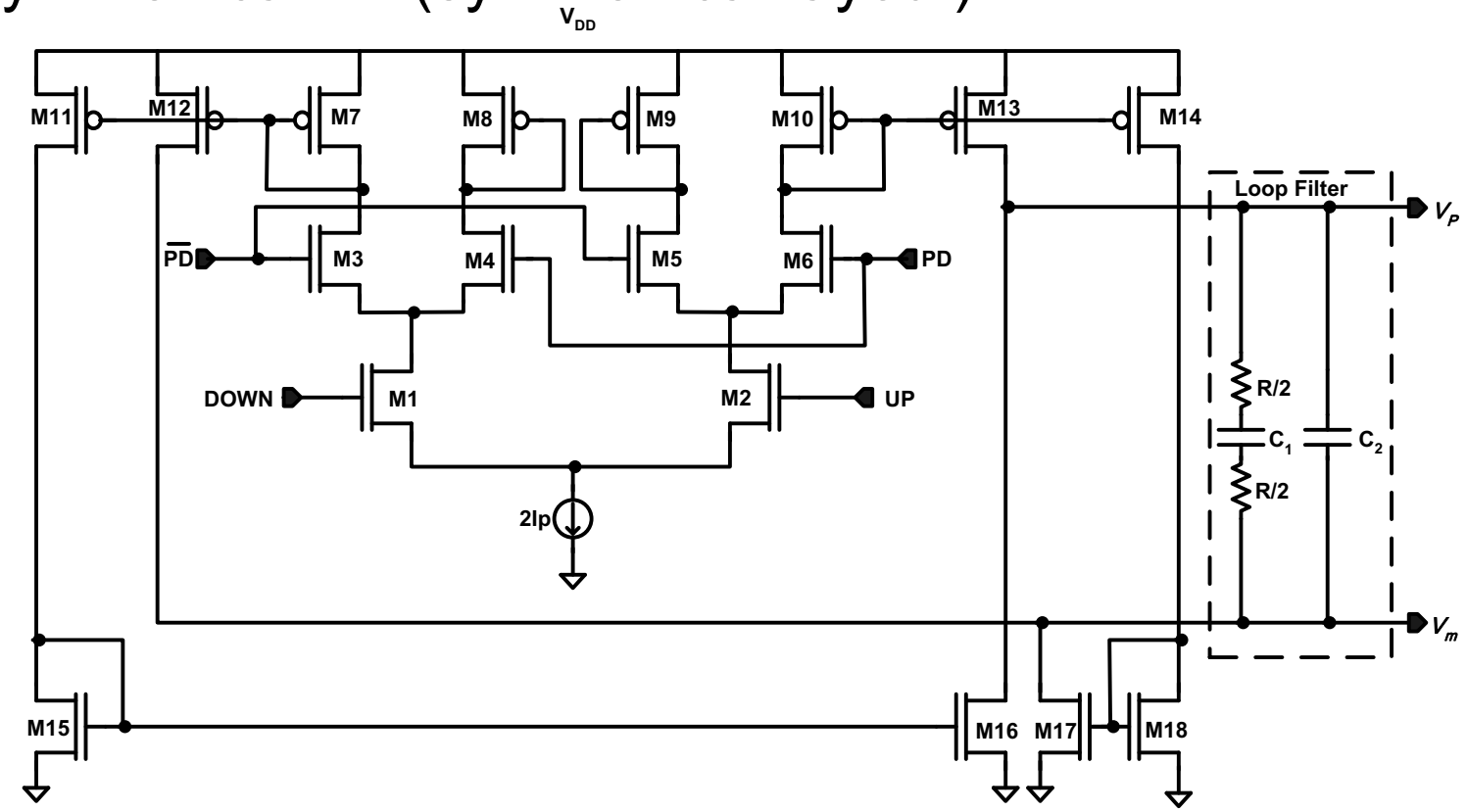
Fast turn-off CP [InK01]

- M_x and M_y ensure fast turn-off of M_{c1} and M_{c2}.
- $M_{d1\text{-}d4}$ reduce charge injection and clock-feedthrough
- Improved matching between UP and DOWN currents by using the dummy load structure.

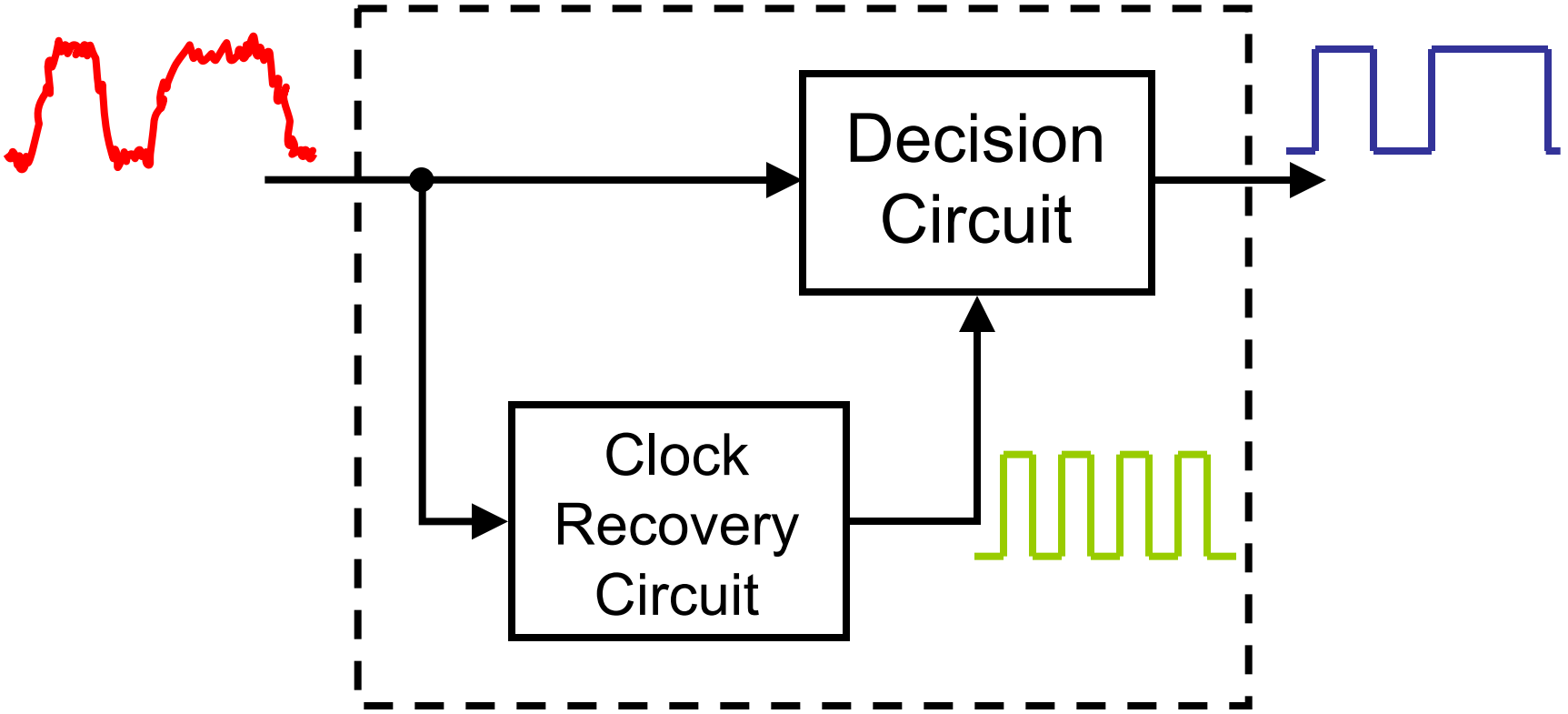


Fully Differential CP [DjS00]

- Different control lines for frequency and phase difference
  - faster frequency capture and smoother phase control
- Identical output paths for charging/discharging LF
- Symmetrical LF (symmetrical layout)



Clock and Data Recovery

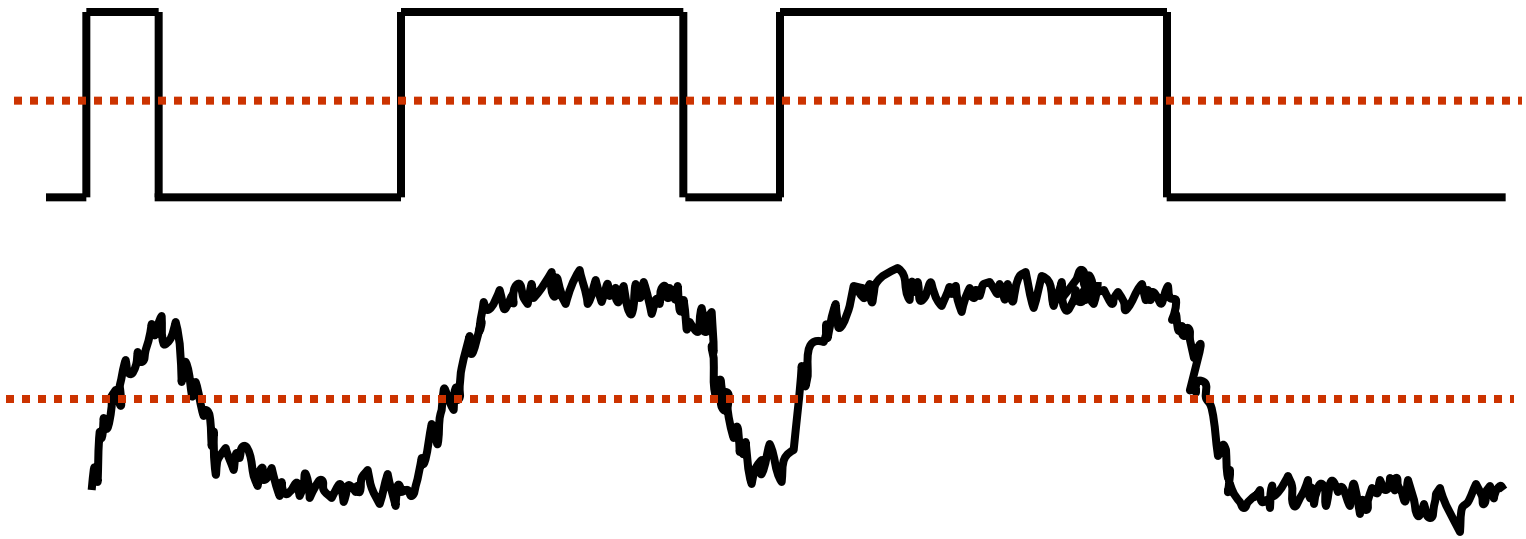


Signal Degradation Mechanisms

- Dispersion
- Baseline wander due to AC coupling
- Intersymbol interference
- Skin/dielectric loss
- Noise
- Connector discontinuties

Jitter

- Deviation of significant instances of a signal (e.g., its zero crossings) from their ideal location in time



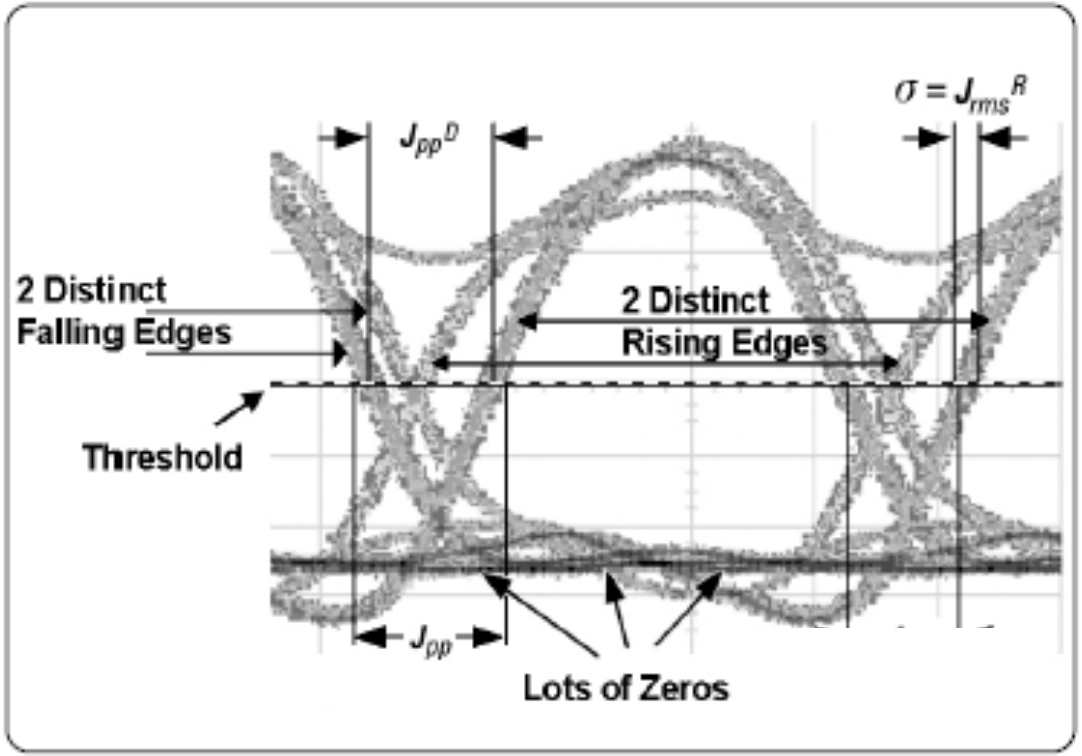
Jitter Measurements

- Based on time-domain (eye diagram):
  - Deterministic jitter
  - Random jitter
- Based on frequency-domain:
  - Jitter tolerance
  - Jitter transfer

Random and Deterministic Jitter

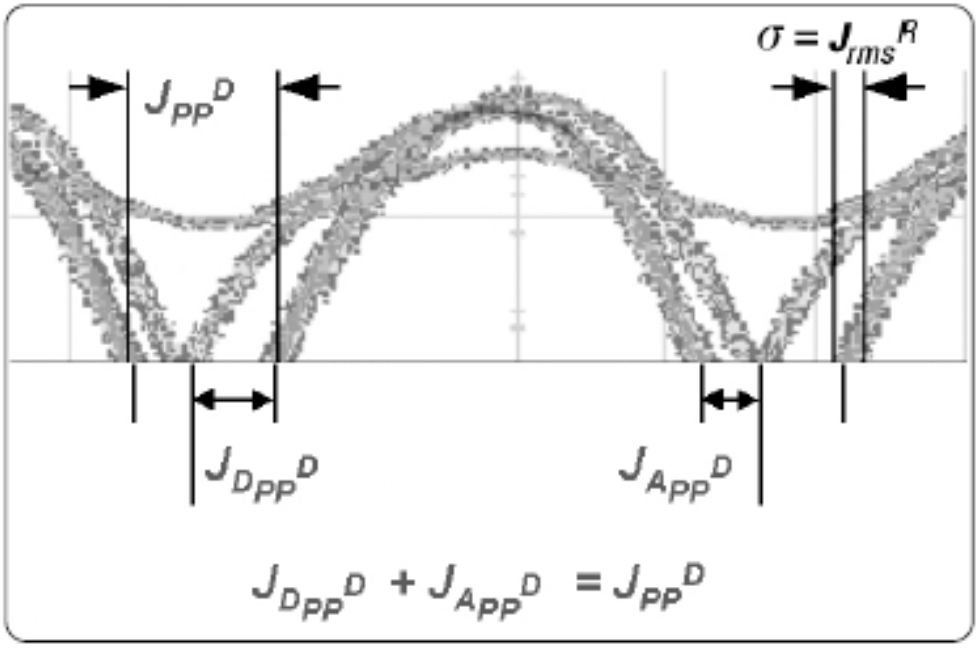
- Random Jitter (RJ)
  - Use a simple repetitive “clock-like” pattern as input.
  - Measure RMS jitter at zero crossings of eye-diagram
- Deterministic Jitter (DJ)
  - Use (pseudo-) random data as input
  - Measure peak-to-peak jitter at zero crossings
  - RJ contribution is subtracted from the measurement

RJ and DJ



Source: Agilent Technologies Application Note 1448-1

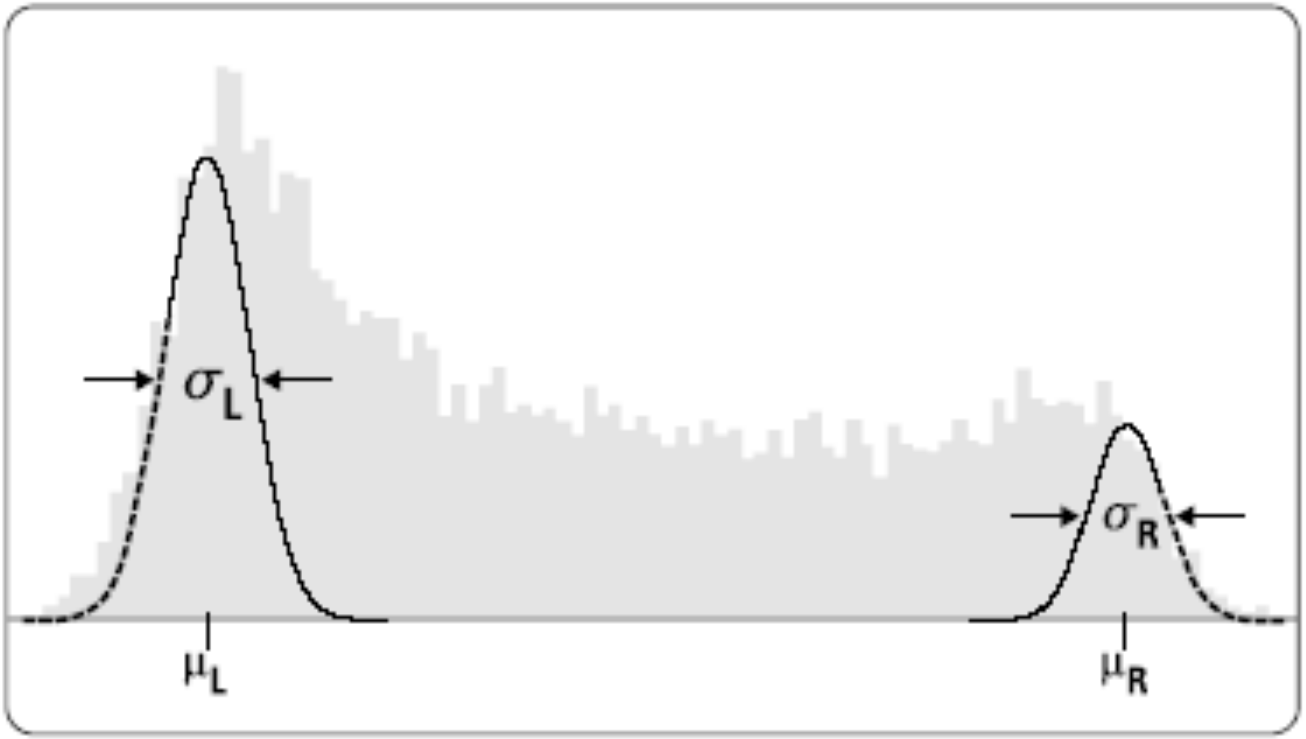
RJ and DJ



Source: Agilent Technologies Application Note 1448-1

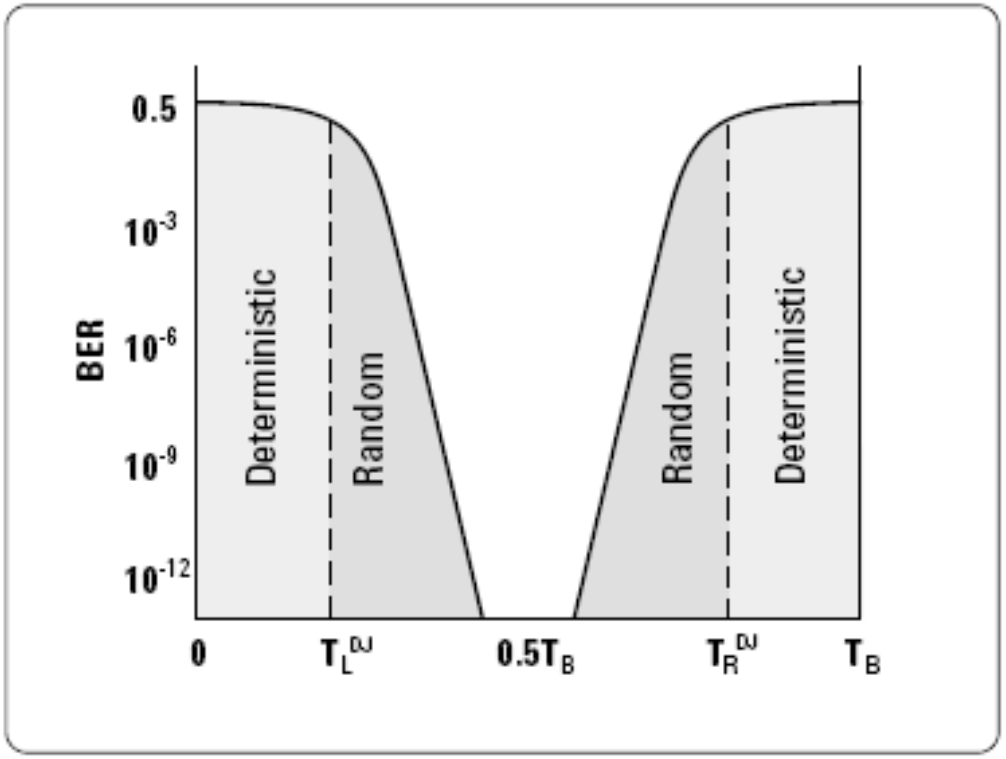
Separating RJ and DJ

- Use histogram of zero crossings



Source: Agilent Technologies Application Note 1448-1

Bath-tub Plot



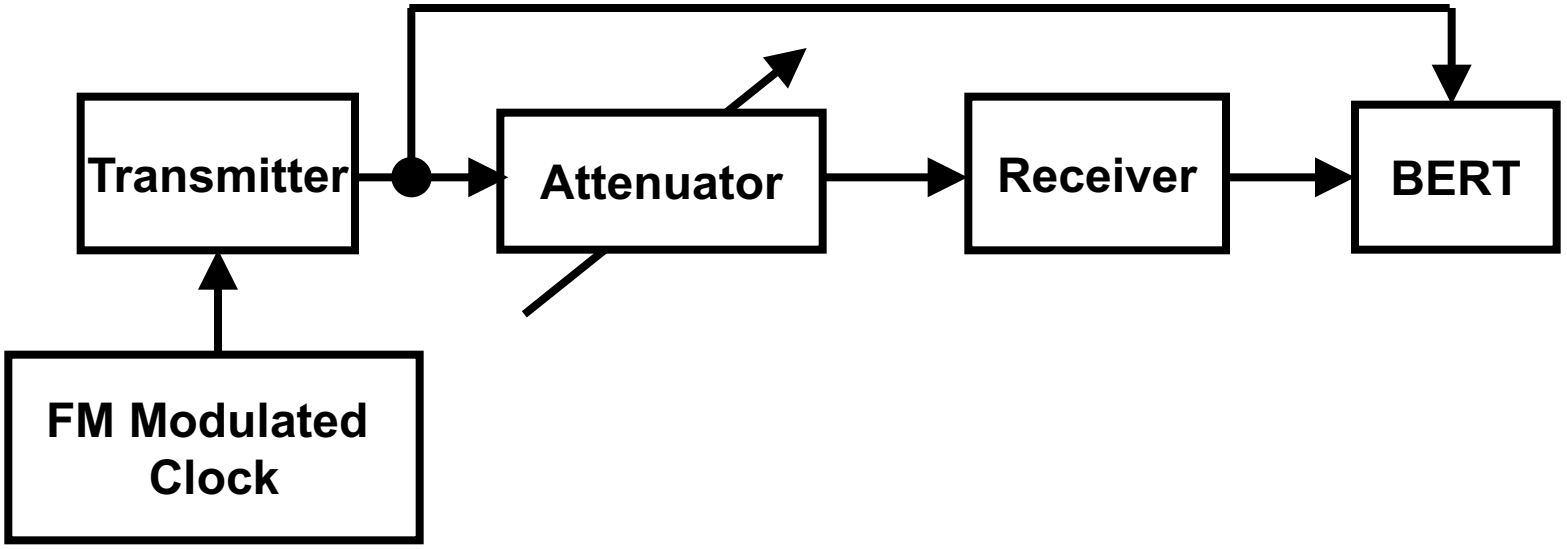
Source: Agilent Technologies Application Note 1448-1

Jitter Tolerance

- A measure of how a known amount of jitter affect the system performance (e.g., BER)

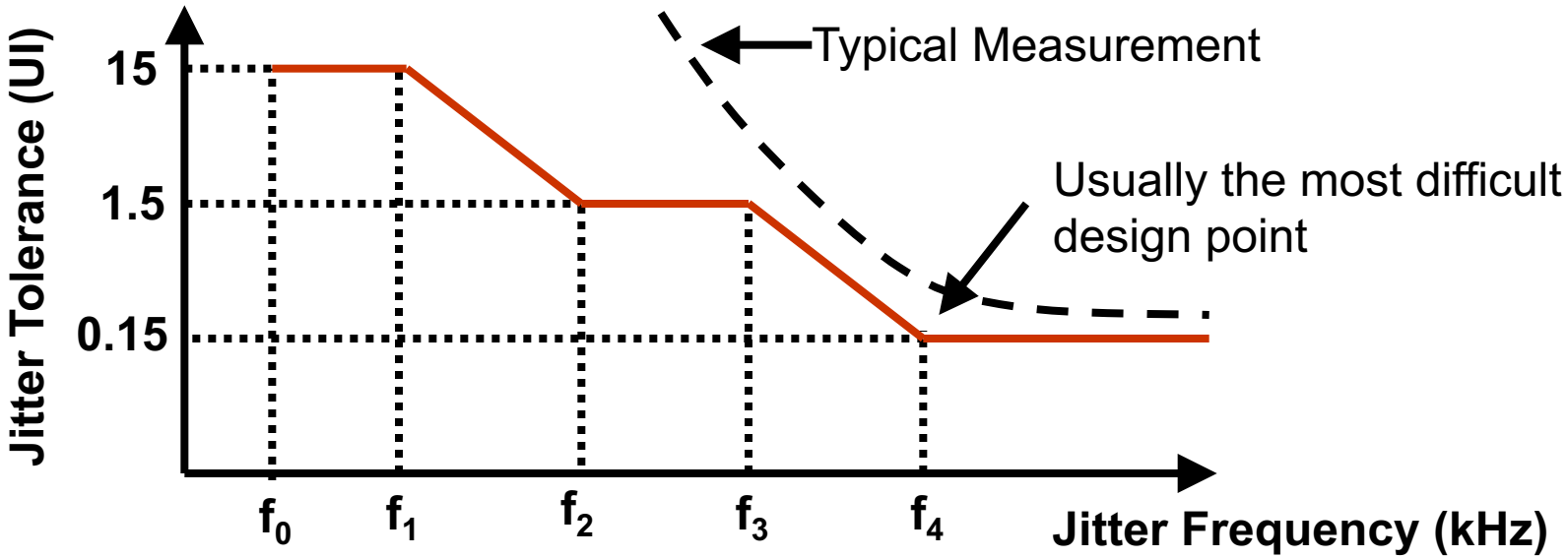
- In a CDR system jitter tolerance can be specified as the input jitter that the CDR system must tolerate without increasing the BER

Jitter Tolerance Measurement Setup



- In SONET jitter tolerance is the tolerable jitter until BER penalty is the same as that caused by 1dB optical attenuation

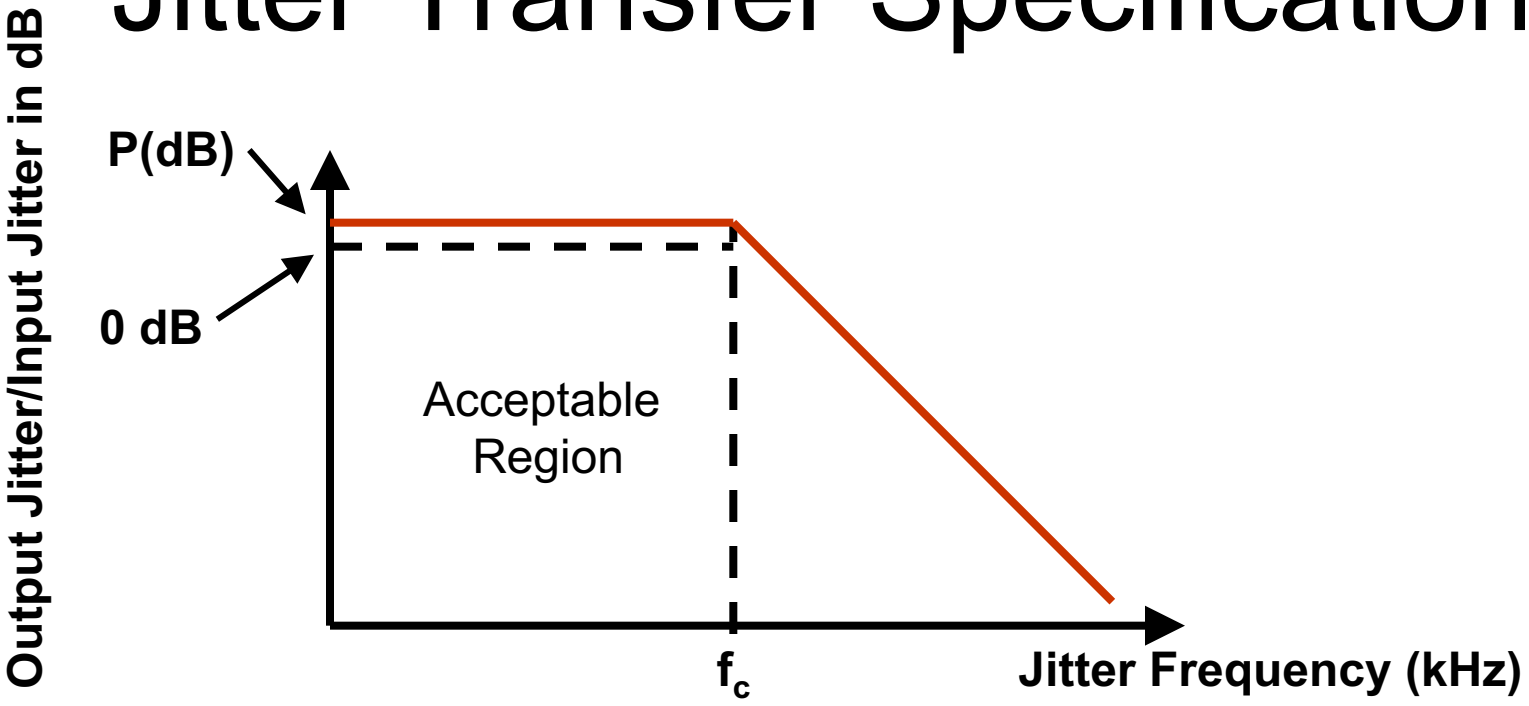
SONET Jitter Tolerance Mask



Data Rate	f_0	f_1	f_2	f_3	f_4
OC-3 (~155Mbps)	0.01	0.03	0.3	6.5	65
OC-12 (~622Mbps)	0.01	0.03	0.3	25	250
OC-48 (~2.5Gbps)	0.01	0.6	6	100	1000
OC-192 (10Gbps)	0.01	2.4	24	400	4000

SONET Spec: TA-NWT-000253 from ISSCC 2002 Short Course, Richard C. Walker

Jitter Transfer Specification

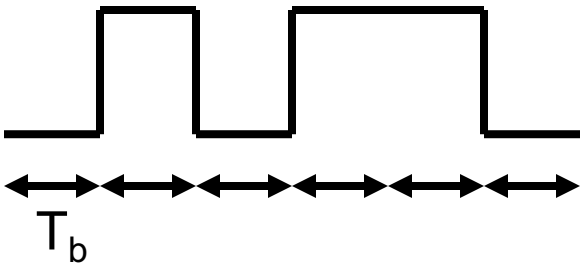


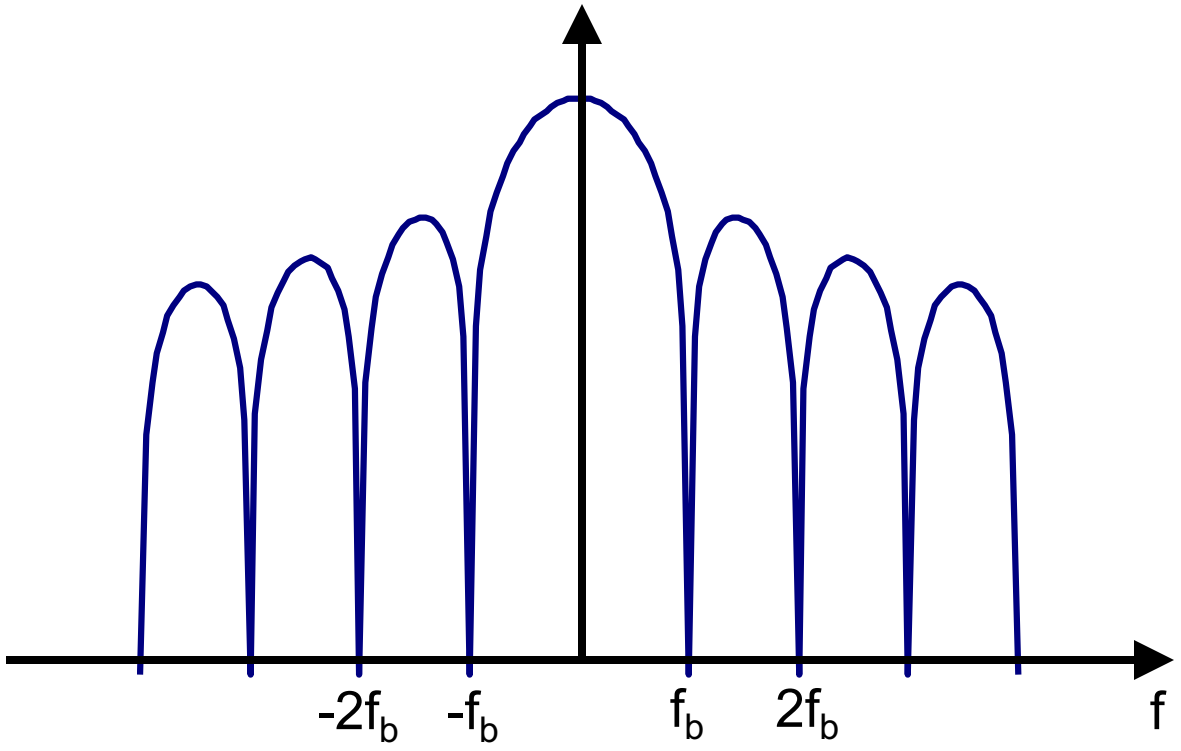
Data Rate	f_c(kHz)	P(dB)
156Mbps	130	0.1
622Mbps	500	0.1
2.5Gbps	2000	0.1

Important specification to control jitter peaking for channels with large number of repeaters

Random Binary Data

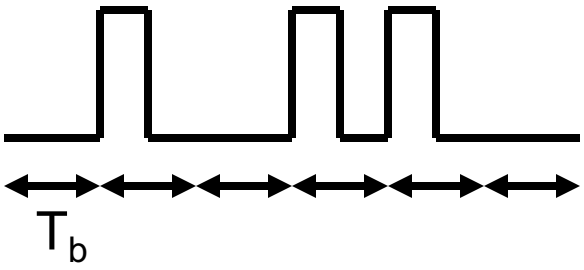
- Non-return to zero
- Power spectrum:

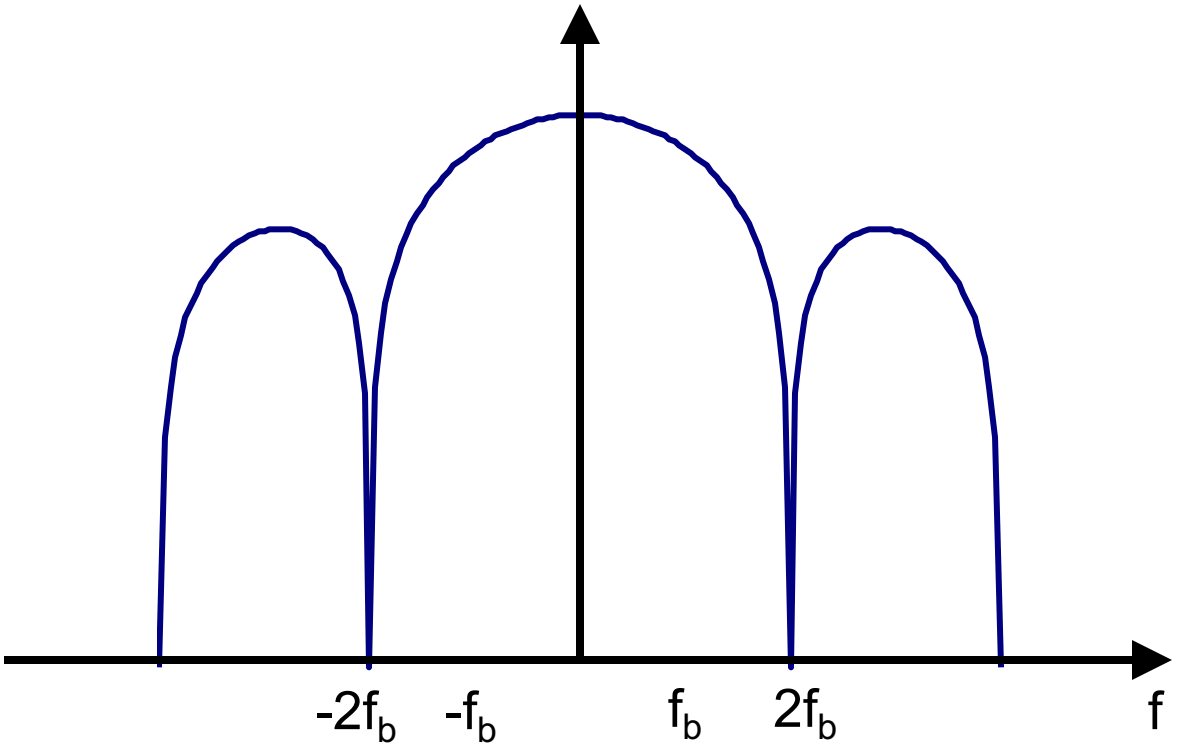




Random Binary Data

- Return to zero
- Power spectrum:





NRZ versus RZ

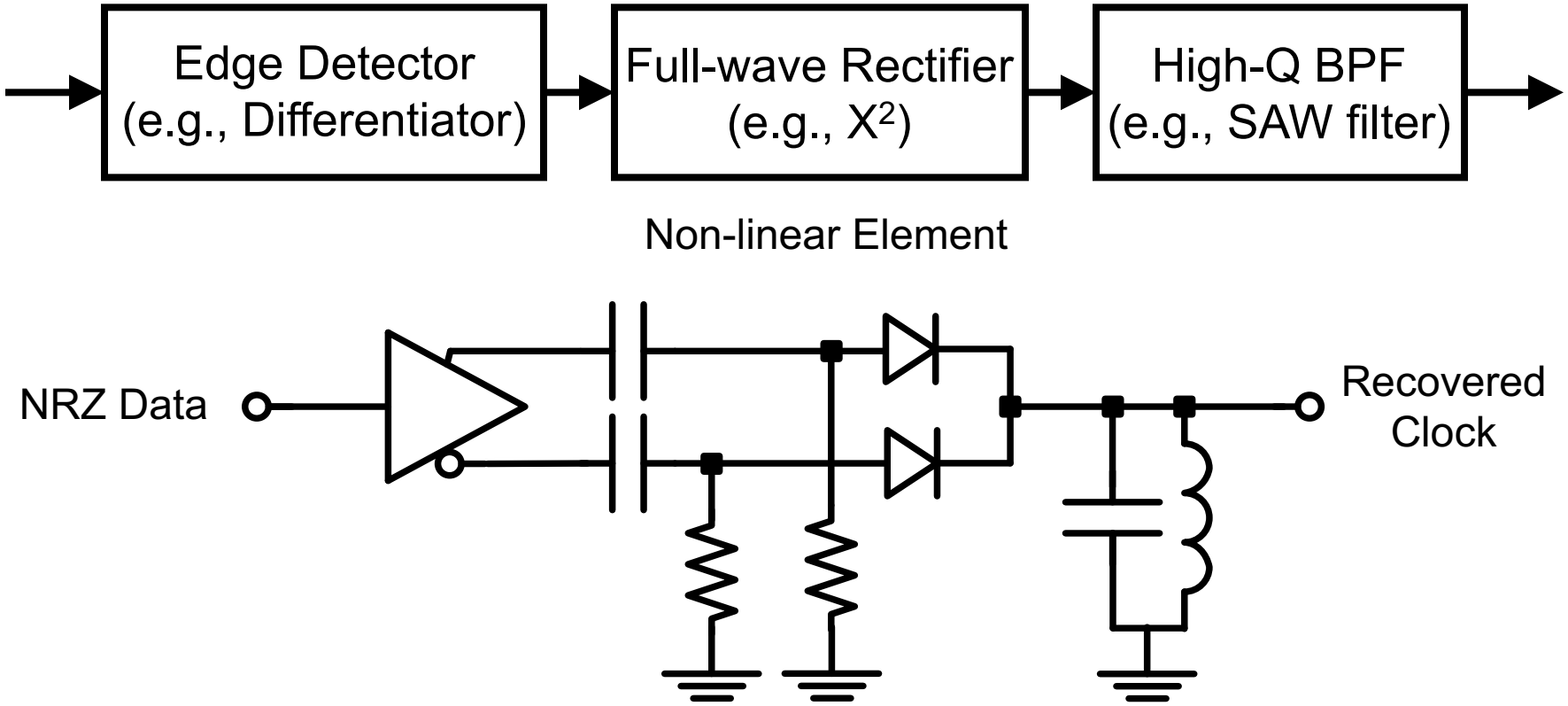
- NRZ is 2x spectrally efficient
- NRZ signaling is almost always used
- However, NRZ data spectrum has no component at clock frequency (more challenging clock recovery) and also susceptible to baseline wander (due to large run length)

Coding

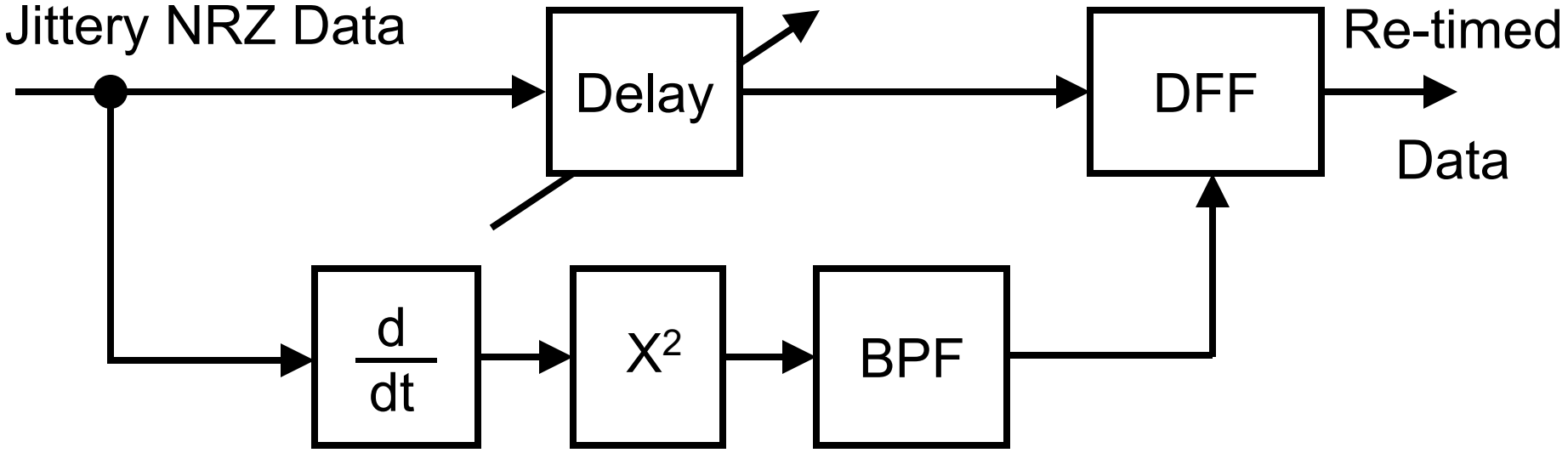
- Coding is generally used to:
  - DC balance and spectral shaping
  - Bounded run length
- High coding efficiency is desired
- Example: 8b/10b used in SONET

Filter based Clock Recovery

- Clock extraction

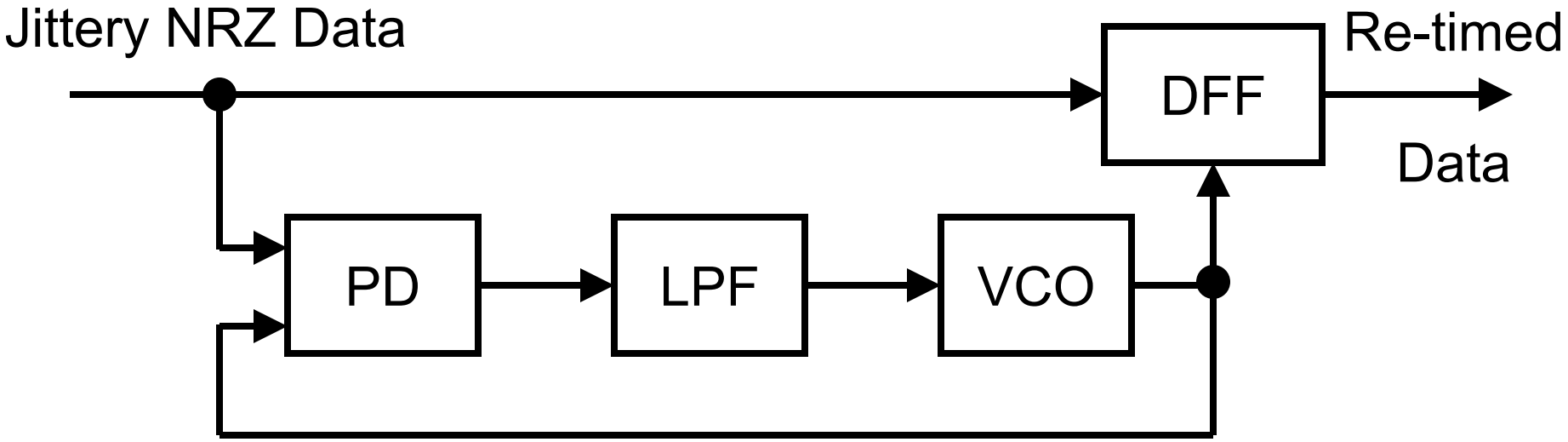


Filter based Clock Recovery

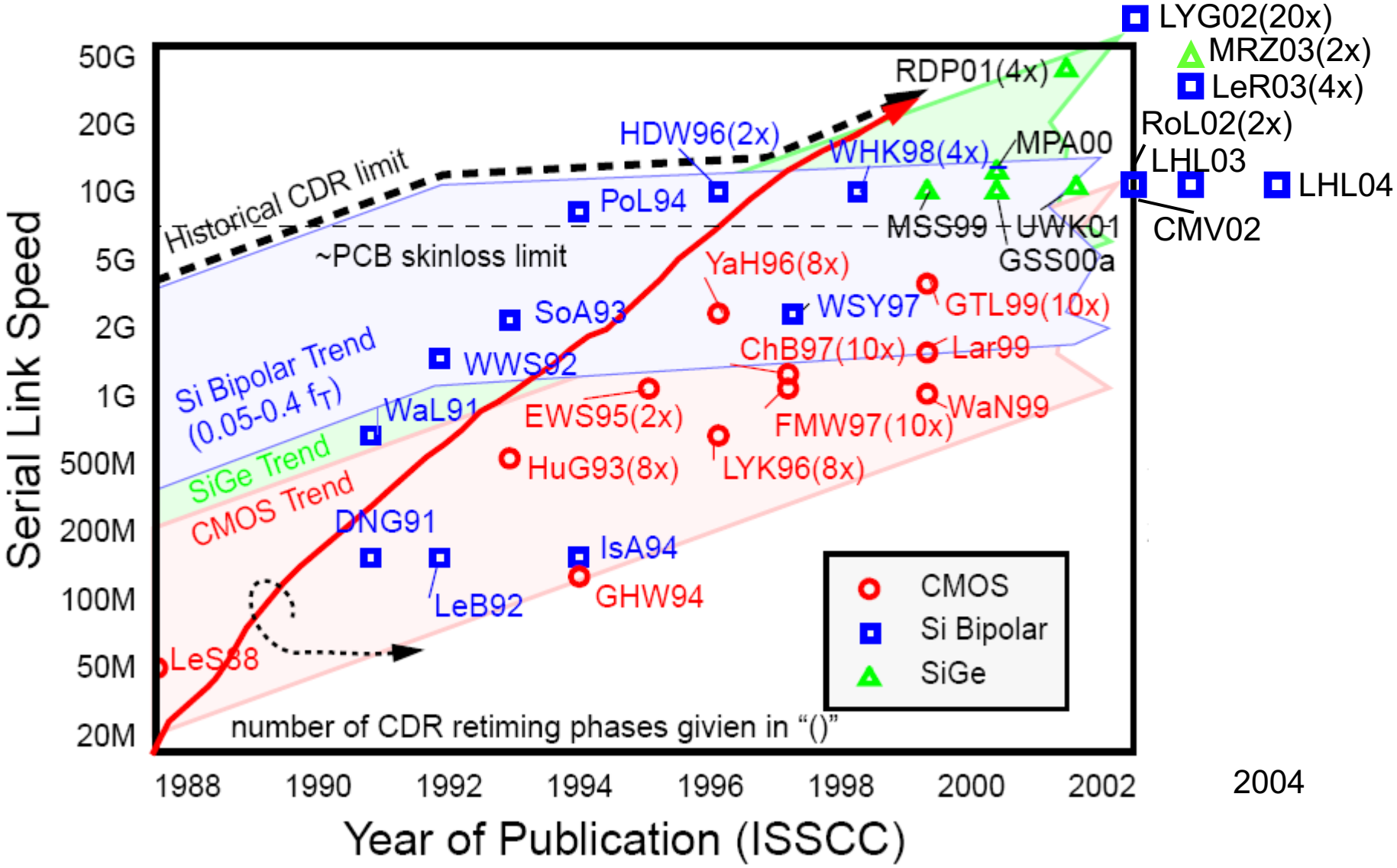


- Pros: Relatively simple discrete implementation
- Cons: Temperature and frequency variation of the filter, narrow pulse generation require high f_T, high-Q filter difficult to integrate

PLL Based Techniques



CDR data rates over time

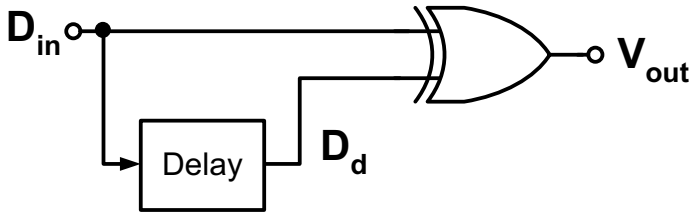


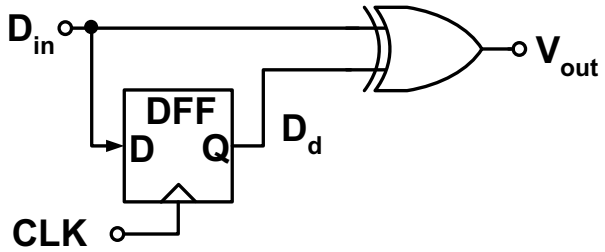
Source: ISSCC 2002 Short Course, Richard C. Walker

Phase Detector for CDR Systems

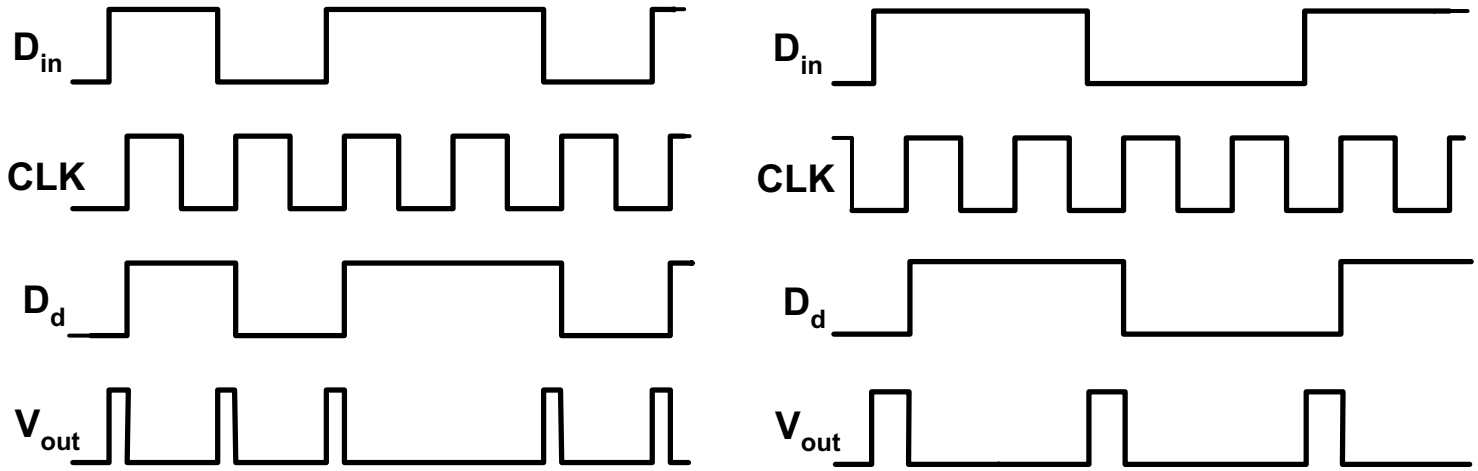
- Linear and bang-bang PDs
  - Hogge and Alexander types
- Full rate and fractional rate PDs

An Edge Detector as a Simple PD



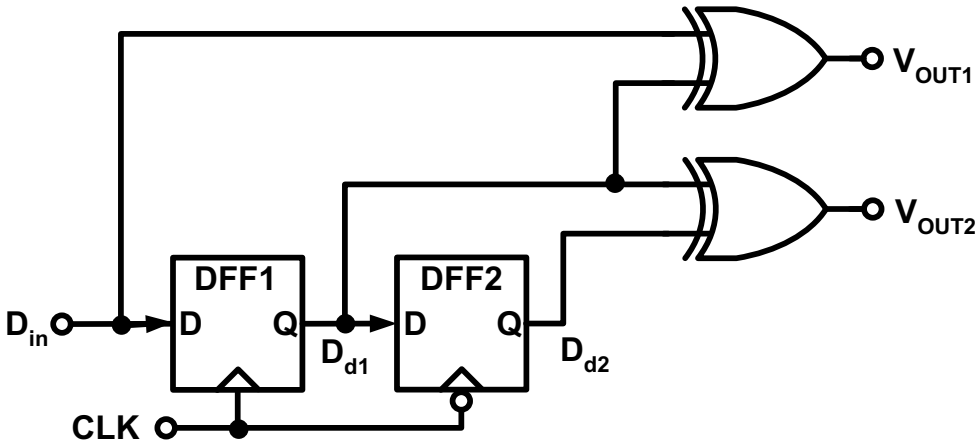


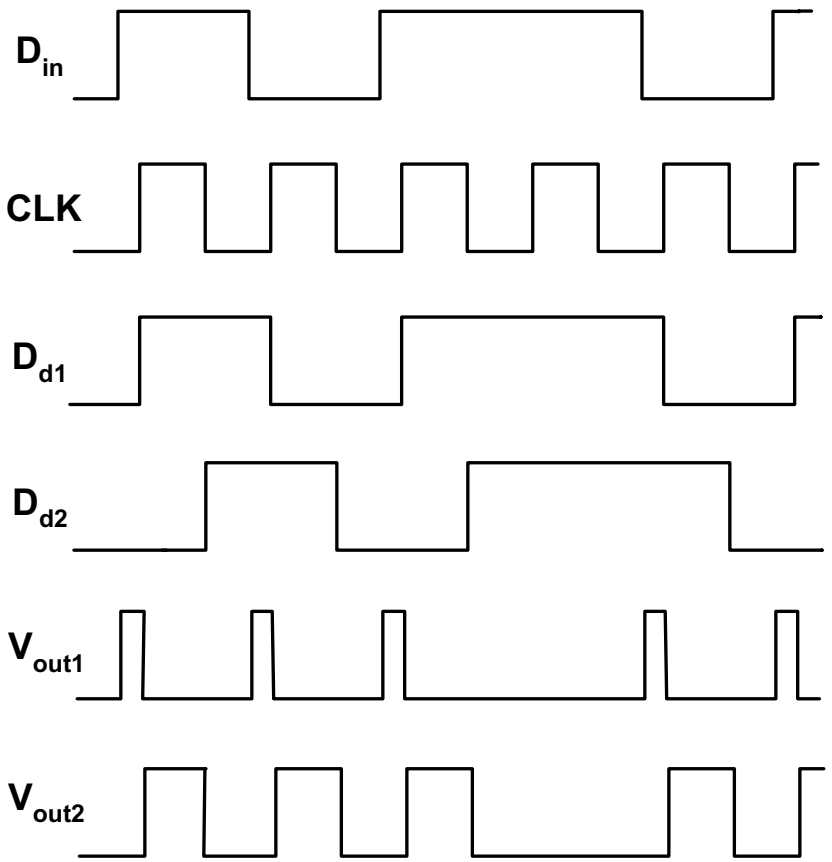
- Use FF as a delay element
- Problem?



Hogge PD

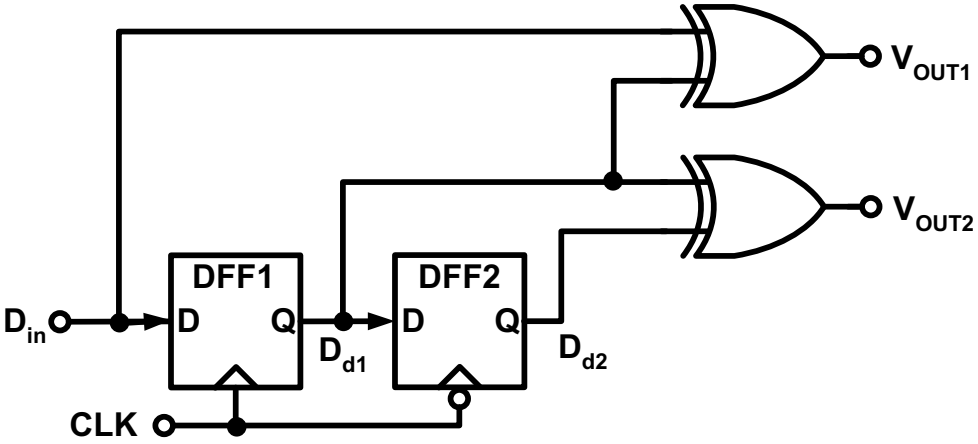
- Use a reference pulse to eliminate the pattern dependency

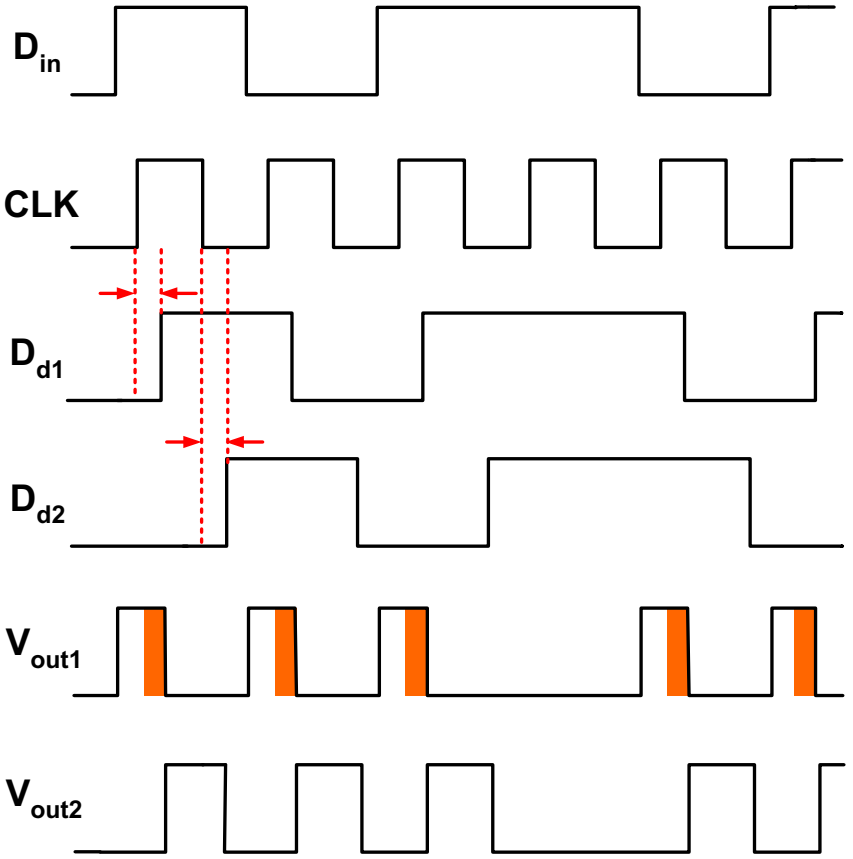




Effect of FF Delay

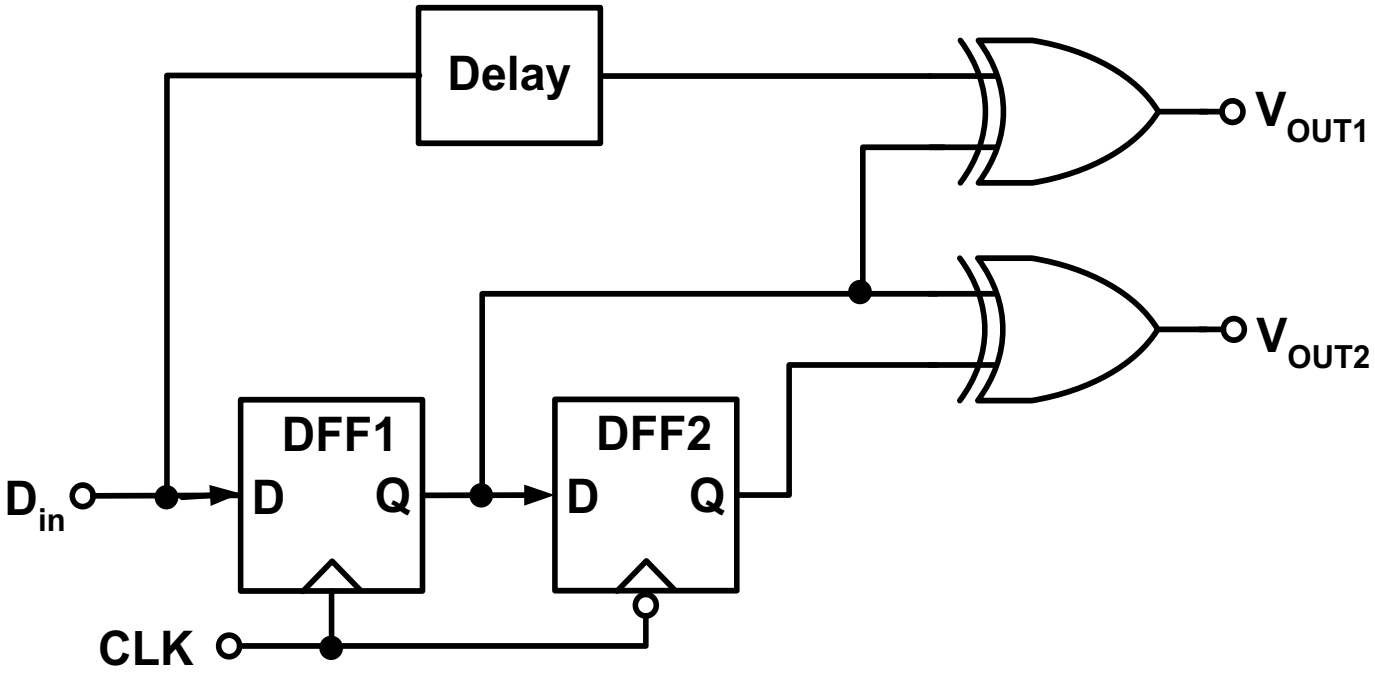
- Due to clock to Q delay of the FF the V_{out1} output pulses are wider.





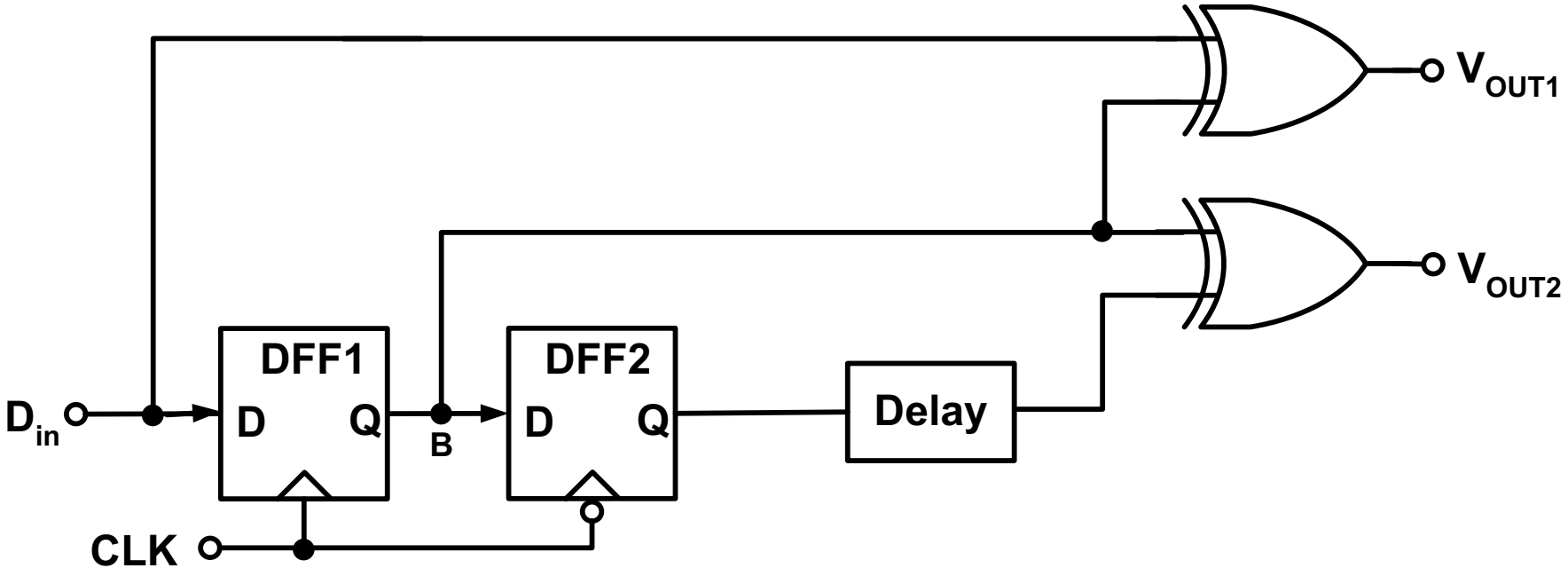
Delay Compensation in Hogge PD

- Add an equal delay in the data path



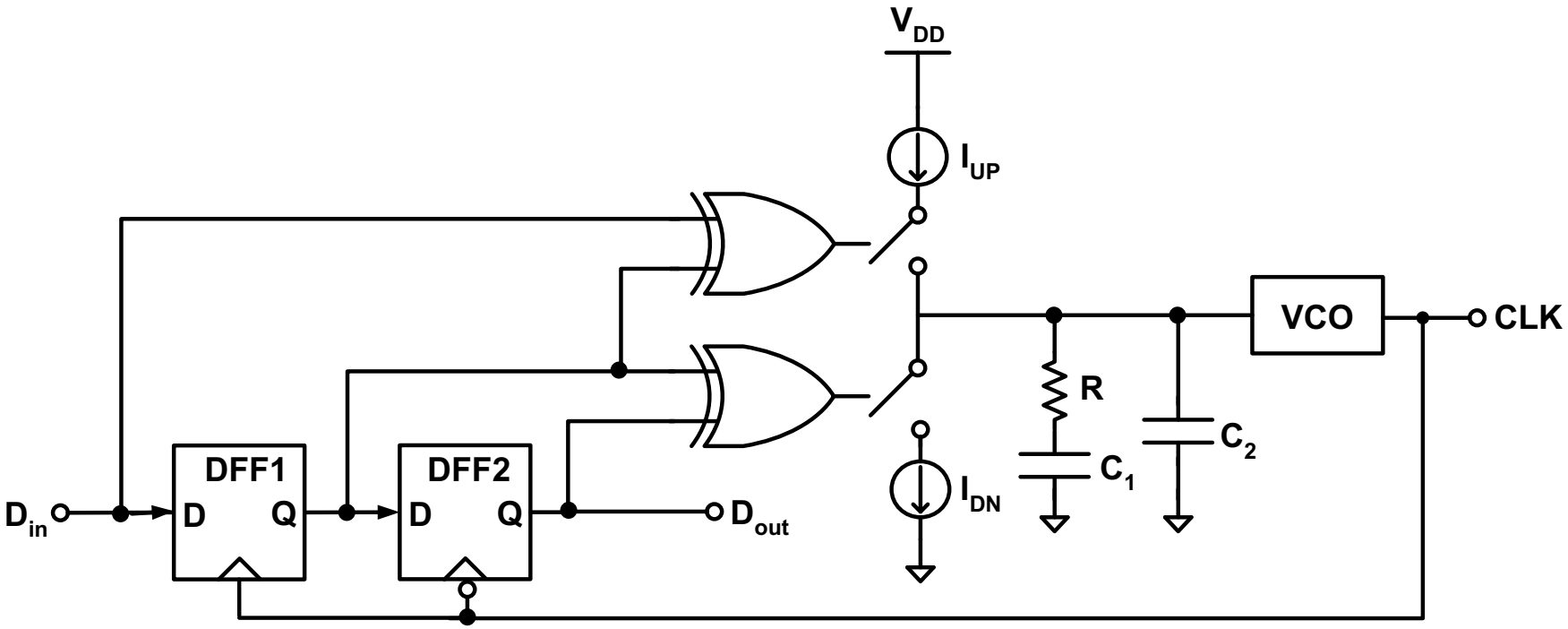
Delay Compensation in Hogge PD

- Widen the reference signal



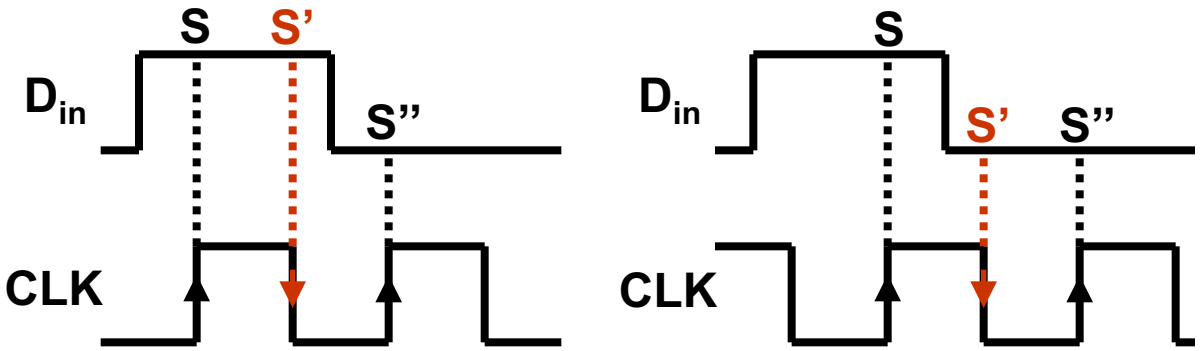
CDR System Using Hogge PD

- Simplified Hogge PD



Alexander PD (A Bang-Bang PD)

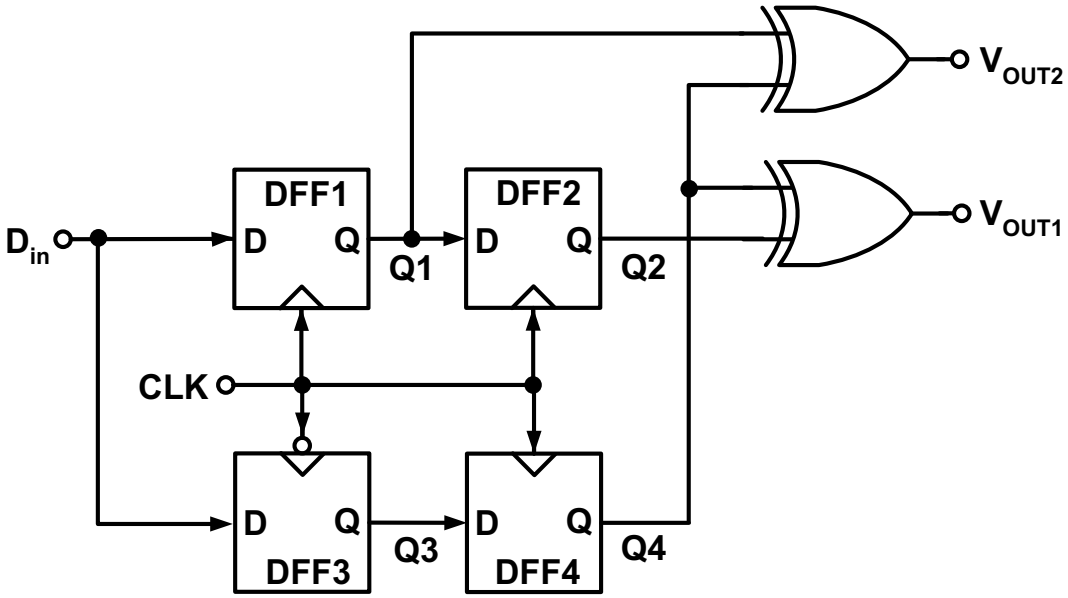
- Based on early-late detection principle

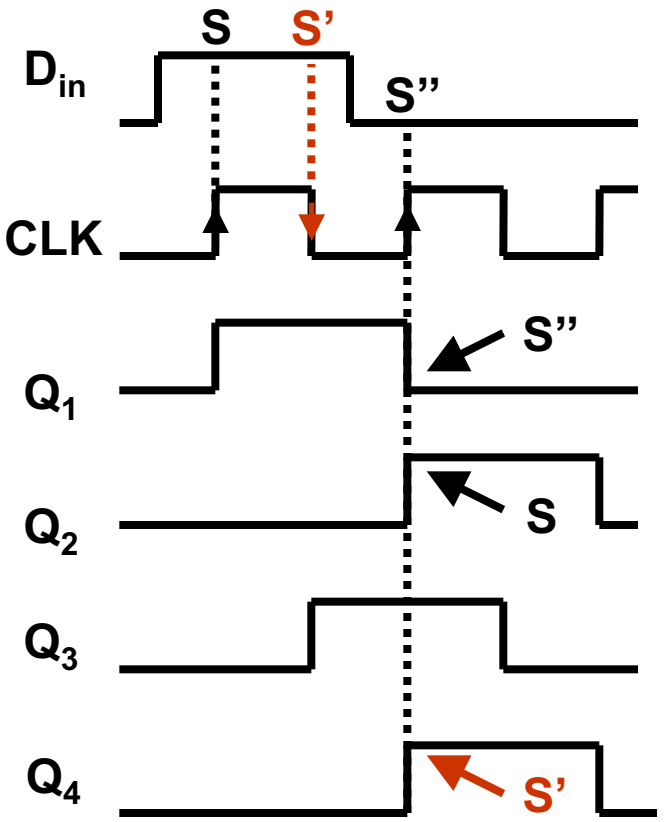


- Determine whether the falling edge of the clock is early or late with respect to data transition point

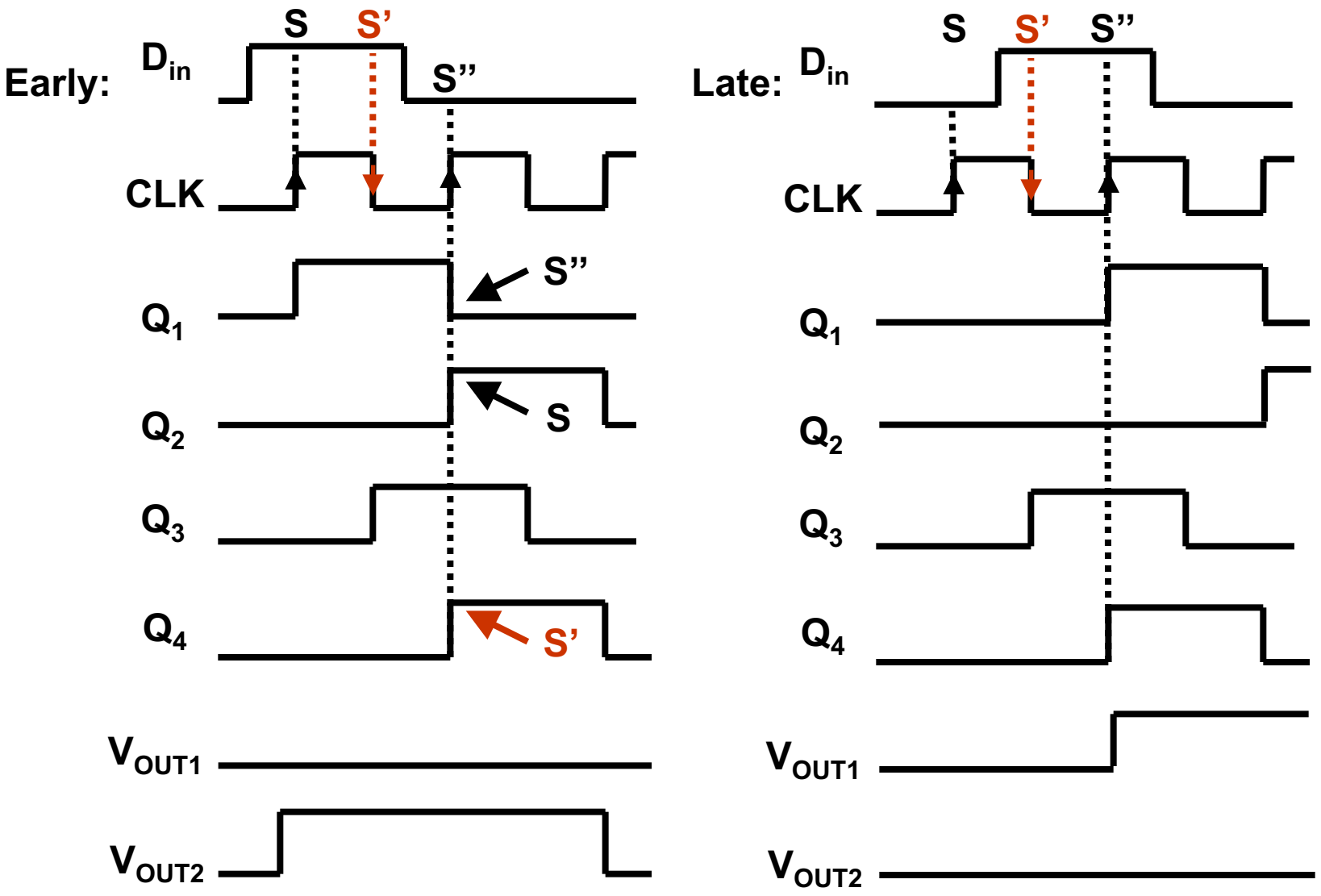
Alexander PD (A Bang-Bang PD)

- Based on early-late detection principle

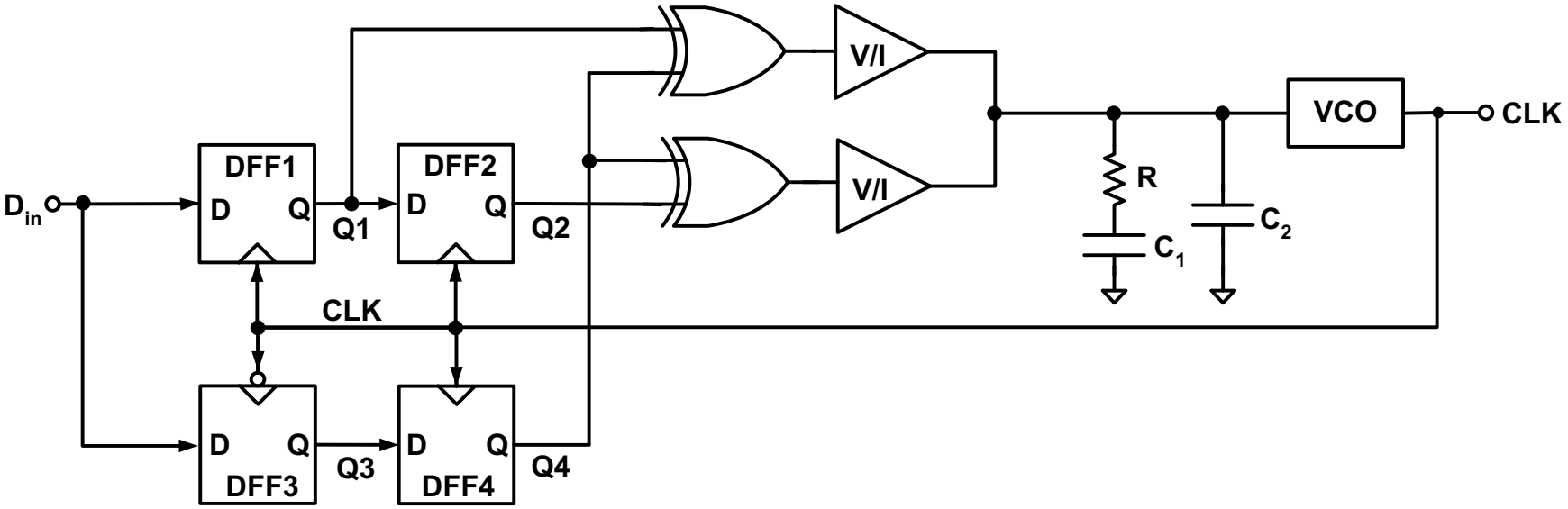




Alexander PD Waveforms



CDR System using Alexander PD

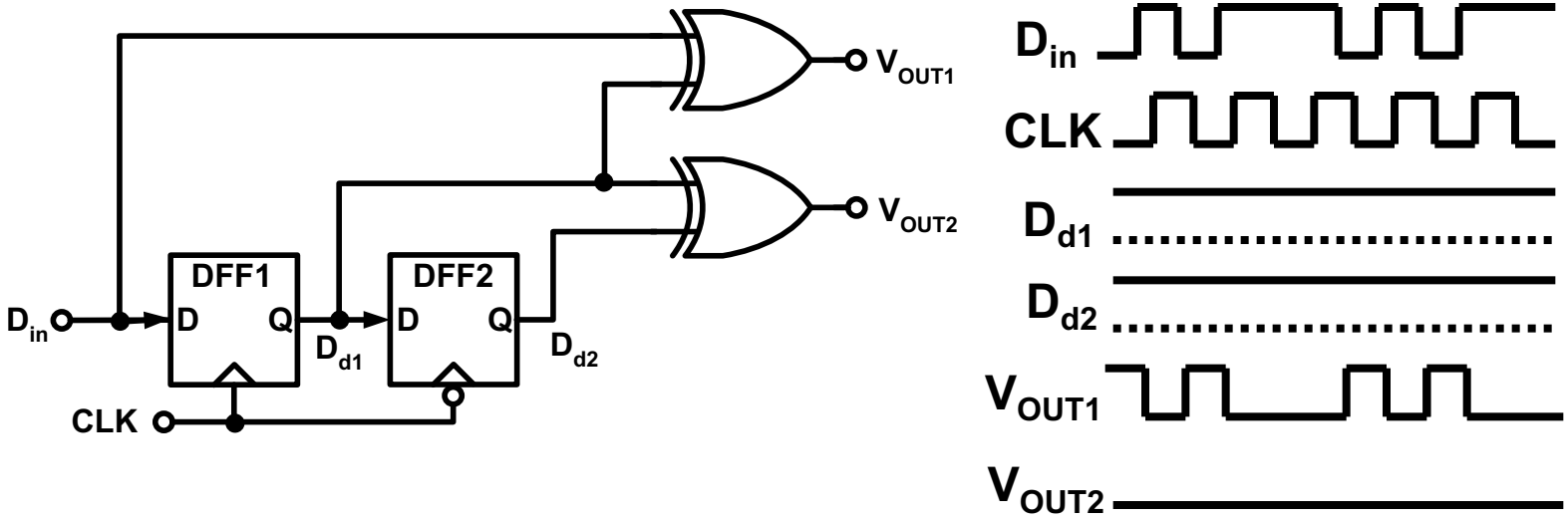


Fractional-Rate CDR Systems

- Design of high-speed adequately tunable clocks with reasonable jitter performance is challenging.
- Use a fractional rate clock (e.g., half-rate)
- The PD should be able to operate at the fractional clock rate.

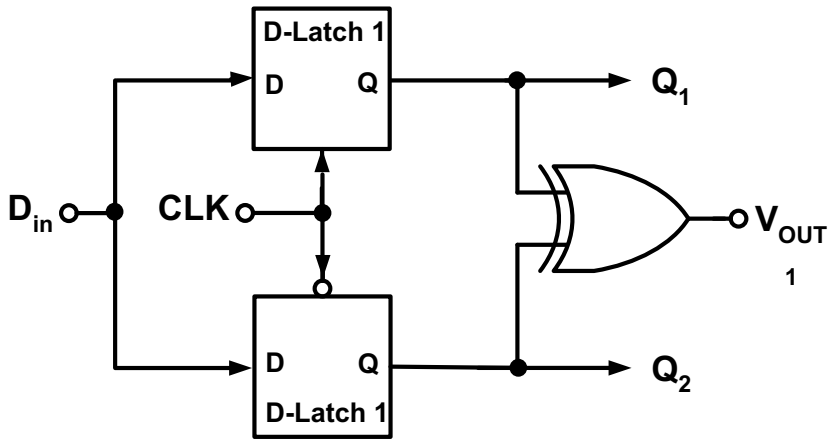
Half-Rate Hogge PD?

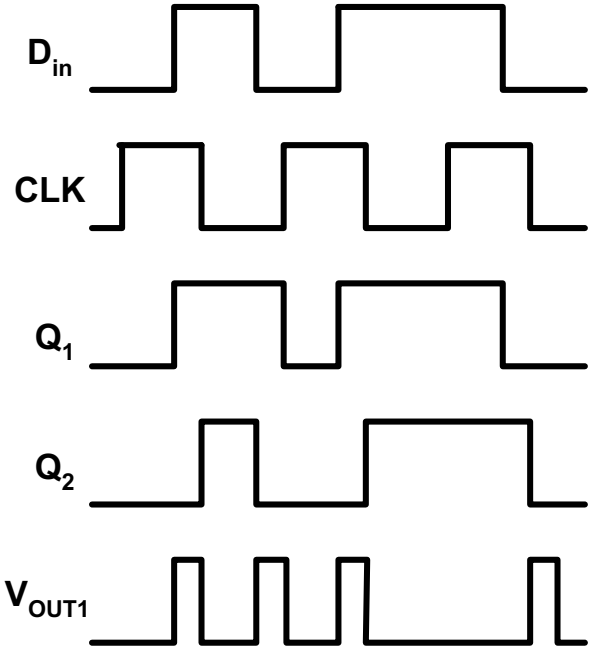
- Problem: Half of the clock transitions are missing, random data can be chosen such that all the samples have the same value.



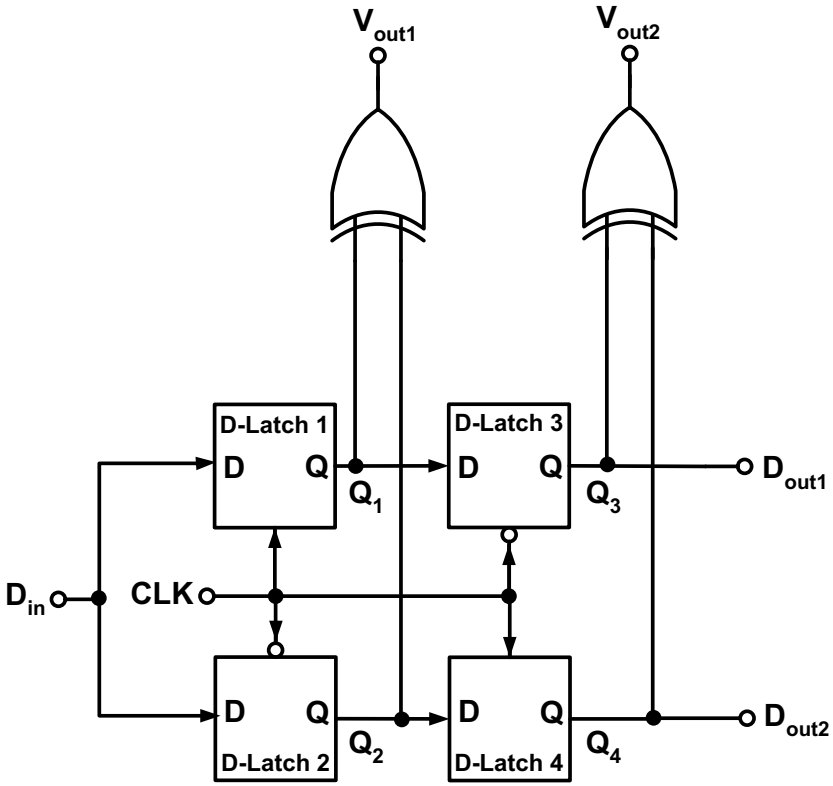
Simple Linear Half-Rate PD

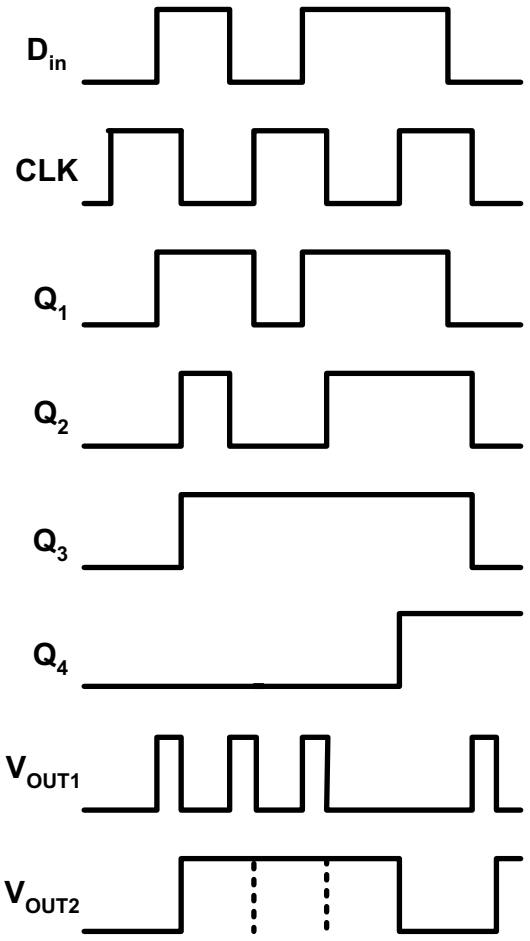
- Use both edges of the half-rate clock





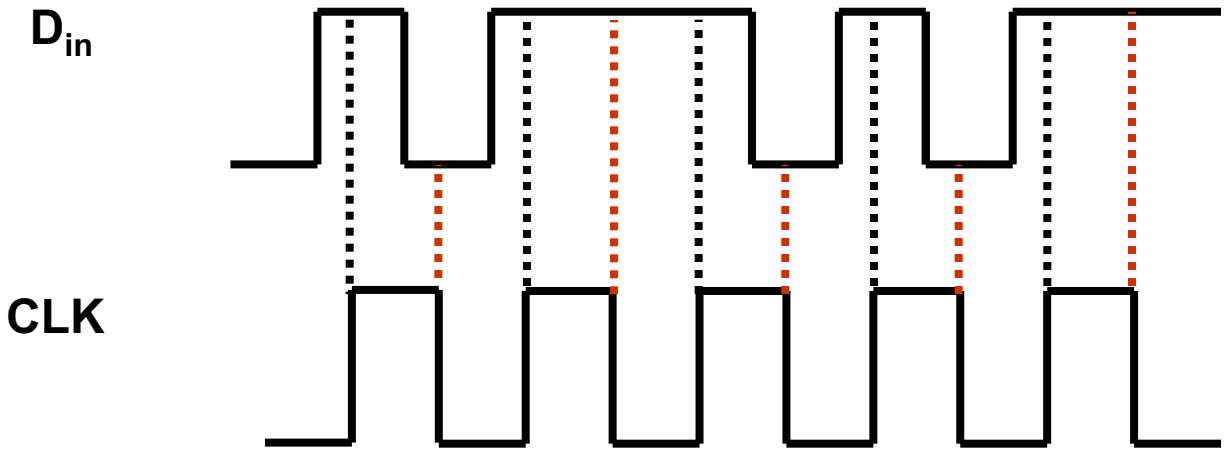
Complete Linear Half-Rate PD





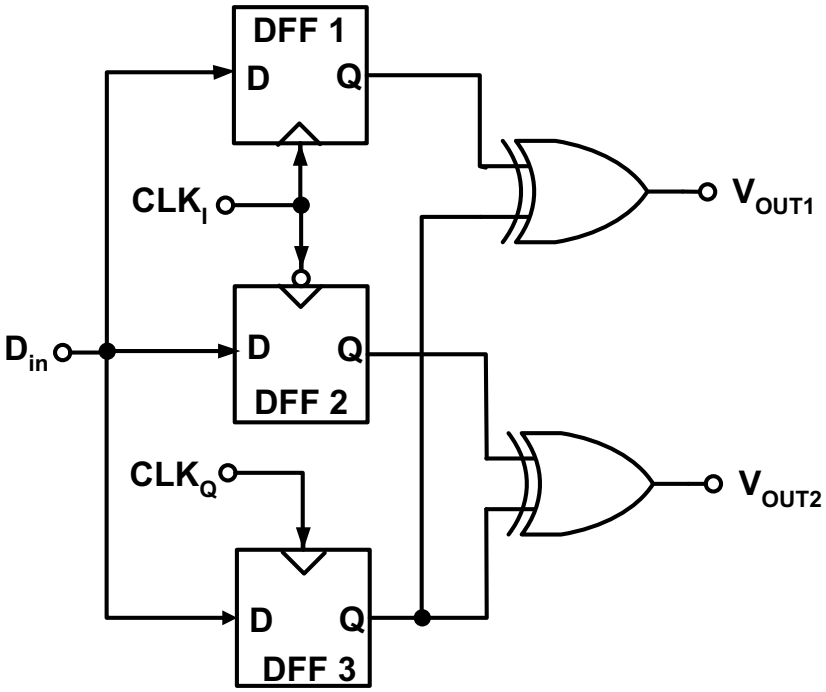
Half-Rate Alexander PD?

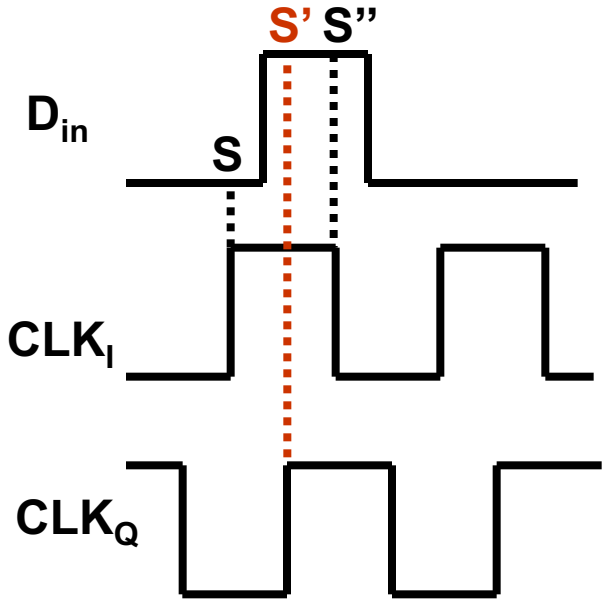
- Problem: Alexander PD already required sampling at both edges of the clock



Half-Rate Bang-Bang PD

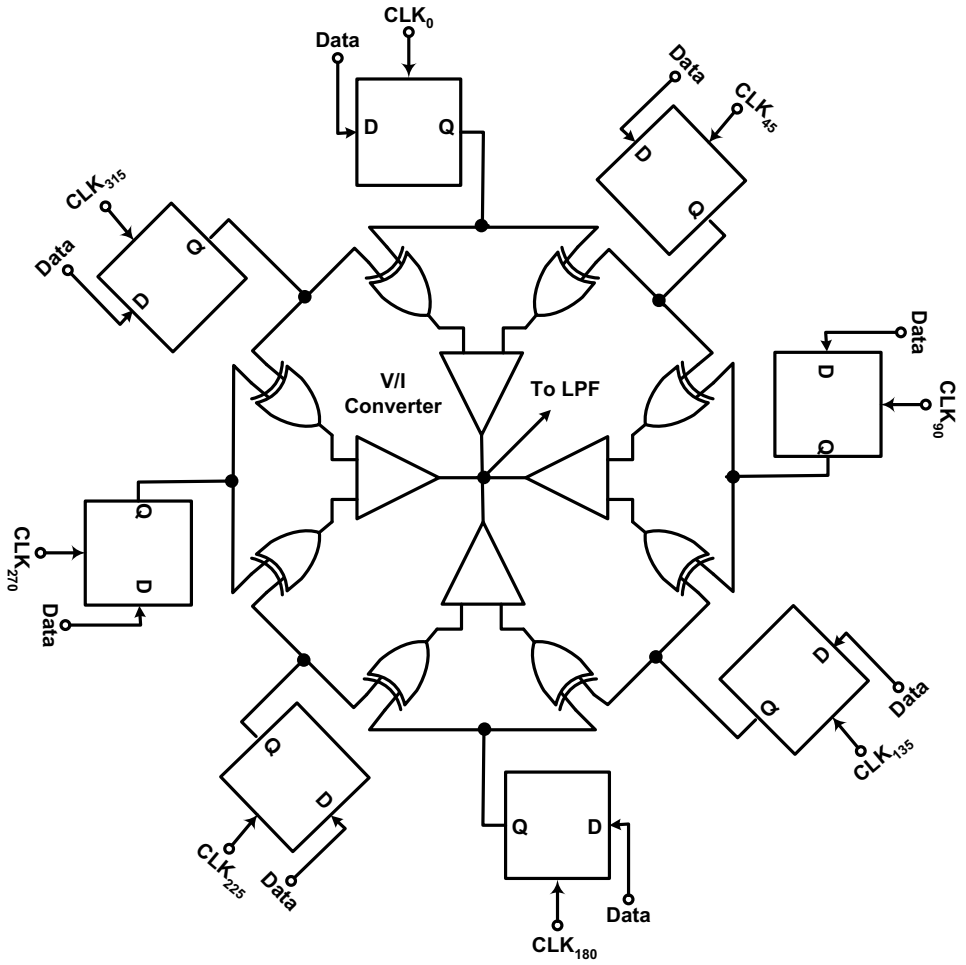
- Use both in-phase and quadrature clock phases



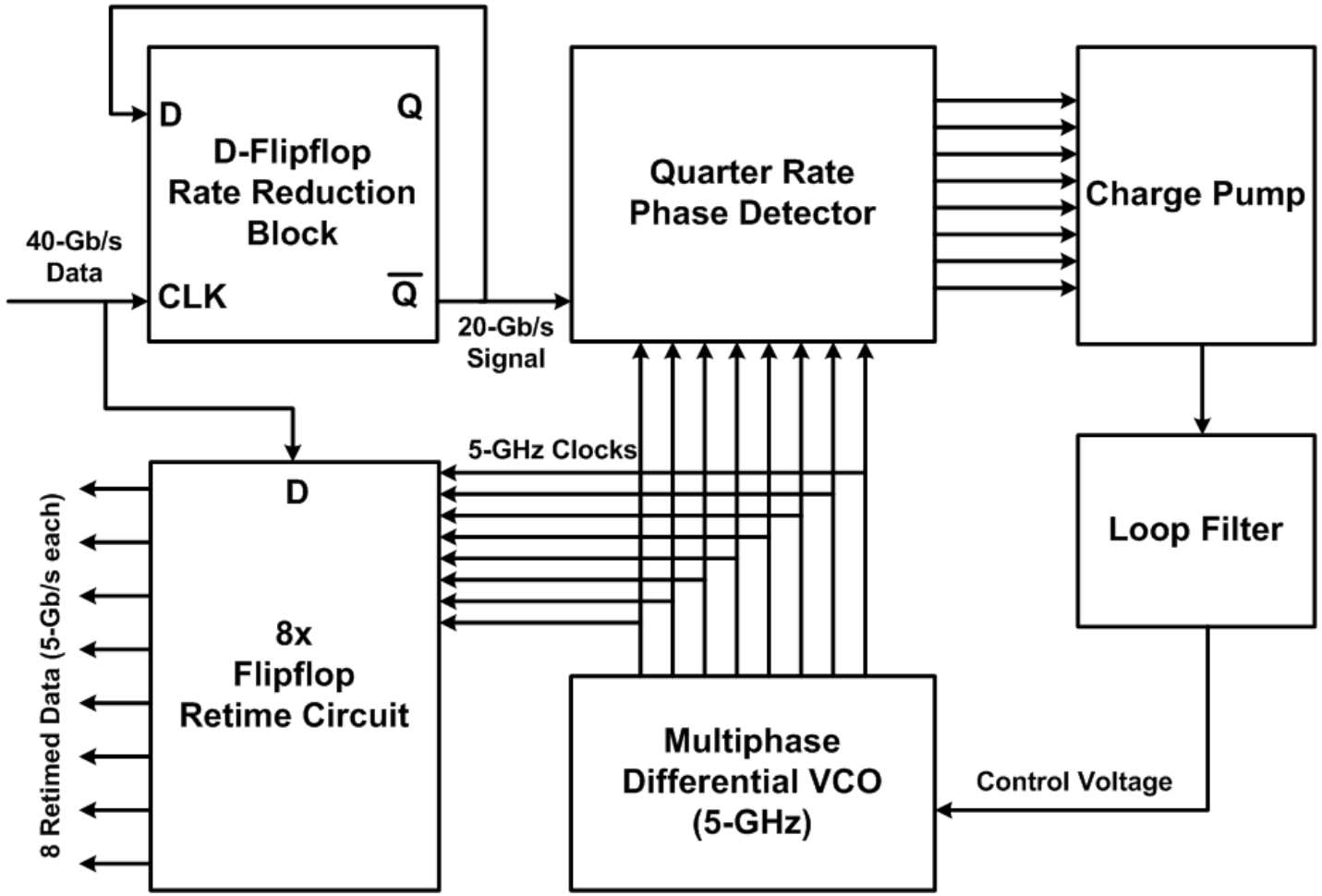


Quarter Rate BB PD [LeR03]

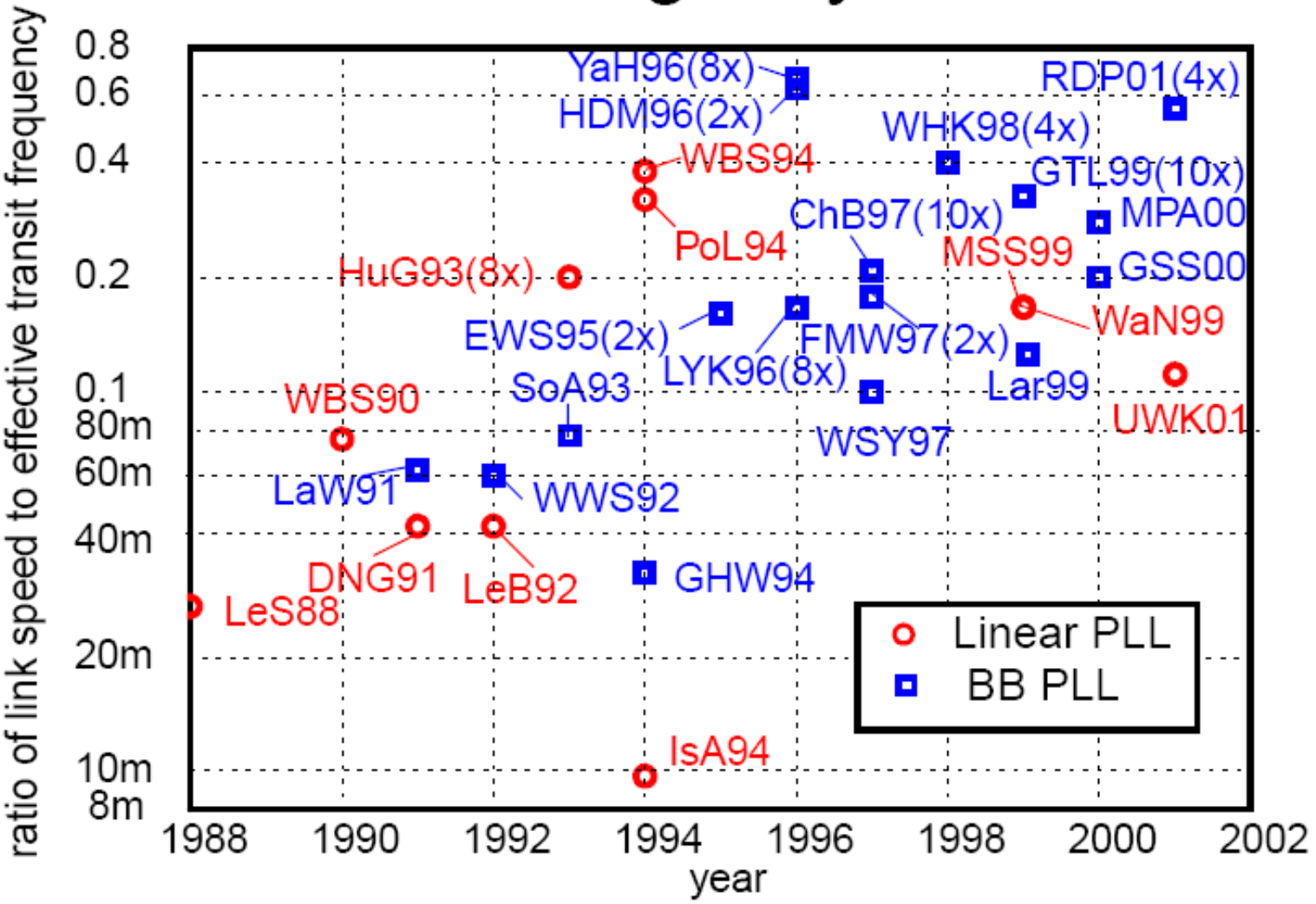
- Use multi-phase half quadrature clocks



1/8-Rate CDR System [SaM04]



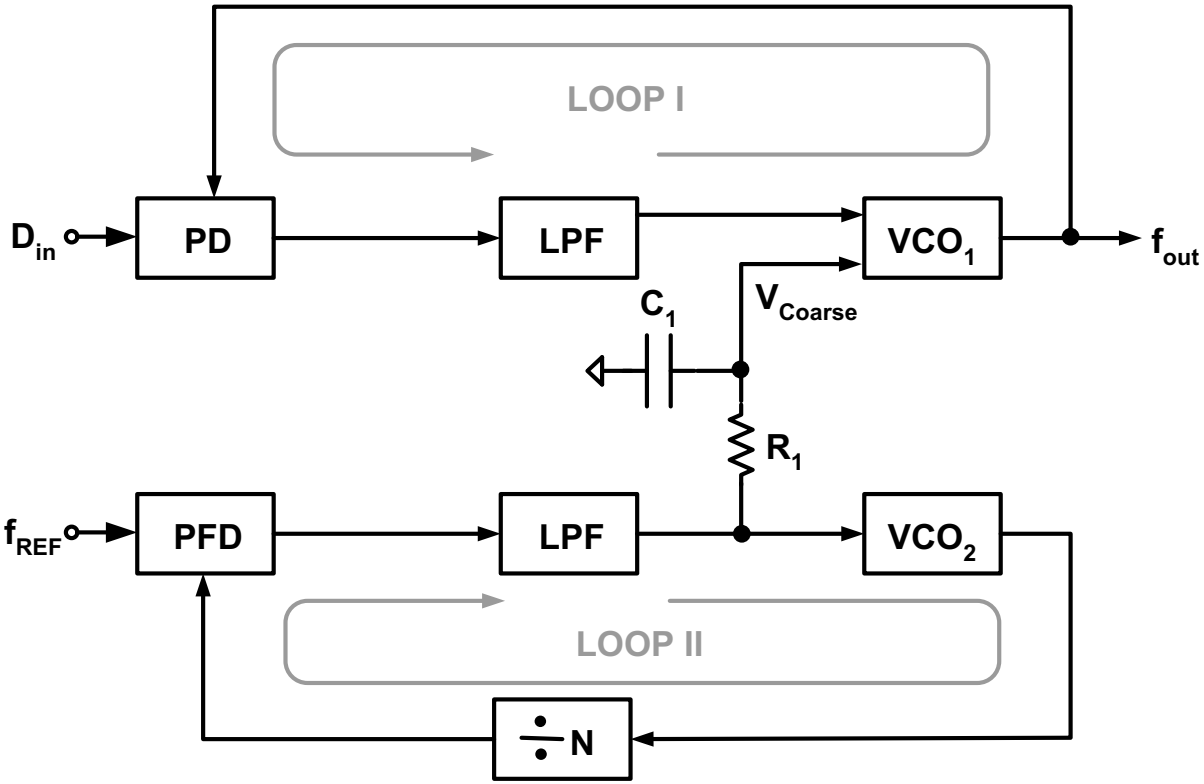
CDR PLL design style over time



Source: ISSCC 2002 Short Course, Richard C. Walker

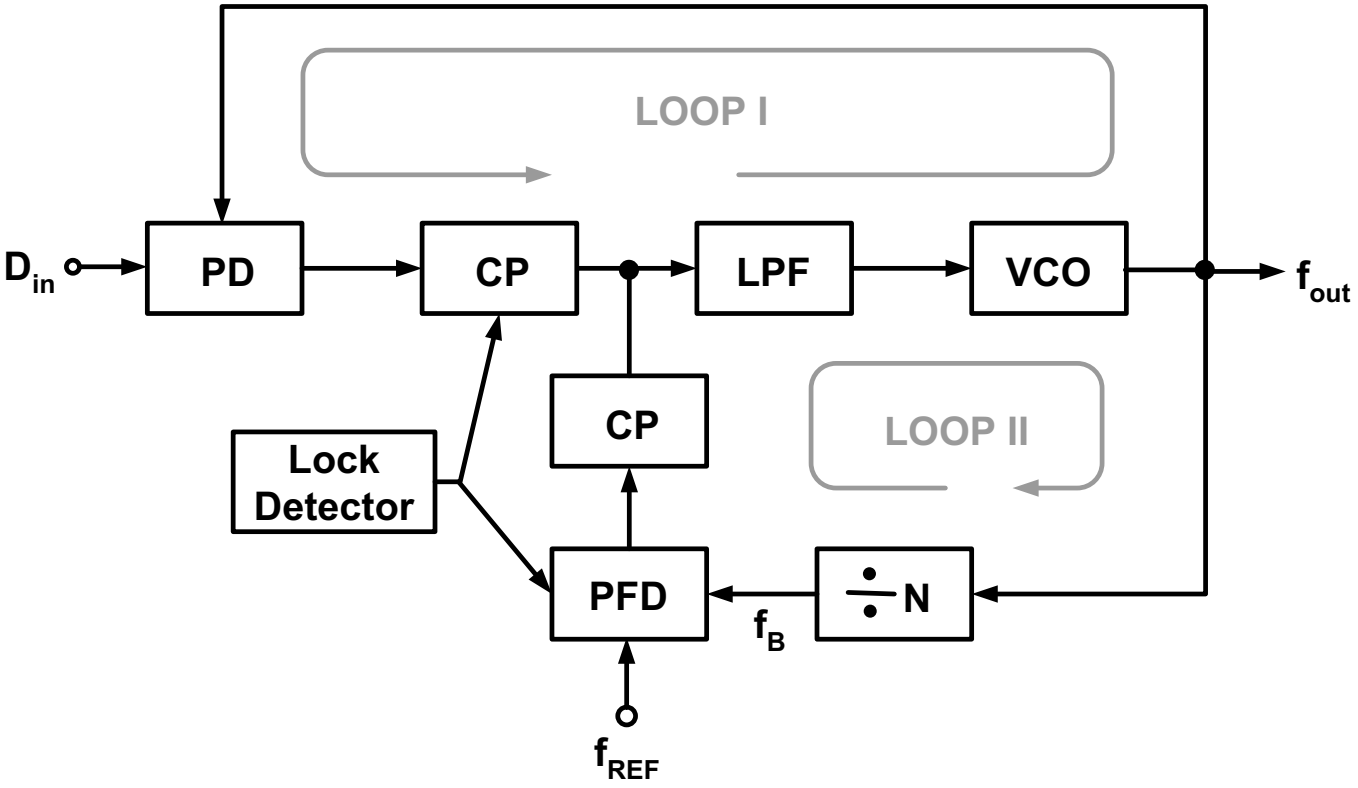
CDR Architectures

- Dual VCO architecture



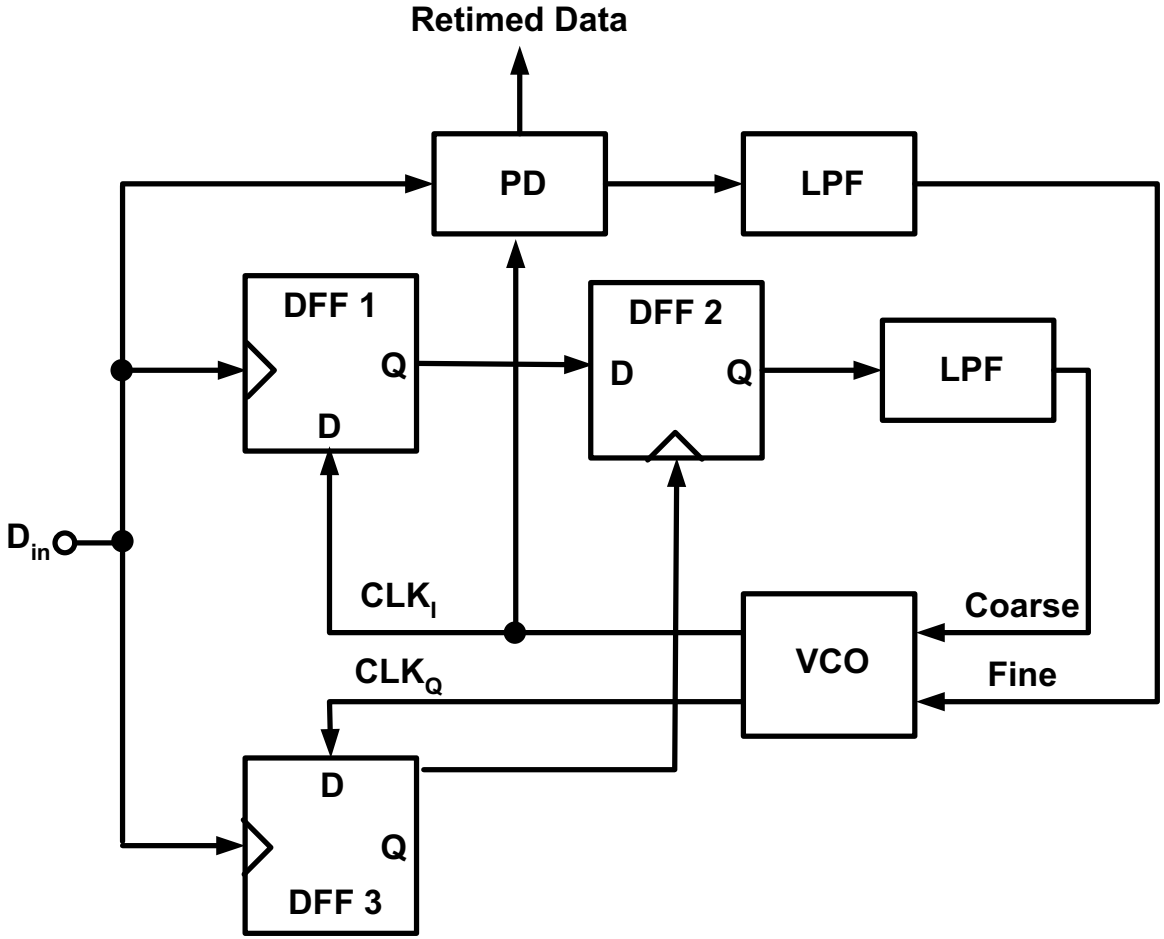
CDR Architectures

- Dual loop architecture with external reference



CDR Architectures

- Full rate CDR with both FD and PD



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1. Most of the references that are prior to 2002 are taken from ISSCC 2002 Short Course by Richard Walker.

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