Warrick Lo

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Skills

Languages: C, C++, Python, MATLAB, Tcl, SystemVerilog, ARM/8051/x86 Assembly, Bash, VBA, SQL
Software: Cadence Virtuoso, Xschem, LTspice, Altium Designer, Simulink, Ansys HFSS, Quartus, ModelSim, Linux, FreeBSD, Git
Hardware: Vector Network Analyser, Spectrum Analyser, Software-Defined Radio, FPGA, STM32, Peripheral Interfaces
Certifications: Amateur Radio Operator Certificate, WHMIS

Education

University of British Columbia Expected 2028 April
Bachelor of Applied Science in Electrical Engineering, Minor in Physics
Relevant courses: Analog Integrated Circuit Design, Digital Systems Design, Signals and Systems, Quantum Mechanics
Co-op program: available for up to 16 months

Design Team Experience

UBC Orbit Satellite Design Team 2024 September–Present
Communication Systems Engineer

- Characterised the GRF5504 power amplifier using vector network analysers and spectrum analysers, measuring S-parameters, third-order intermodulation distortion, and 1 dB compression point to evaluate its linear range for satellite signal integrity
- Conducted detailed simulations of spacecraft antenna designs using Ansys HFSS to analyse radiation patterns, calculate theoretical gain, and verify performance against mission link budget constraints
- Authored and executed test plans for power amplifier, RF switch, and low-pass filter evaluation boards

Technical Projects

Two-Stage CMOS Operational Amplifier Design | warricklo.net/opamp 2025 December–2026 January

- Designed a two-stage CMOS operational amplifier with the SKY130 PDK in Xschem, incorporating common-mode feedback and Miller compensation to achieve 50.48 dB gain, 75.8 V/µs slew rate, 75.2° phase margin, 66.2 MHz unity gain frequency, and 282.2 µW power consumption
- Performed AC and transient analyses using ngspice to validate slew rate, settling time, and step response performance
- Created Tcl scripts to automate large-scale tasks and execute parameter sweeps

Five-Stage RISC Processor on FPGA | warricklo.net/cpu 2024 November

- Architected and implemented a Turing-complete, 5-stage, non-pipelined RISC processor in SystemVerilog, synthesised onto the DE1-SoC development board, achieving the **3rd fastest performance** in a class of 300 students
- Developed and executed over 100 test cases in ModelSim to ensure correct system functionality

Autonomous Coin Collecting Robot | warricklo.net/robot 2025 March

- Built an autonomous and remote-controlled coin-collecting robot, capable of detecting and retrieving Canadian coin denominations within a wire-defined boundary using inductive sensors and a Colpitts oscillator-based metal-detection system
- Developed embedded systems in C using STM32 and EFM8 microcontrollers, integrating wireless communication, motor control via H-bridge and optoisolators, and a servo-actuated electromagnetic arm

FM Radio Receiver | warricklo.net/radio 2024 August

- Designed detailed schematics for a radio receiver circuit using Altium Designer
- Incorporated a tuned LC oscillator circuit for frequency selection and demodulation of FM signals and an LM386 audio amplifier circuit to enhance signal output and audio clarity

Research Experience

Undergraduate Research on Energy Harvesting with Piezoelectric Transducers 2026 January–Present

- Analysing rectifying techniques to enhance electromagnetic energy conversion in MEMS devices for low-power applications
- Performing SPICE simulations of energy harvesting through synchronised switch harvesting on inductor (SSHI)

Publications

Eisha Khan, David Tang, Ari Cholakian, Max Xiang, Warrick Lo, and David Michelson, "Using a Dynamic Channel Emulator for Cubesat GNSS Receiver Testing and Integration", *2025 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, Vancouver, Canada, May 2025. doi: 10.1109/CCECE64018.2025.11364492.