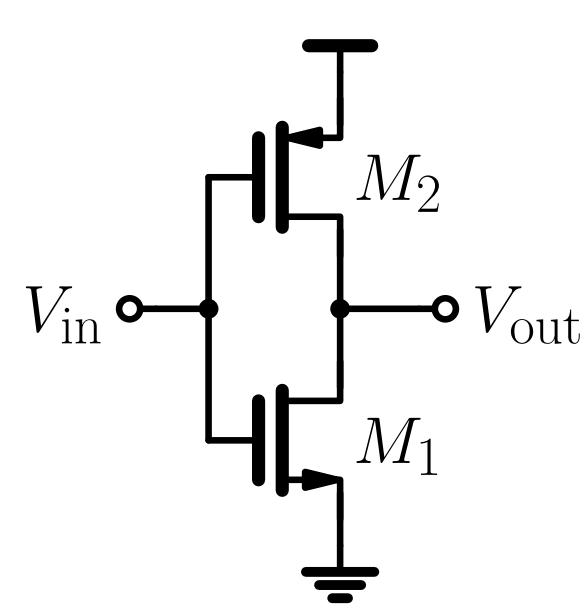
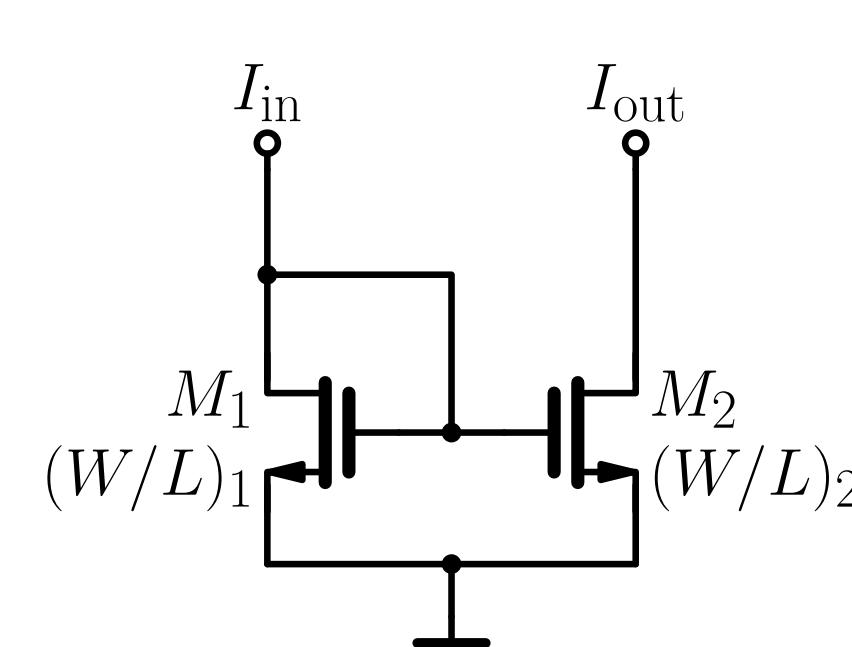


**Circuit No. 1**



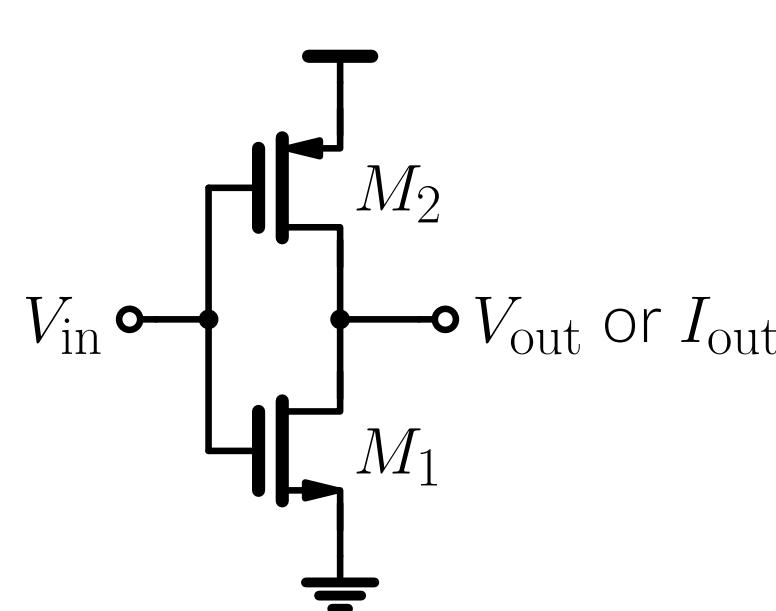
This is the ubiquitous **digital inverter**. The input voltage  $V_{in}$  switches one of both transistors on while the other is off.

**Circuit No. 8**



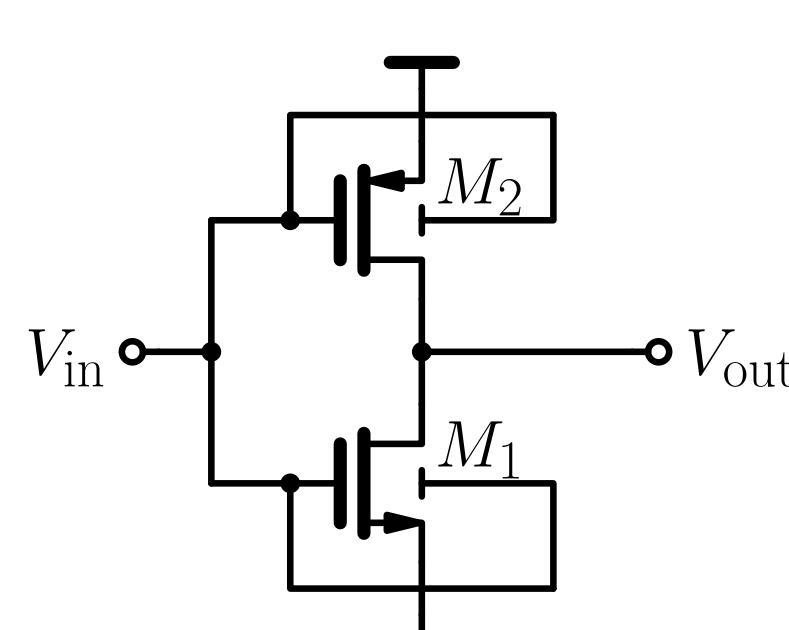
This circuit is the basic **current mirror**, simultaneously copying and sizing of  $I_{out} = (W/L)_2/(W/L)_1 \cdot I_{in}$  according to the dimensions of  $M_1$  and  $M_2$ .

**Circuit No. 2**



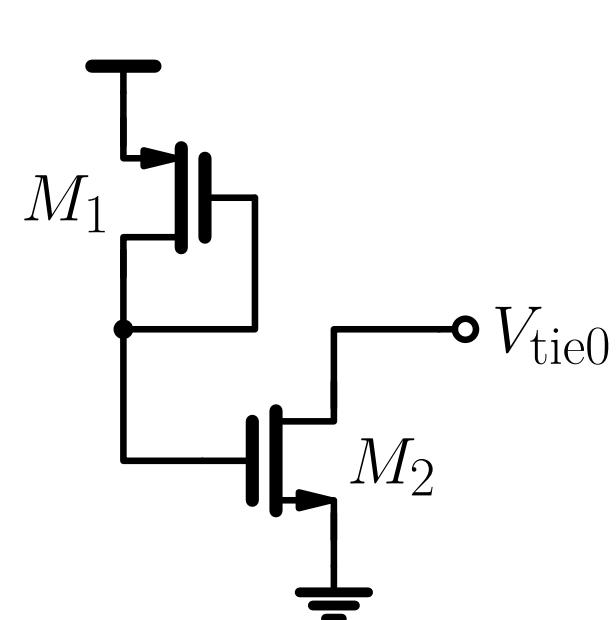
The same structure can be used as a **voltage amplifier** ( $V_{out}$ , with high- $Z$  loading) or low-voltage complementary **transconductance stage** ( $I_{out}$ , with low- $Z$  loading) when both MOS-FET are held in saturation.

**Circuit No. 3**



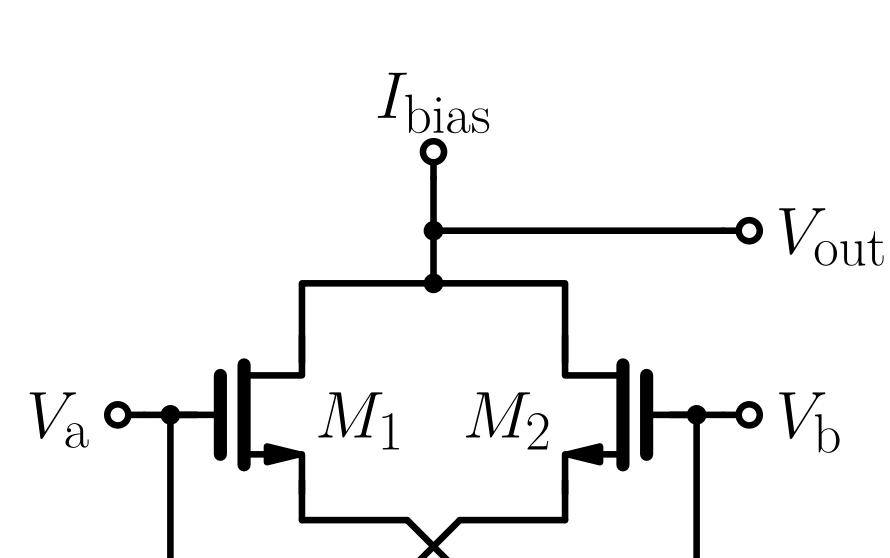
The (dynamic threshold) **DT-MOS inverter** achieves an improved current drive at low leakage current. It needs to be operated at low supply voltages to avoid a forward bias of the well diodes.

**Circuit No. 4**



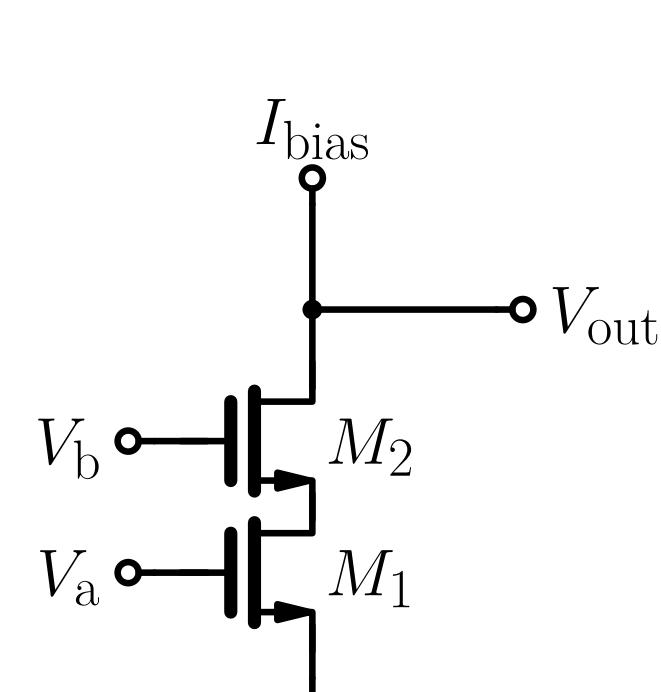
An ESD-safe **tie-zero** for unused CMOS logic inputs (no MOS-FET gate should be tied directly to a supply rail). The tie-one can be constructed accordingly.

**Circuit No. 5**



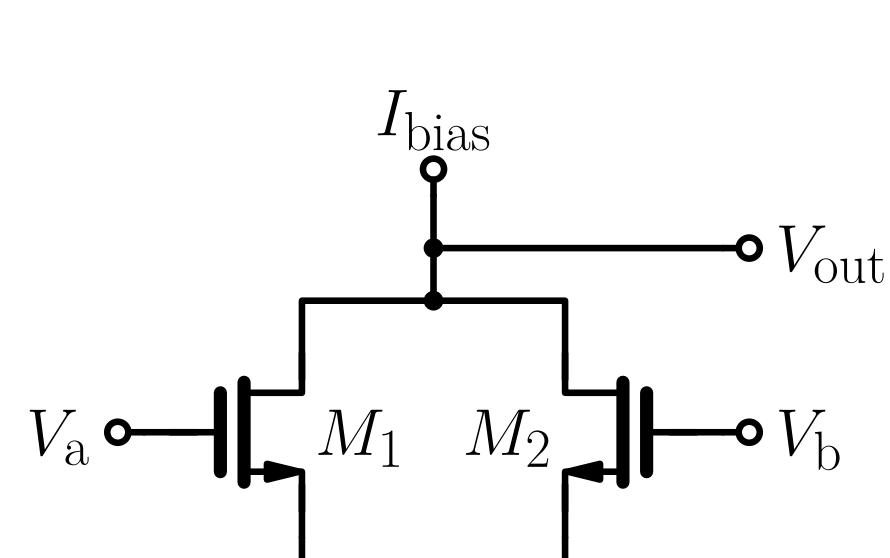
Using a current source  $I_{bias}$  with finite output impedance to bias this structure, this circuit implements an **XNOR** logic function ( $V_{out} = \bar{V}_a \oplus \bar{V}_b$ ). The logic inputs  $V_a$  and  $V_b$  must be driven by low-ohmic logic levels between  $V_{DD}$  and  $V_{SS}$ .

**Circuit No. 6**



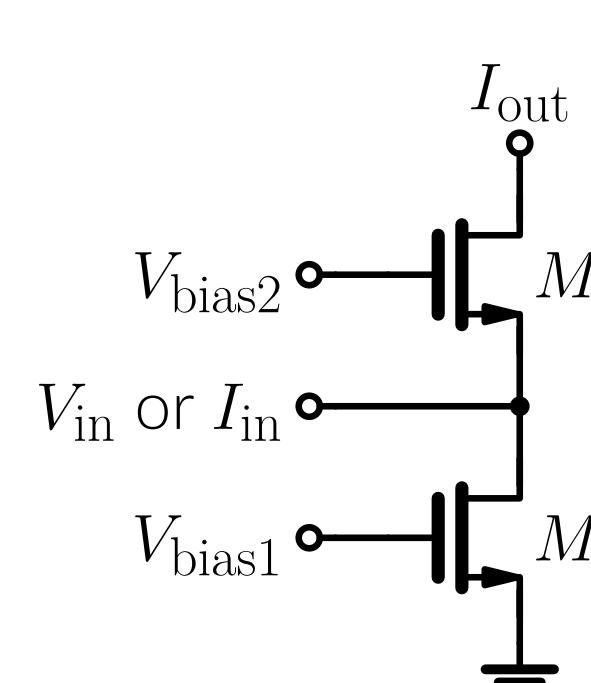
This series connection of two MOS-FETs realizes a logical **NAND** function ( $V_{out} = \bar{V}_a \wedge \bar{V}_b$ ) when driven by logic inputs.

**Circuit No. 7**



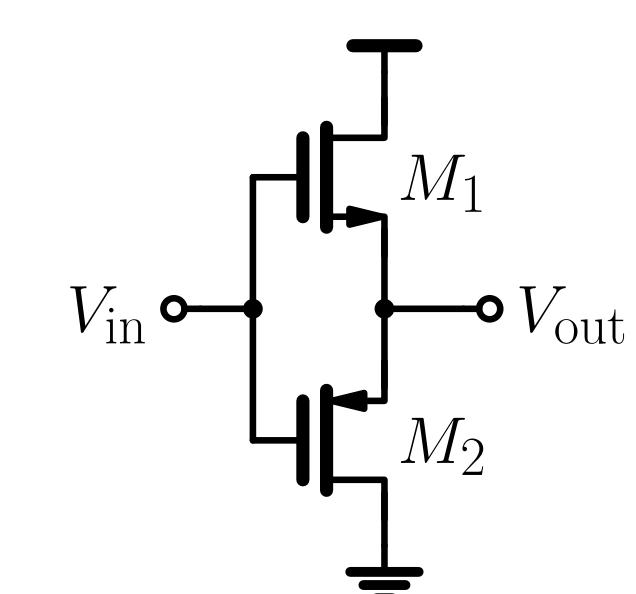
This circuit complements the logic gates and realizes a **NOR** function ( $V_{out} = \bar{V}_a \vee \bar{V}_b$ ).

**Circuit No. 15**



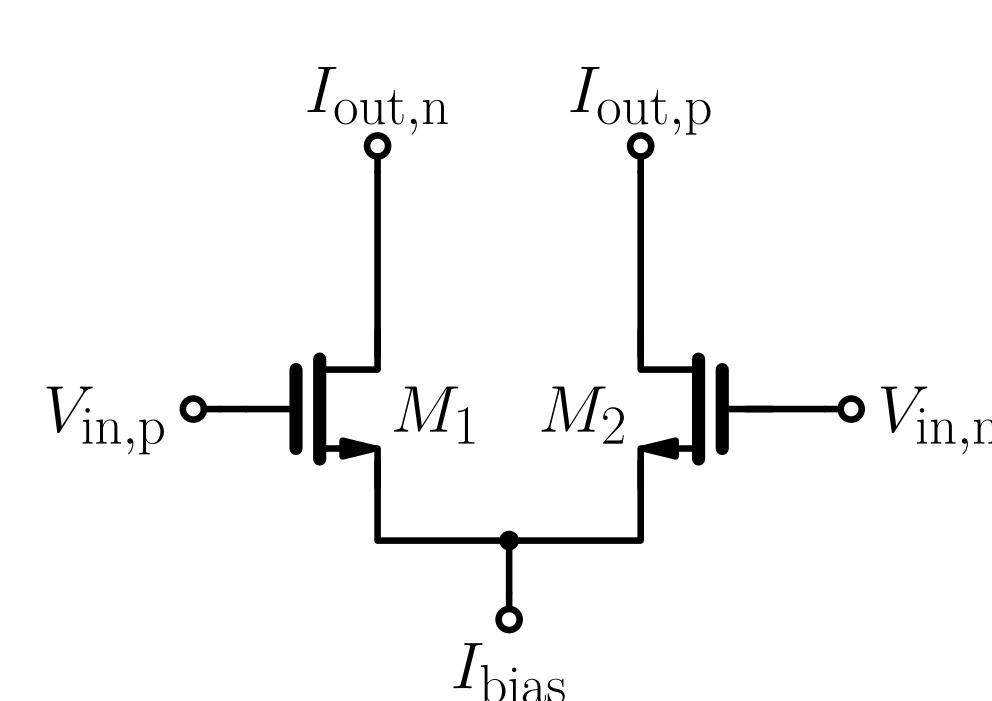
The **common-gate stage**, employing  $M_3$  as a current source to bias transistor  $M_1$ . The input can be either a voltage- or a current-signal.

**Circuit No. 22**



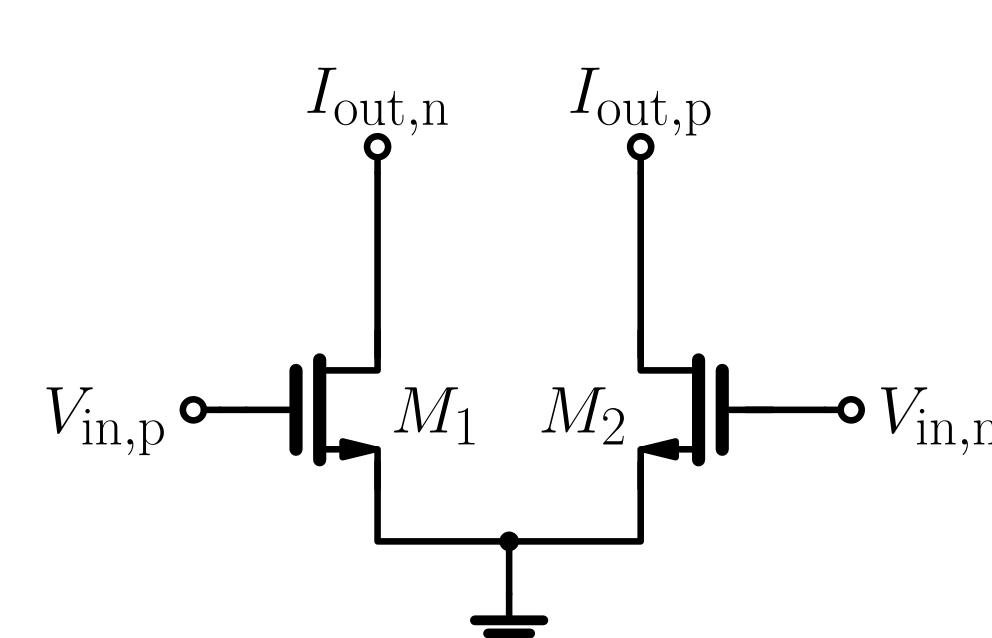
This class-B **push-pull follower** can be considered an enhanced version of the simple source follower. However, lacking a class-A bias component, this structure is subject to cross-over distortion.

**Circuit No. 9**



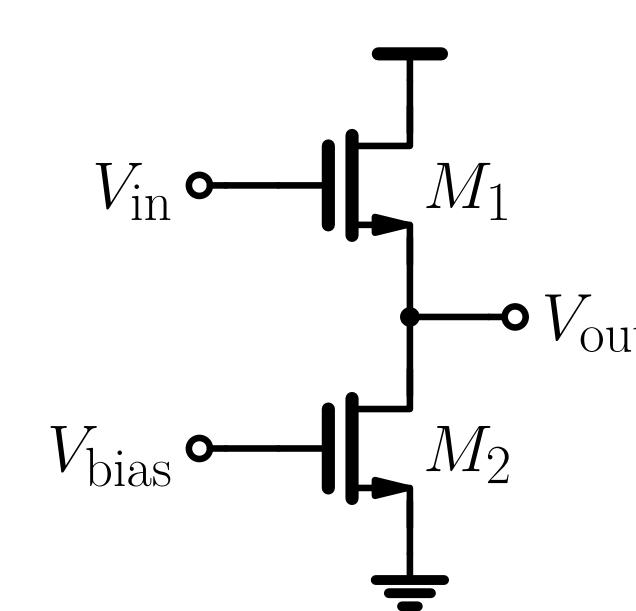
The ubiquitous **differential pair** (or long-tailed pair), like the current mirror, is a fundamental building block in integrated circuits.

**Circuit No. 10**



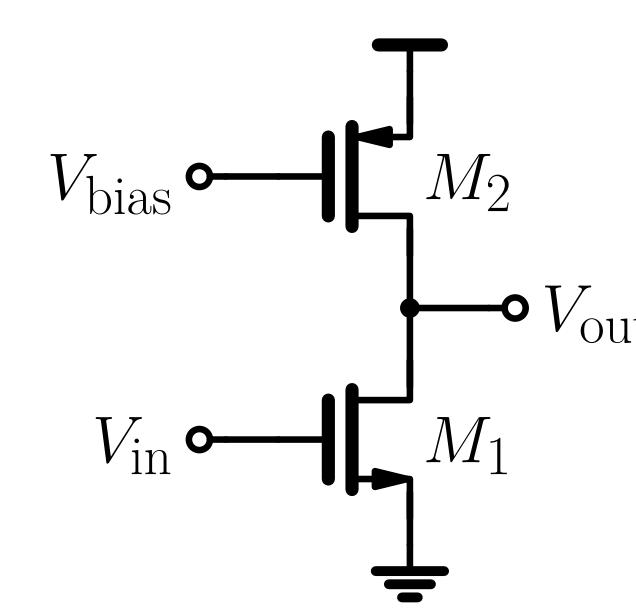
The **pseudo-differential pair** spares the tail current source's headroom in exchange for reduced common-mode rejection, but with the benefit of class-AB operation.

**Circuit No. 11**



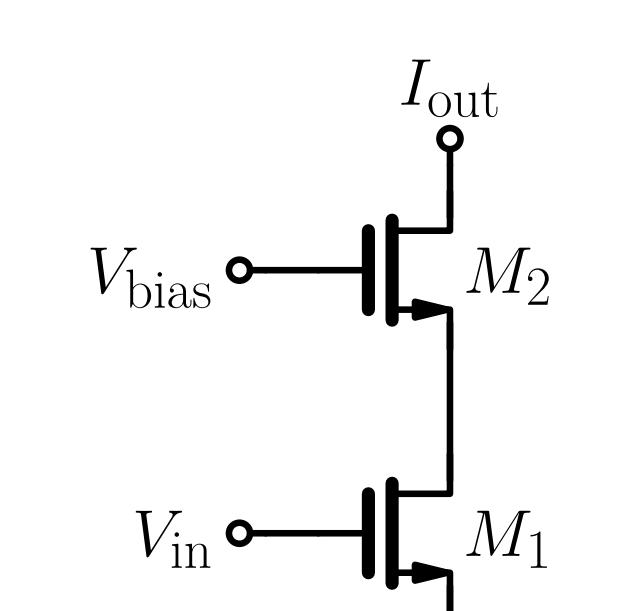
This is the **source follower** (or common-drain stage), utilizing  $M_2$  as a current source to bias  $M_1$ .

**Circuit No. 12**



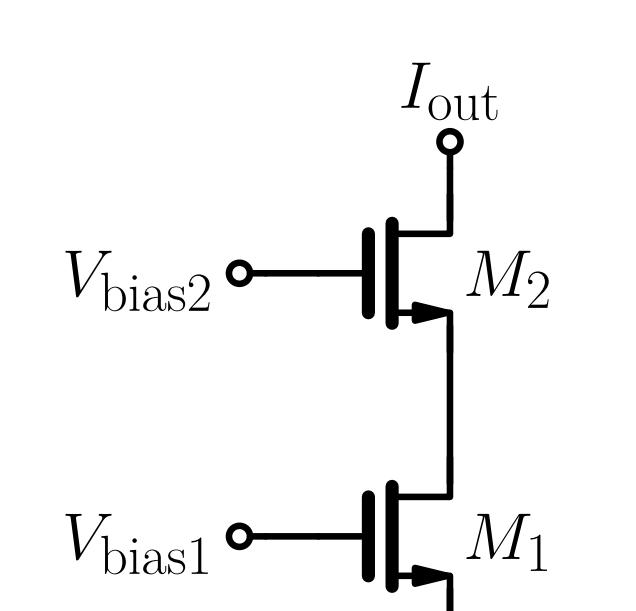
The **common-source** amplifier stage with active load.

**Circuit No. 13**



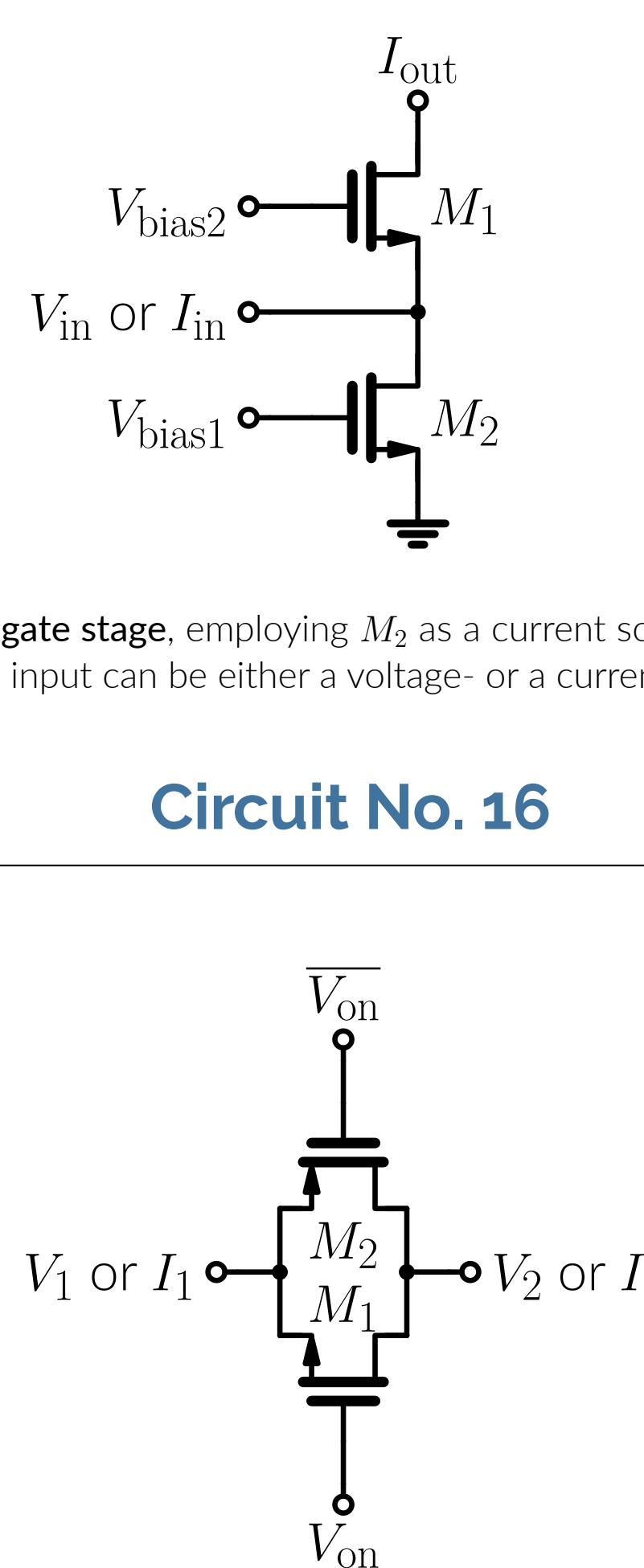
The **cascoded common-source** stage boosts the output impedance of  $M_1$  considerably to  $r_{out} \approx g_{m2}/(g_{ds1} \cdot g_{ds2})$ .

**Circuit No. 14**



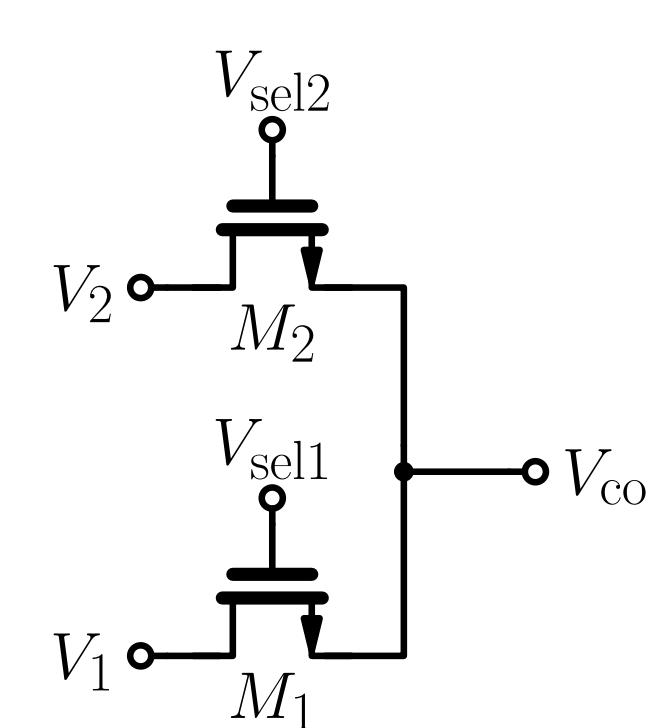
This is the **cascoded common-gate** stage. Note that  $I_{out} \approx I_{in}$ , but the impedance level changes drastically, creating gain or a high output impedance at the output node.

**Circuit No. 16**



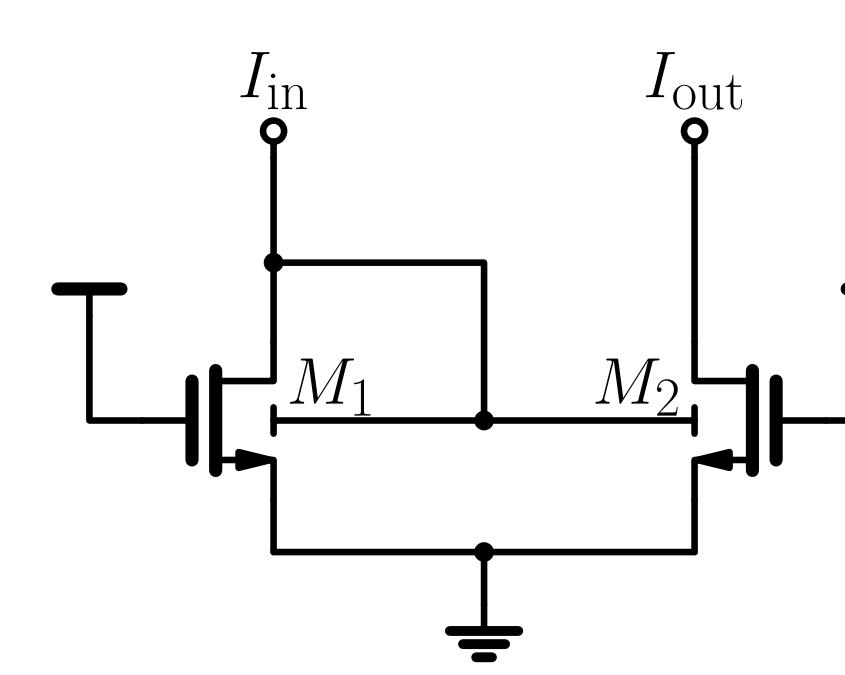
The **transmission gate** switches either voltage ( $V_1$  and  $V_2$ ) or current ( $I_1$  and  $I_2$ ) (and it works rail to rail, too).

**Circuit No. 17**



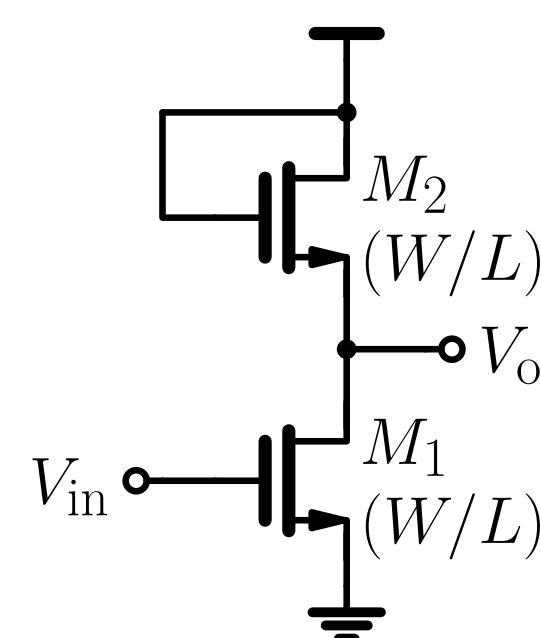
The 2-to-1 **multiplexer**, connecting either  $V_1$  or  $V_2$  to  $V_{com}$ . Depending on  $V_{sel1}$  and  $V_{sel2}$ , the MOS-FETs are alternately switched on or off.

**Circuit No. 18**



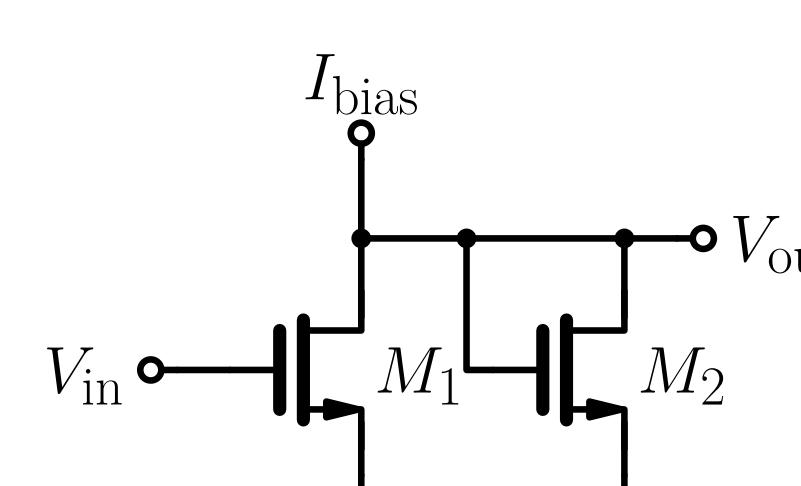
This circuit is an improved **bulk-driven current mirror** that allows low voltage operation, requiring a voltage headroom substantially less than  $V_{GS1}$ .

**Circuit No. 19**



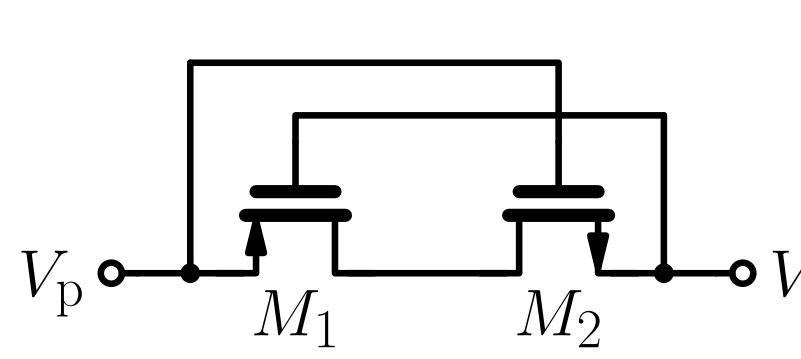
The **common-source amplifier with diode load** is sometimes called a wide-band amplifier due to its potentially high-speed operation. Here, the gain is set precisely to  $A_v = V_{out}/V_{in} = -\sqrt{(W/L)_1/(W/L)_2}$ , only depending on transistor sizing (if we neglect the body effect and finite output conductance).

**Circuit No. 20**



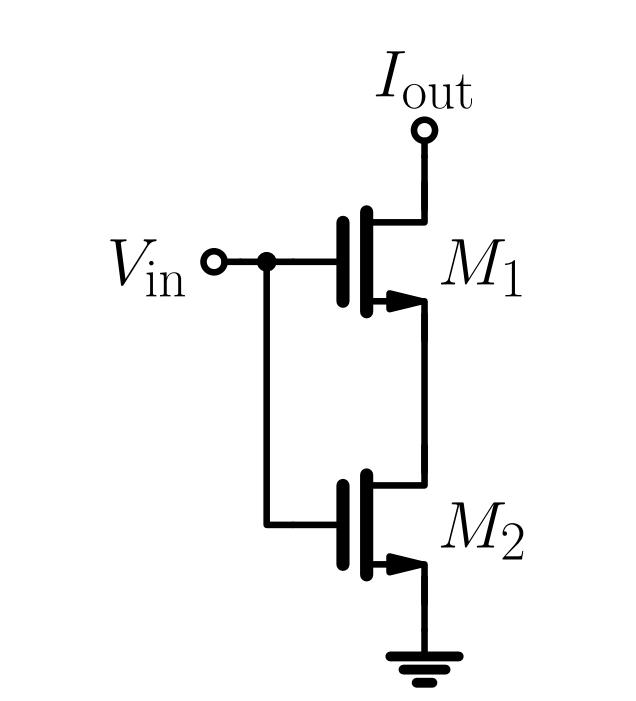
This **wide-band amplifier** has the advantage of a removed body effect in  $M_2$  and a ground-referred output node.

**Circuit No. 21**



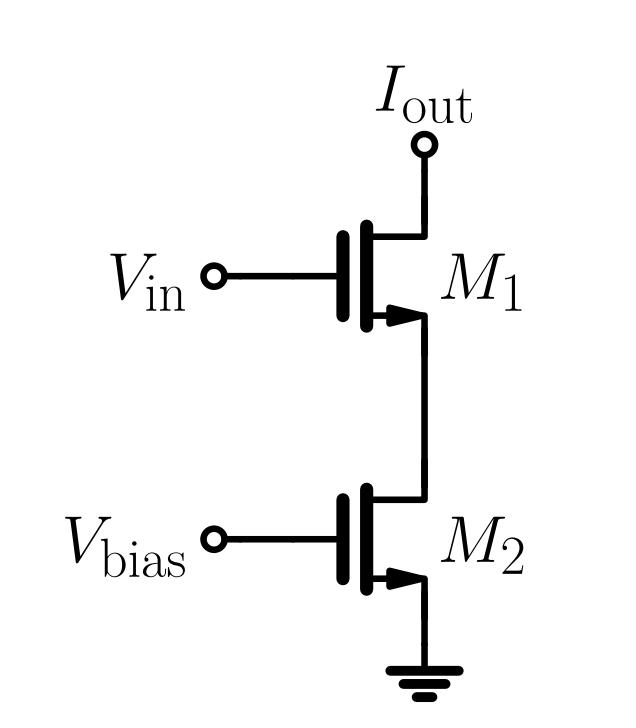
This **ultra-low-power diode (ULPD)** shows a reduced leakage in the reverse direction when  $V_{in} > V_p$ .

**Circuit No. 23**



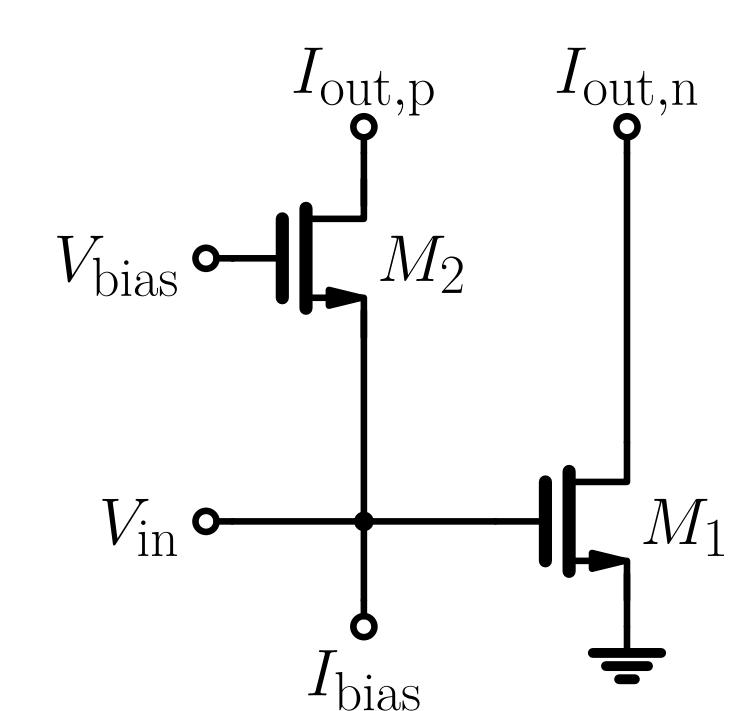
This circuit is a **MOS-FET-R degenerated common-source stage**. By sizing  $M_2$  appropriately, the degeneration can be adapted. This arrangement using two transistors can also increase the length of a (compound) device, for example, in current mirrors, as otherwise, MOS-FETs with different  $L$  will not match well.

**Circuit No. 24**



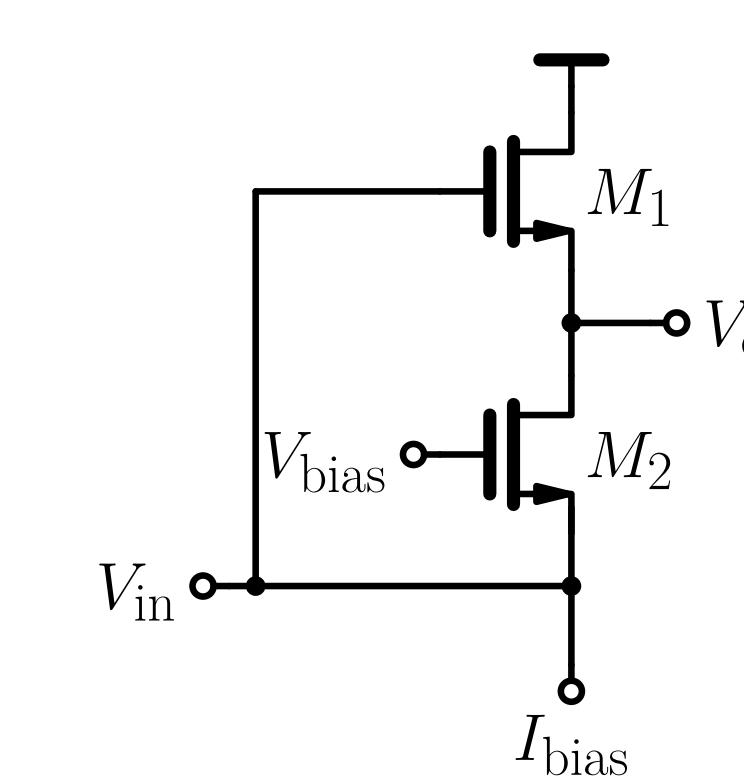
This is a variation of the implementation shown earlier, where the degeneration of  $M_1$  can be adapted by tuning  $V_{bias}$ .

**Circuit No. 25**



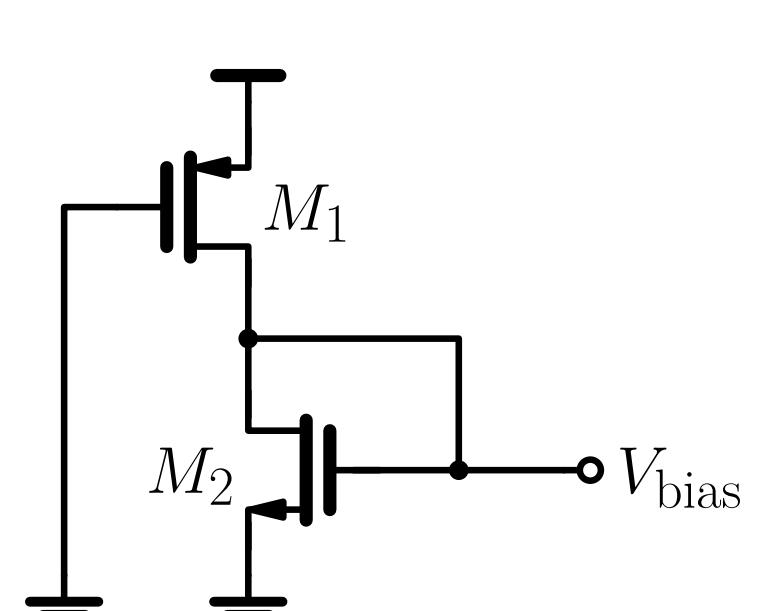
This **common-gate-common-source** topology offers an impedance-matched single-ended input and a differential output while simultaneously canceling noise and distortion.

**Circuit No. 26**



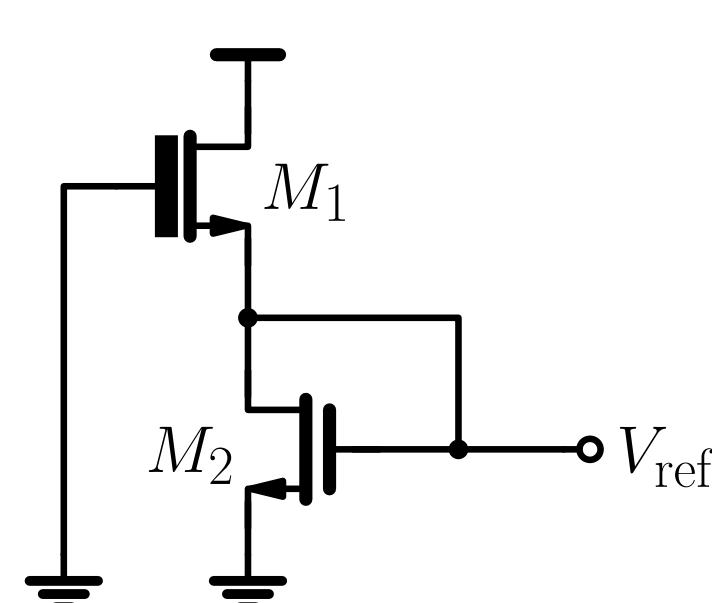
This **low-noise amplifier** was discovered by doing an exhaustive search for potential two-transistor wide-band amplifiers. For practical implementation,  $M_1$  requires an ac-coupling (and proper biasing) in its gate connection to keep  $M_2$  in saturation.

**Circuit No. 27**



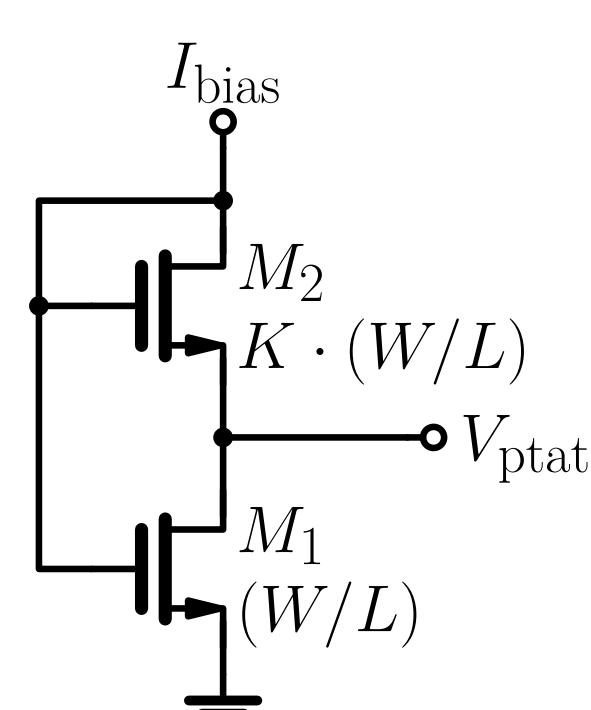
This **(simple) bias voltage generator** uses the current source  $M_1$  to bias  $M_2$  so that  $V_{bias} = V_{GS2}$ . Note that the generated voltage is susceptible to changes in process, supply voltage, and temperature (PVT).

**Circuit No. 28**



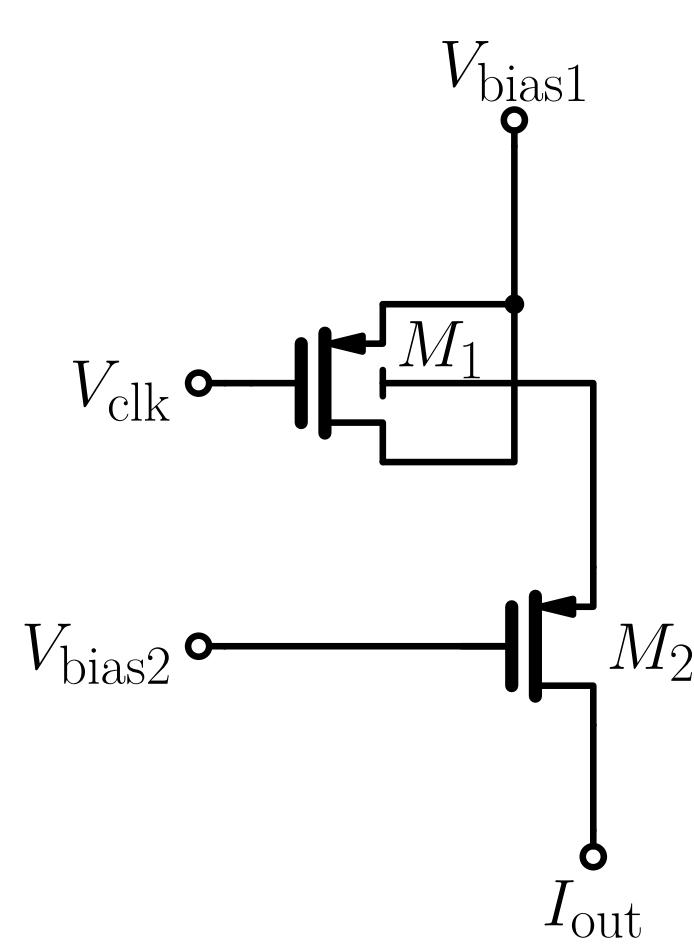
This **constant bias voltage** generator creates a remarkably stable output voltage (note that  $M_1$  and  $M_2$  must have different threshold voltages  $V_{th1} \neq V_{th2}$ ).

**Circuit No. 29**



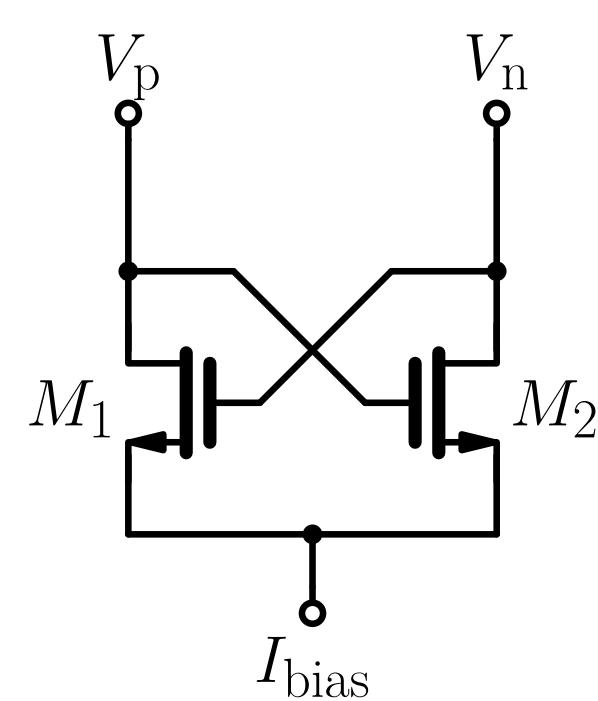
This circuit is a **PTAT voltage** generator, if  $M_1$  and  $M_2$  are kept in sub-threshold operation.

**Circuit No. 30**



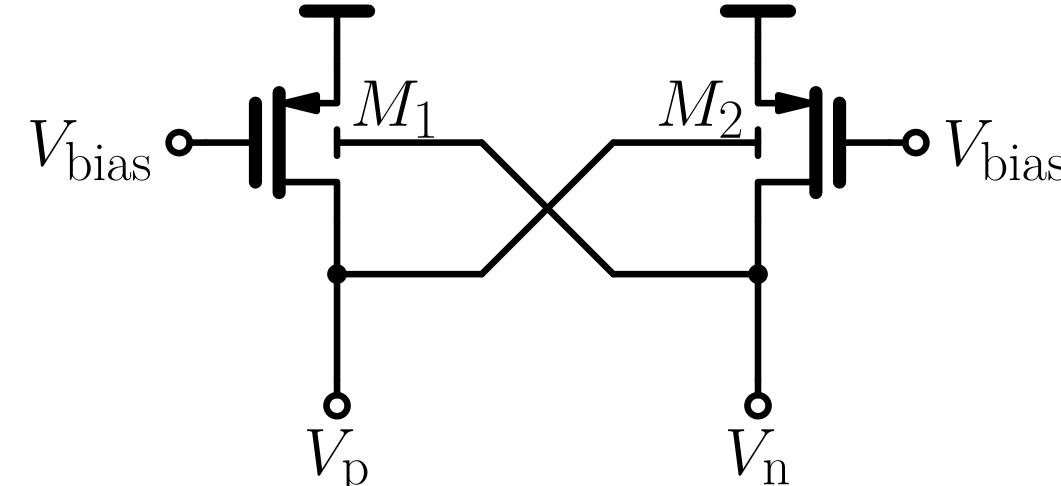
This **pA current source** is based on the periodic filling and flushing of the Si-SiO<sub>2</sub> interface traps by alternating  $M_1$  between accumulation and inversion. It can operate with reasonably high clock frequencies and still create tiny currents.

**Circuit No. 31**



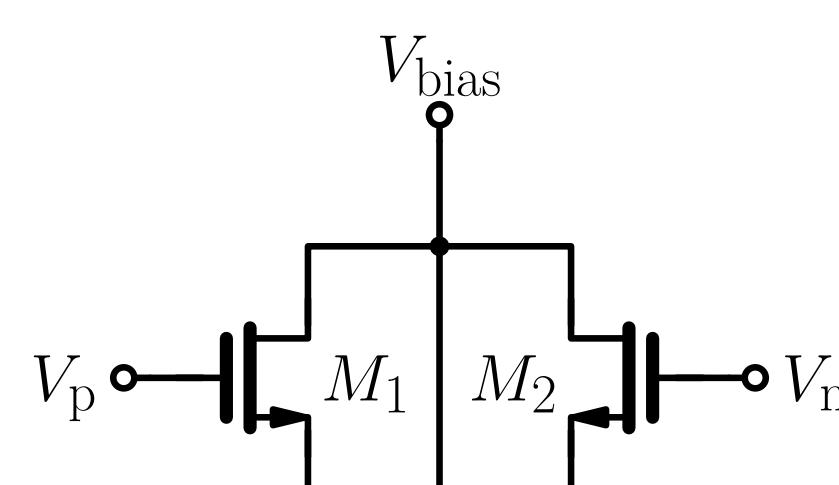
Two transistors with cross-coupling form a **negative resistance** between  $V_p$  and  $V_n$ , mainly employed in oscillators and comparators. As in a differential pair, the bias current source can be replaced by a fixed potential.

**Circuit No. 32**



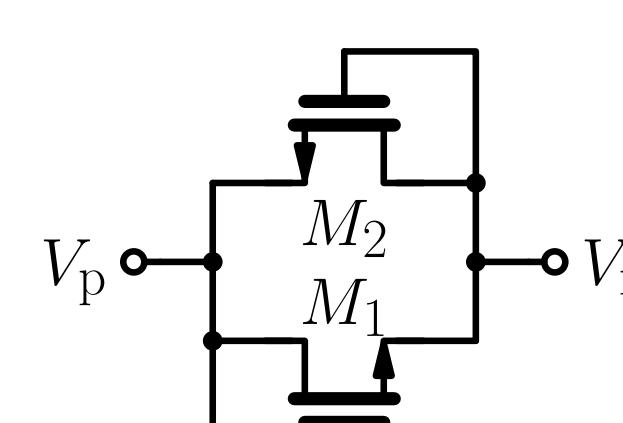
This circuit is a **low-voltage** version of a **cross-coupled pair**, where the body controls the MOS-FETs, avoiding the significant  $V_{GS}$  drop at  $V_p$  and  $V_n$ .

**Circuit No. 33**



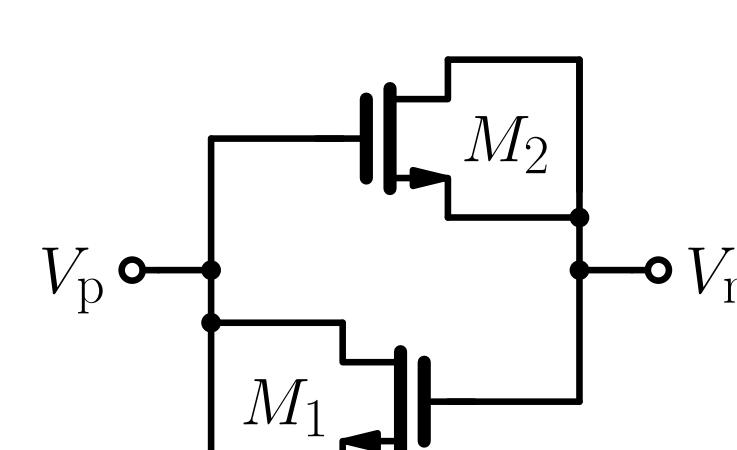
This **varactor** (the capacitance between  $V_p$  and  $V_n$  depends on the bias voltage  $V_{bias}$ ) is often used in voltage-controlled oscillators. In most technologies, the NMOS can be put inside the n-well so that the varactor works in accumulation, providing an optimized tuning range and high  $Q$ .

**Circuit No. 34**



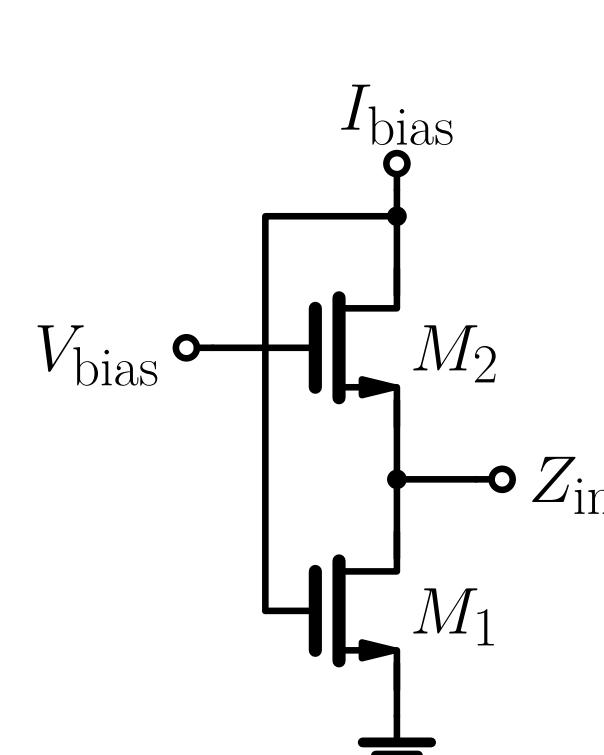
The **anti-parallel MOS-FET diodes** can be employed for many things, for example, voltage clamping.

**Circuit No. 35**



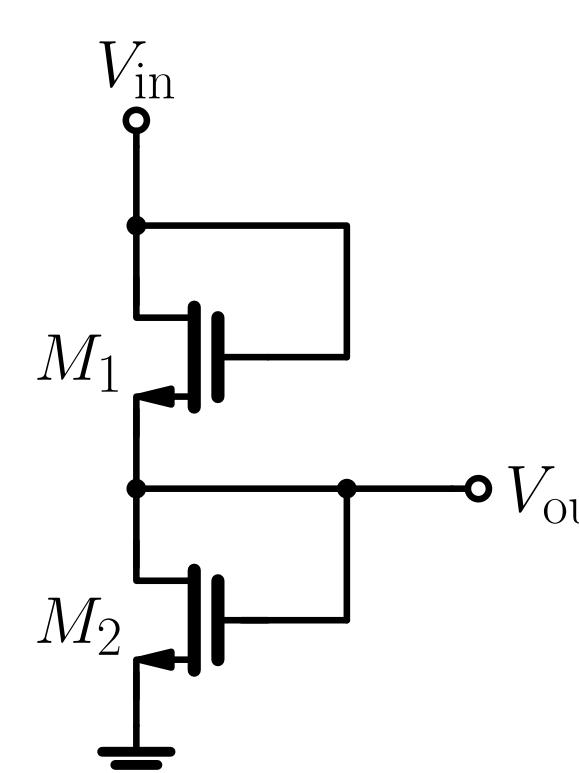
The **anti-parallel MOS-FET capacitors** make the differential capacitance between  $V_p$  and  $V_n$  more linear and symmetrical. As in a varactor, an NMOS-in-n-well is an option.

**Circuit No. 36**



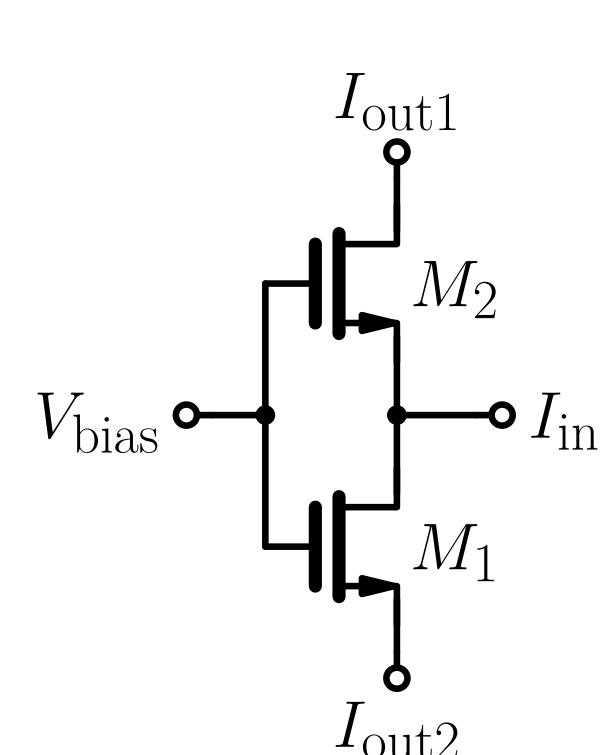
This circuit, which is a similar configuration as the flipped voltage follower, can function as an **active inductor**, providing  $L = C_{GS1}/(g_{m1} \cdot g_{m2})$ .

**Circuit No. 37**



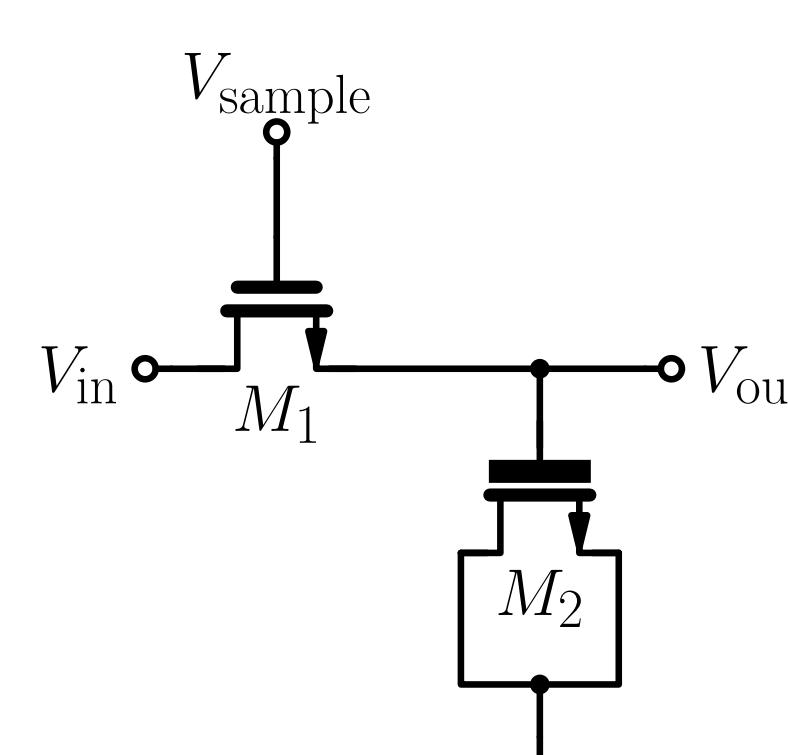
This circuit is an **area-efficient voltage divider**. If  $M_1$  and  $M_2$  are of the same size, then  $V_{out} \approx V_{in}/2$ . Often, a PMOS version is a better choice since it can avoid the body effect by tying the body to the respective source for  $M_1$  and  $M_2$ .

**Circuit No. 38**



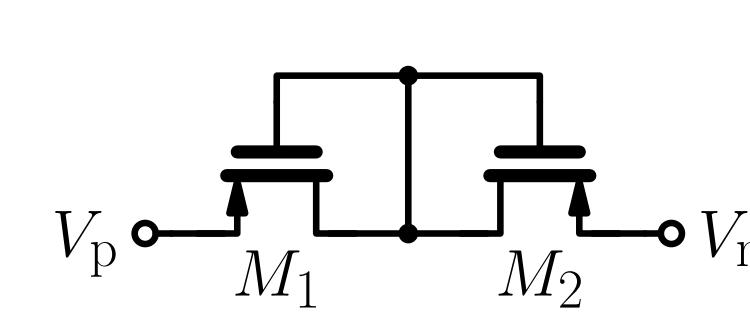
This implementation is the **Bolt current divider** (if  $M_1$  and  $M_2$  are of identical size, then  $I_{in}$  is precisely split in half between  $I_{out1}$  and  $I_{out2}$ ).

**Circuit No. 39**



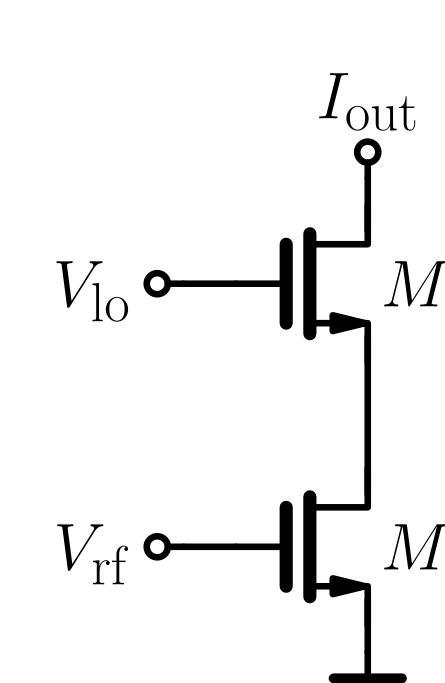
This is a **sample-and-hold** circuit as used in a lot of ADC implementations, using the gate capacitance of  $M_2$  as a storage capacitor (a low to zero  $V_{th}$  would be an advantage in this case).

**Circuit No. 40**



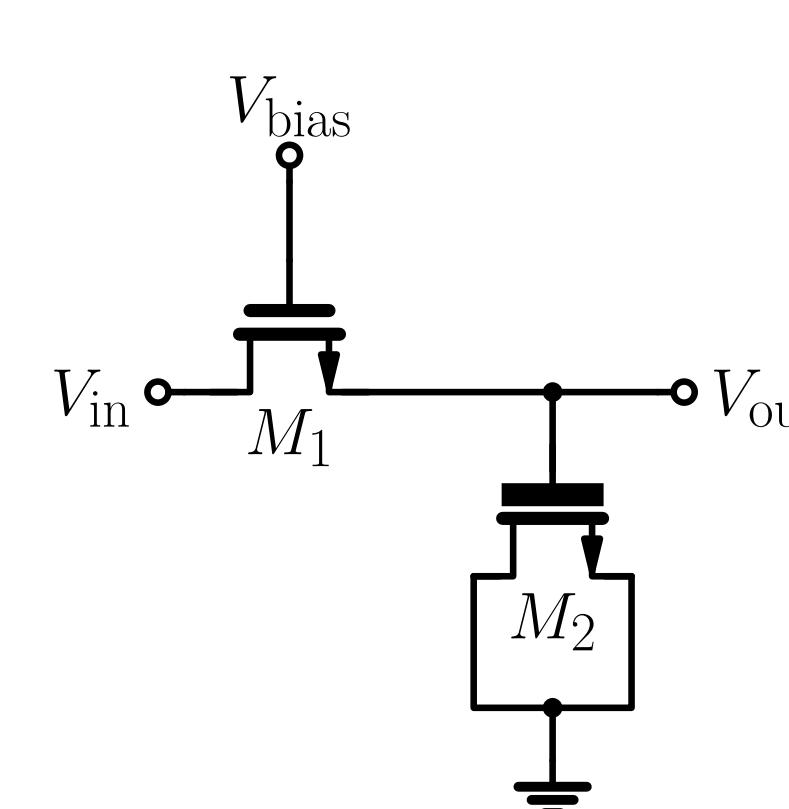
This arrangement creates an enormous resistance between  $V_p$  and  $V_n$ , although susceptible to temperature and process variations.

**Circuit No. 41**



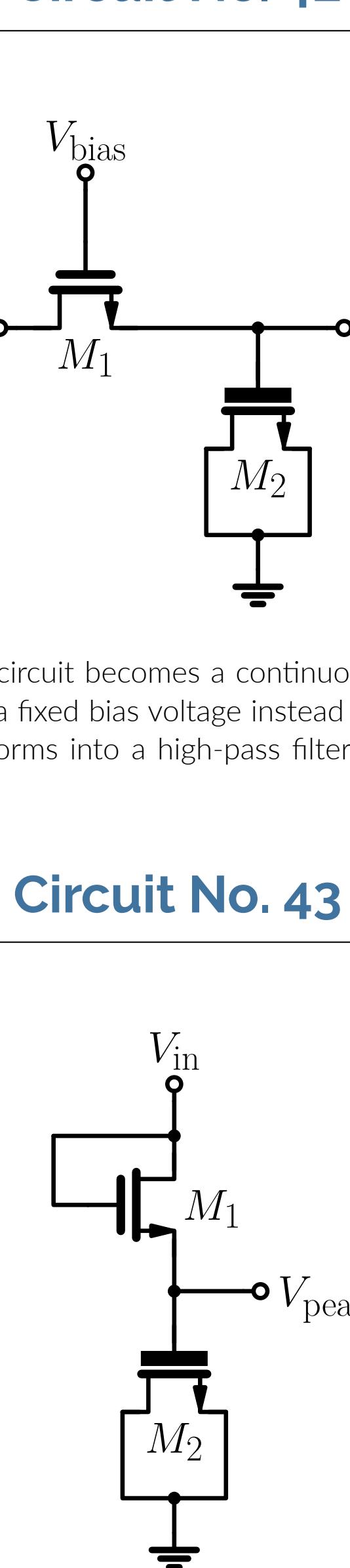
In this **dual-gate MOS-FET mixer**, the periodic local-oscillator signal  $V_{rf}$  causes the time-variant change of the transconductance of  $M_1$ , resulting in a frequency conversion from the input  $V_{lo}$  to the output  $I_{out}$ .

**Circuit No. 42**



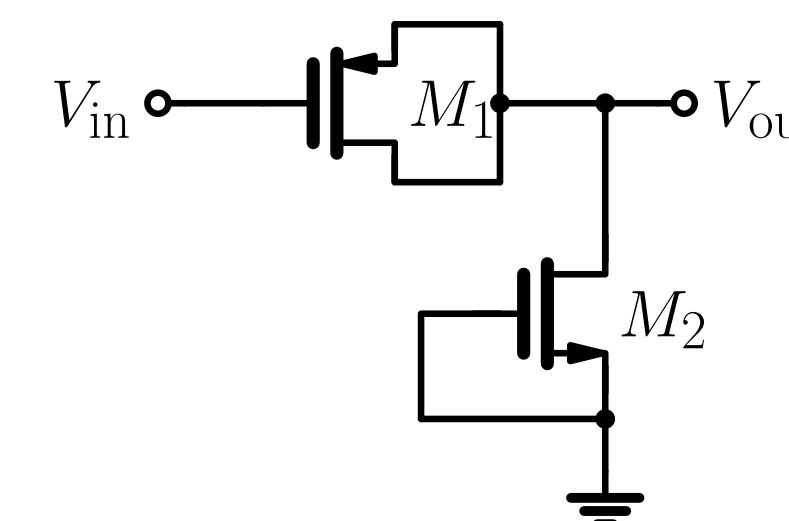
This circuit is a perfectly **linear I-to-V converter** with  $V_{out}/I_{in} = [\mu C_{ox} \cdot (W/L) \cdot (V_{bias} - 2V_{th})]^{-1}$ , if we assume a square-law behavior, neglect the body effect, and  $M_1$  and  $M_2$  are of same size and kept in saturation.

**Circuit No. 43**



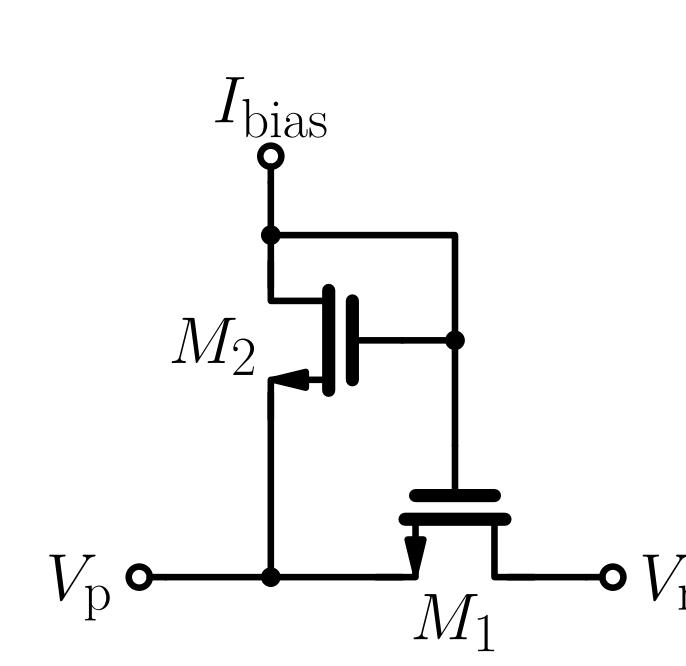
The sample-and-hold circuit becomes a continuous-time **low-pass filter** if  $M_1$  is connected to a fixed bias voltage instead of a clock signal. Note that this circuit transforms into a high-pass filter when  $M_1$  and  $M_2$  are swapped.

**Circuit No. 44**



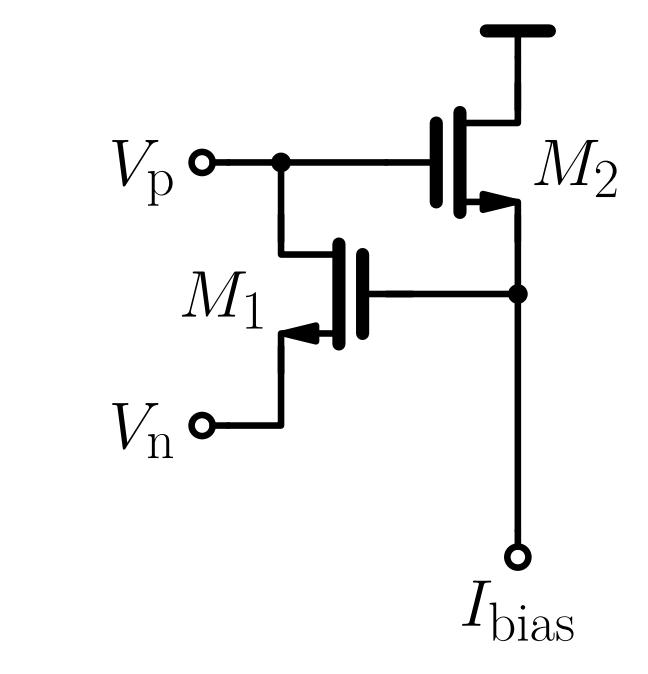
A similar circuit to the peak detector can function as an **approximate voltage doubler** when driven by a sinusoidal input voltage (on negative swings of  $V_{in}$  the capacitor  $M_1$  gets charged to  $|V_{in}| - V_{gs2}$ , which is added to  $V_{in}$  during positive swings when  $M_2$  is off). As in any circuit with negative voltages, proper connection of the wells is required.

**Circuit No. 45**



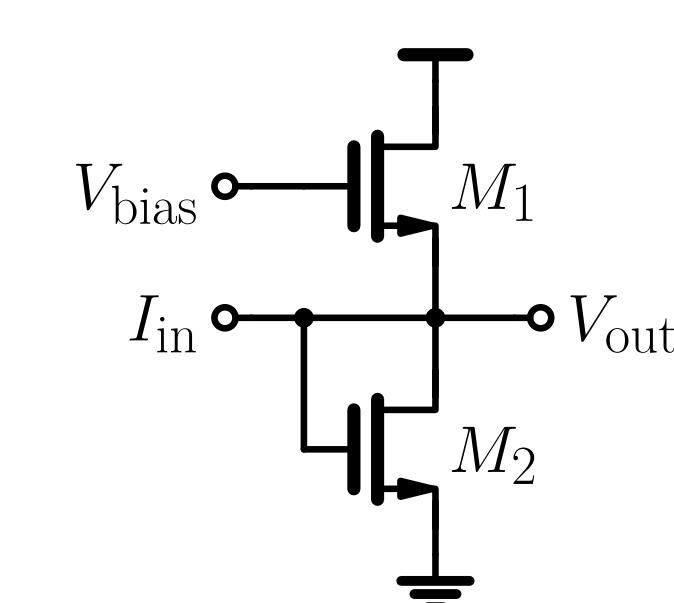
This circuit implements a current-controlled (high-impedance) floating **resistor** between  $V_p$  and  $V_n$ .

**Circuit No. 46**



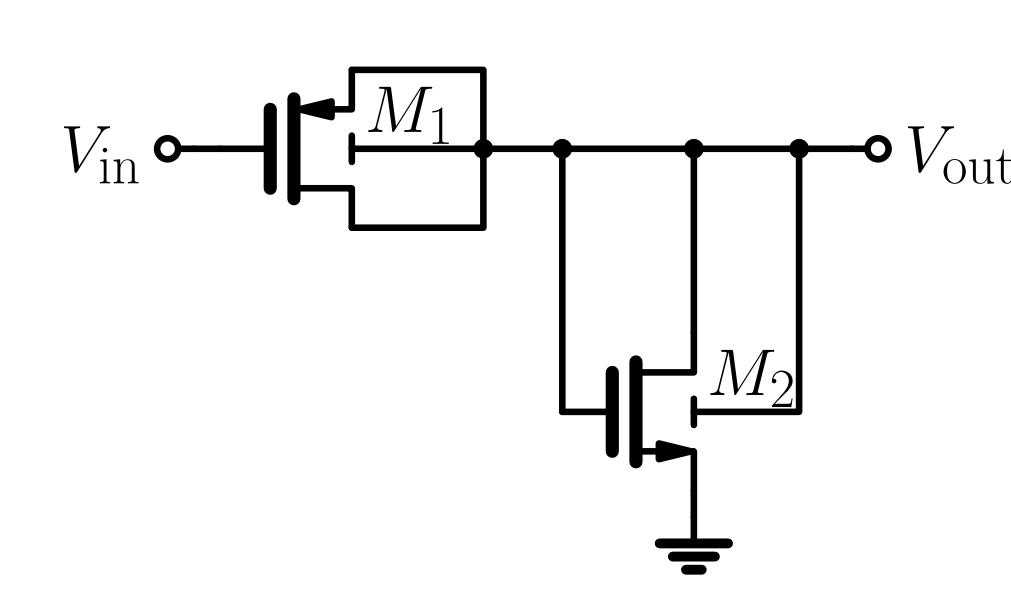
The floating **level shift** (or "floating battery") effectively shifts a bias point between  $V_p$  and  $V_n$ , as  $V_{shift} = V_p - V_n = V_{gs1} + V_{gs2}$ .

**Circuit No. 47**



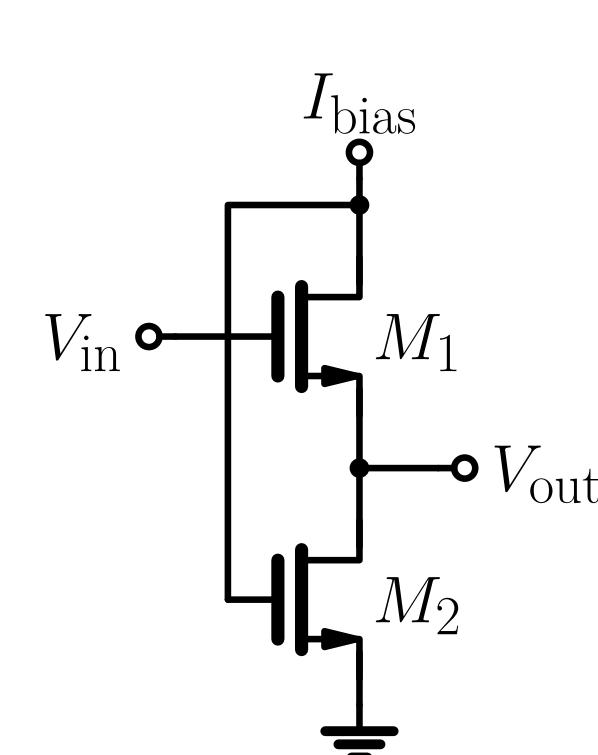
This circuit is a perfectly **linear I-to-V converter** with  $V_{out}/I_{in} = [\mu C_{ox} \cdot (W/L) \cdot (V_{bias} - 2V_{th})]^{-1}$ , if we assume a square-law behavior, neglect the body effect, and  $M_1$  and  $M_2$  are of same size and kept in saturation.

**Circuit No. 48**



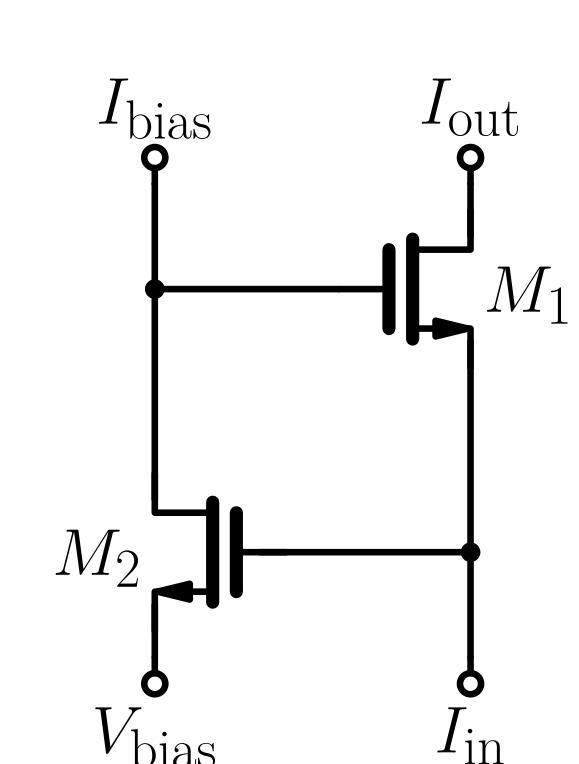
This **level-shifter circuit** shifts a digital input voltage  $V_{in}$  to an output voltage  $V_{out}$  swinging around  $V_{ss}$ .

**Circuit No. 49**



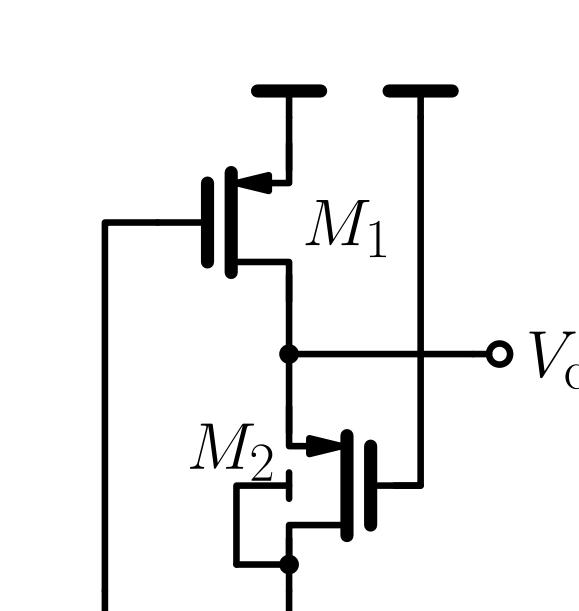
The **flipped voltage follower** is an improved version of the standard source follower, employing feedback to lower the output impedance to  $r_{out} = g_{ds2}/(g_{m1} \cdot g_{m2})$ .

**Circuit No. 50**



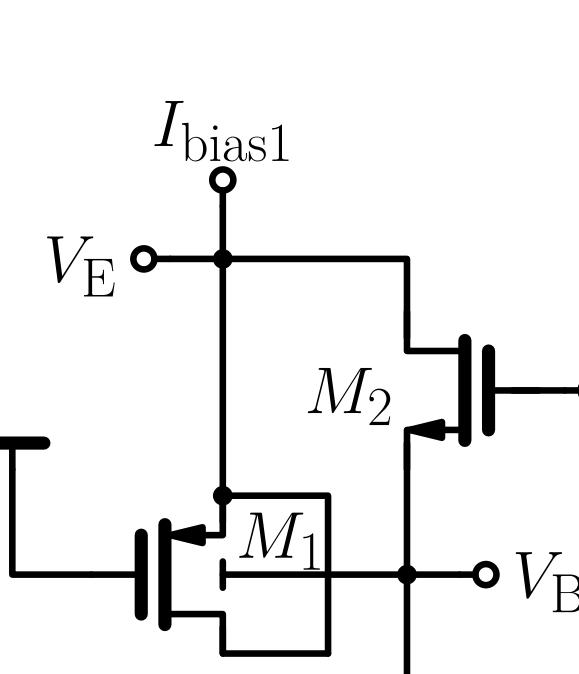
The **regulated cascode** improves the effect of the cascode  $M_1$  by  $g_{m2}/g_{ds2}$  due to feedback. Note that the source of  $M_2$  can be tied to ground if combined with a common-source input stage.

**Circuit No. 51**



Exploiting the parasitic (lateral) PNP transistor inherent in a PMOS structure, this simple **CTAT voltage generator** can be created.

**Circuit No. 52**



The parasitic BJT (lateral or vertical) often suffers from poor  $\beta \ll 10$ . This circuit forces the collector current of the parasitic (vertical) PNP (realized by  $M_1$ ) to  $I_C = I_{bias1} - I_{bias2}$ , although the collector terminal (being the p-substrate) is not accessible. By doing this, the resulting  $V_{EB} = V_E - V_B$  can be accurately used in a bandgap circuit.